ISSN:1306-3111
e-Journal of New World Sciences Academy
2009, Volume: 4, Number: 4, Article Number: 1A0049

ENGINEERING SCIENCES
Received: April 2009
Accepted: September 2009
Series : 1A
ISSN : 1308-7231

İbrahim Yücedağ
Duzce University
yucedagi@gmail.com
Düzce-Turkey

ON THE DENSITY DISTRIBUTION PROFILES OF INTERFACE STATES IN Al/SiO_2/p-Si (MIS) STRUCTURES

ABSTRACT

In this study, the energy distribution profile of the interface states (N_{ss}) and their relaxation time (τ) of Al/SiO_2/p-Si (MIS) structure with a thin (32Å) SiO_2 have been investigated by use the conductance methods. The C-V-f and G/ω-V-f characteristics of these devices were measured in the frequency range of 0.2kHz-100kHz. The experimental characteristics of MIS structure show fairly large frequency dispersion especially at low frequencies due to R_s and N_{ss}. The capacitance of this structure decreases with increasing frequency. The increase in C especially at low frequencies result forms the presence of N_{ss}. The N_{ss} and τ profiles have been determined in the band-gap of Si. The main value of N_{ss} was found about $3.5x10^{14}$ $eV^{-1}cm^{-2}$ and slightly changes. The values of relaxation time range from $1.05x10^{-5}$ s to $1.58x10^{-3}$ s and have shown an exponential rise with bias from the top of the valance bend towards the mid-gap

Keyword: Interface States, Relaxation Time, Conductance Method, Series Resistance, Thin Insulator Layer

Al/SiO_2/p-Si (MIS) YAPILARDA ARAYÜZEY DURUMLARININ YOĞUNLUK DAĞILIM PROFİLİ

ÖZET

Bu çalışmada, ince bir (32Å) SiO_2'li Al/SiO_2/p-Si (MIS)yapının ara yüzey durumu (N_{ss}) ve gevşeme zamanının (τ) enerji dağılımı profili iletkenlik yöntemleri kullanılarak araştırılmıştır. Bu cihazların C-V-f ve G/ω-V-f karakteristikleri 0,2 kHz–100 kHz frekans aralığında ölçülmüştür. Bu yapının deneysel karakteristikleri R_s ve N_{ss} yüzünden özellikle düşük frekanslarda oldukça büyük frekans dağılımı göstermektedir. Bu yapının kapasitansı artan frekans ile azalmaktadır. Düşük frekanslarda özellikle C'deki artış N_{ss}'in varlığını ortaya koymaktadır. N_{ss} ve τ özellikleri Si'nin bant aralığında tespit edilmiştir. N_{ss}'in temel değeri yaklaşık olarak $3x10^{14}$ $eV^{-1}cm^{-2}$ civarında ve çok az değişiklikle bulundu. Gevşeme zamanının değerleri $1.05x10^{-5}$ s ile $1.58x10^{-3}$ s aralığında ve orta boşluğa doğru üstel olarak artış göstermiştir.

Anahtar Kelimeler: Ara Yüzey Durumları, Gevşeme Zamanı, İletkenlik Yöntemi, Seri Direnç, İnce Yalıtkan Tabaka

1. INTRODUCTION (GİRİŞ)

To prevent the interface diffusion and reaction between the metal and semiconductor an insulator layer and such as SiO_2, SnO_2 and Si_3N_4 generally inserted at metal/semiconductor interface. Thus, metal/semiconductor (MS) structure is converted to a metal-insulator-semiconductor (MIS) structure. The combination of SiO_2/Si is believed to be the most stable and its excellent interface characteristics. In recent years, MIS diodes or structures become more and more important in a great variety of fields of modern semiconductor technology. The performance of these structures and their reliability depend highly on the quality and the degree of technological control of the intermediate thin insulator layer, R_s and N_{ss}. The semiconductor/insulator (Si/SiO_2) interface and defects on its neighborhood have been extensively studied in the past four decades [1-12]. In the real MIS structures, the localized N_{ss} exist at the Si/SiO_2 and the device behavior is different from an ideal case due to the presence of these localized N_{ss}. The reason for their existence is the interruption of the periodic lattice structure at the surface, surface preparation, formation of insulator layer and impurity concentration of semiconductor [1, 2, 5, 6, 7, 8, 9, 10, and 11]. These N_{ss} usually cause a bias shift and frequency dispersion of the C-V and G/ω-V curves [1, 2, 3, and 4]. The applied a.c. signal causes the Fermi level to oscillate about the mean positions governed by the d.c. bias, when the MIS diode is in depletion. The N_{ss} at the Fermi level change their occupancy by capture and emission process, and a conductance loss occurs, since the response of states lags behind the phase of the signal. The N_{ss} is found from the conductance loss resulting from the interface states by measuring the a.c. conductance as a function of bias voltage in depletion at various frequencies. In the equivalent circuit of MIS diode, the N_{ss} are represented by a capacitance C_p and conductance G_p in parallel with the semiconductor space-charge capacitance C_{sc}. In this circuit, the oxide capacitance C_{ox} is in series with those components. The G_p/ω vs f curve at a constant bias voltage shows a maximum and G_p/ω is proportional to the N_{ss}, for a p-MIS diode, the N_{ss} and the capture cross-section are nearly constant over energy of a few kT/q, and the G_p/ω are given by Depas at al. in [5].

2. RESEARCH SIGNIFICANCE (ÇALIŞMANIN ÖNEMİ)

To achieve a better understand of the effects of different charge N_{ss} and τ on the MIS structures we used admittance spectroscopy methods. Therefore, we have obtained the forward and reverse bias C-V and G/ω-V measurements of these structures by the use of a computerized HP 4192A LF impedance analyzer (5 Hz-13 MHz) at room temperature with frequencies ranging from 0.2 kHz to 100 kHz.

3. EXPERIMENTAL PROCEDURE (DENEYSEL YÖNTEM)

The MS structures used in this study were fabricated using p-type (boron-doped) single crystal silicon wafer with <100> surface orientation, having thickness of 280 μm, 2" diameter and 8 Ω.cm resistivity. For the fabrication process, the Si wafer was degreased for 5 min. in boiling trichloroethylene, acetone and ethanol consecutively and then etched in a sequence of H_2SO_4 an H_2O_2, 20% HF, a solution of $6HNO_3$: 1HF: $35H_2O$, 20% HF. Preceding each cleaning step, the wafer was rinsed thoroughly in de-ionized water of resistivity of 18 MΩ-cm. The detail fabrication procedures have been given in our previous study [13].

The C-V and G/ω-V have been measured at room temperature in the frequency range of 0.2 kHz - 100 kHz. Small sinusoidal signal of 40 mV peak to peak from the external pulse generator is applied to the sample in order to meet the requirement [1,2]. All measurements were carried out with the help of a microcomputer through an IEEE-488 AC/DC converter card.

4. RESULTS AND DISCUSSION (SONUÇLAR VE TARTIŞMA)

4.1. Frequency Dependence Capacitance and Conductance Measurements (Frekansa Bağlı Kapasitans ve İletkenlik Ölçümleri)

Several experimental methods have been developed for the study of the Si-SiO_2 N_{ss} essentially based on differential capacitance measurement [1, 7, and 11]. Among these methods, the conductance method maps out the energy distribution of the N_{ss} within band gap of Si [1 and 2]. In addition, this method can identify both bulk and interface defects when used on MIS diodes and particular when the diodes are based in depletion and superimposed ac signal is applied across the diode terminals [1]. Therefore, the C-V and G/ω-V measurements were performed in the dark at frequency range of 0.2 KHz–100 kHz and are given in Figure 1. As small sinusoidal signal of 40 mV p-p from the external pulse generator is applied to the sample in order to meet the requirement [1 and 2].

Figure 1(a) and (b) show the measured C_m-V and G_m/ω-V characteristics of MIS structure, respectively, measured at various frequencies with an oscillator level of 40 mV peak to peak at room temperature. The applied voltage range was between +2 V and +6 V. The three regimes of accumulation, depletion and inversion are clearly shown for each ac frequency, verifying a typical MIS behavior. It is shown that there is the significantly larger frequency dispersion in C-V and G/ω-V curves indicate existence of N_{ss} that are in thermal equilibrium with the Si and cannot communicate with the metal. Usually, there are various kinds of states with different lifetimes at the Si/SiO_2 interface. If the C-V or G/ω-V measurements are carried out at sufficiently high frequency such that τ is much larger than ($T=1/\omega$) the N_{ss} cannot follow an ac signal [14]. At high frequency, the R_s become significant because of the low impedance of the capacitor. Hence, one must account for the simultaneous presence of both the R_s and shunt parasitic resistances in the C-V and G/ω-V measurement. In this case, the device capacitance may be found from a single measurement by neglecting the shunt resistance and determining the capacitance. In addition to the C-V characteristic of the MIS structure in Figure 1(a) consists of a peak located at low forward bias region due to the N_{ss} contribution shifts from the high forward bias voltage the low bias voltage as increasing frequency.

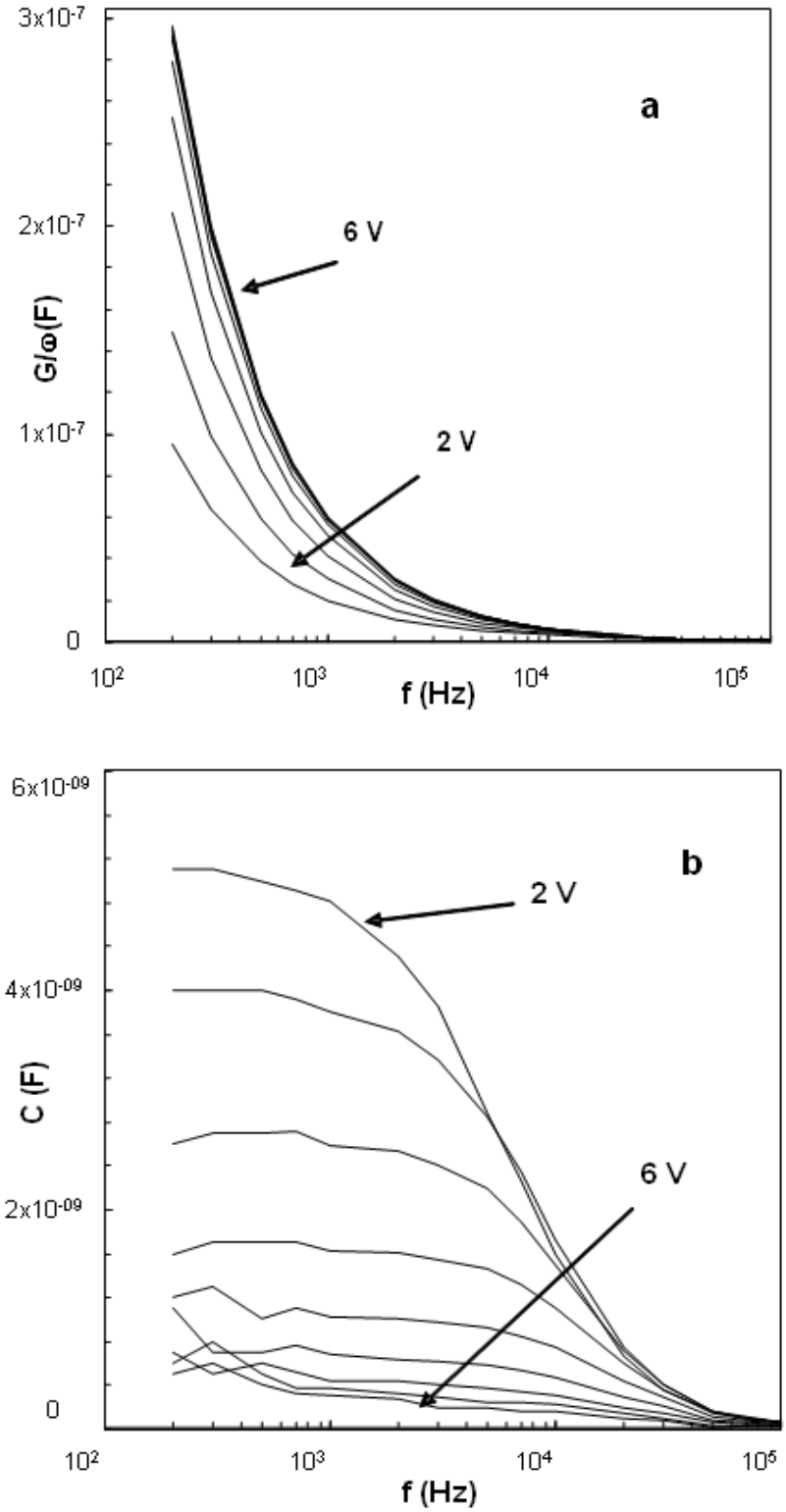

Figure 1. Experimental forward bias capacitance and conductance plots as a function of the frequency with bias voltage as a parameter of the Al/SiO_2/p-Si structure (2-6 V) with steps of 0.5 V at room temperature (Şekil 1. Oda sıcaklığında 0,5 V adımlı olarak (2-6 V arasında) Al/SiO_2/p-Si yapının voltaj ile frekansın bir fonksiyonu olarak deneyden elde edilen kapasitans ve iletkenlik eğrileri)

4.2. Conductance Method (İletkenlik Yöntemi)

According to this method, an applied ac signal on devices causes the Fermi energy level to oscillate about the mean positions governed by the dc bias, when the MIS diode is in the depletion. In Nicollian and Goetzberger's statically theory [1 and 2], in which random distribution of discrete insulator charges and charged N_{ss} in the Si/SiO_2 interface plane cause a nonuniform distribution of surface band bending over the interfacial plane. In addition, admittance spectroscopy can identify both bulk and interface defects when used on MIS diodes, and in particular, when the diodes are biased in depletion and superimposed ac signal is applied across the diode terminals [2]. Subsequent measurement of the parallel conductance as the frequency of the applied voltage for certain dc biases in depletion and suitable modeling provides the N_{ss}. At the same time the interface trap lifetime, referred also as relaxation time (τ), can be obtained. Therefore the equation describing the measured parallel conductance (G_p) as a function of frequency (ω) of the applied signal was that of the statistical model proposed by Nicollian and Brews [1 and 2] for the SiO_2/Si system:

$$\frac{G_p}{\omega} = \frac{qD_{it}}{2\omega\tau(2\pi\sigma)^{0.5}} x \int_{-\infty}^{\infty} \exp(-\varphi) x \ln[1+(\omega\tau)^2 \exp(2\varphi)] \exp[\frac{-\varphi^2}{2\sigma^2}] d\varphi_s$$

$$= (qAD_{it}/2\omega\tau_p) Ln(1+\omega^2\tau^2) \quad (1)$$

where q is the electronic charge, σ is a parameter dependent on the statistical behaviour of the system and φ is the surface potential at various energy levels and is given as:

$$\tau_p = (v_{th}\sigma_p N_A \exp(-\varphi_s))^{-1} \quad (2)$$

where v_{th} is the thermal velocity of carriers (= 10^7 cm/s) and φ_s is the normalised surface potential ($\varphi_s = q\bar{\varphi}_s/kT$) at a bias voltage V, σ_p is the capture cross sections and N_A is the doping density of the substance. The source of the G_p is due to the simple level states, or a continuum of states or a continuum of states under the influence of statistical fluctuations of the surface potential [1].

Figure 2, depicts the G_p/ω vs. lnf for different depletion bias show a maximum and with increasing bias, the peak amplitude, $(G_p/\omega)_{max}$ decreases and the frequency (ω_p) at which the maxima occur moves towards lower value. This behaviour can be explained by using the interface trap model. As indicated before, there exists an almost continuous distribution of N_{ss} energy levels. At a given bias, the Fermi level fixes the occupancy of these trap levels and a particular hole density will be at oxide/strained-Si interface which determines the capture rate of the related trap levels. Capture and emission occurs primarily by traps located within a few kT/q above and below the Fermi level. If the frequency is slightly different from the capture rate, losses are reduced because trap levels either do not respond or the response occurs at a different frequency. Therefore, the loss peak is a function of frequency. Furthermore, the peak value depends on capture rate, i.e., on the interface trap level occupancy, which is determined by the applied gate bias [15 and 17].

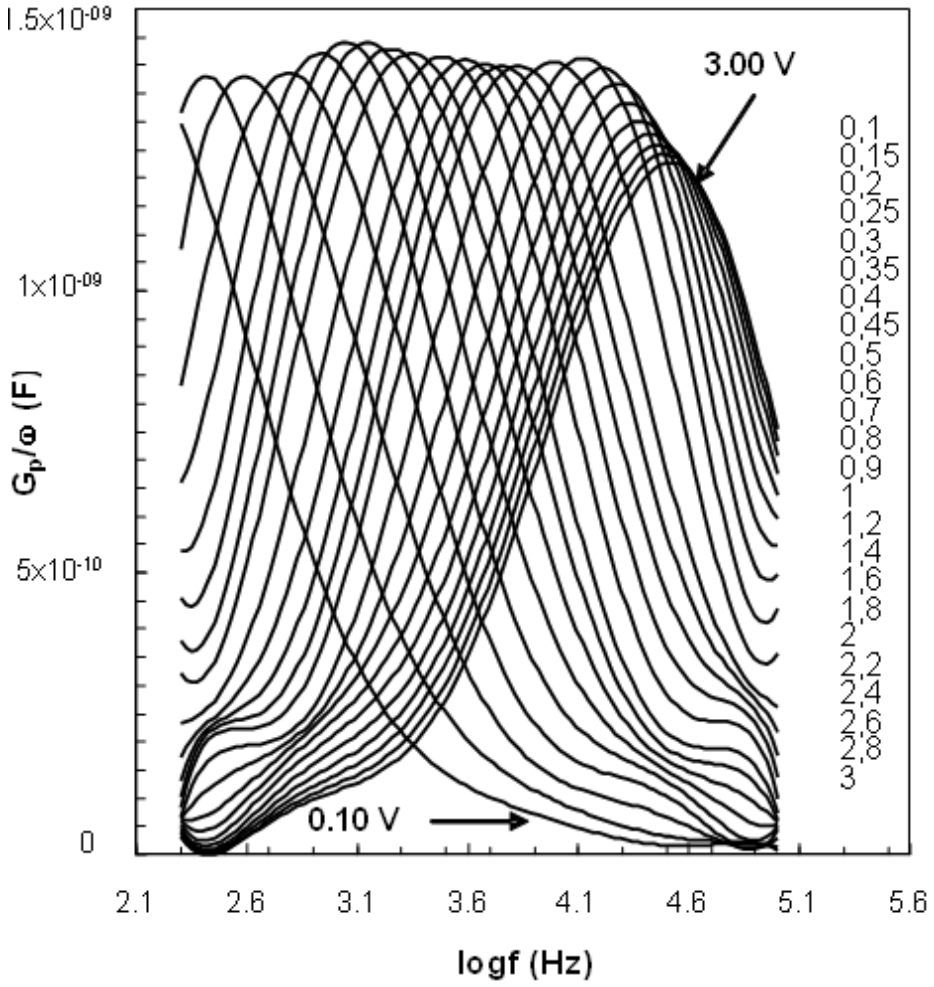

Figure 2. The equivalent parallel conductance (Gp/ω) vs. frequency at various gate biases for the Al/SiO_2/p-Si structure for various frequencies at room temperature
(Şekil 2. Oda sıcaklığında değişik frekanslarda Al/SiO2/p-Si yapı için değişik gerilimlerde eşdeğer paralel iletkenlik (Gp/ω)-frekans eğrileri)

The energy position in the p-Si band gap is calculated by

$$E_{ss}-E_v = q(\varphi_s+\phi_F) \quad (3)$$

where ϕ_F is the position of the Fermi level energy.

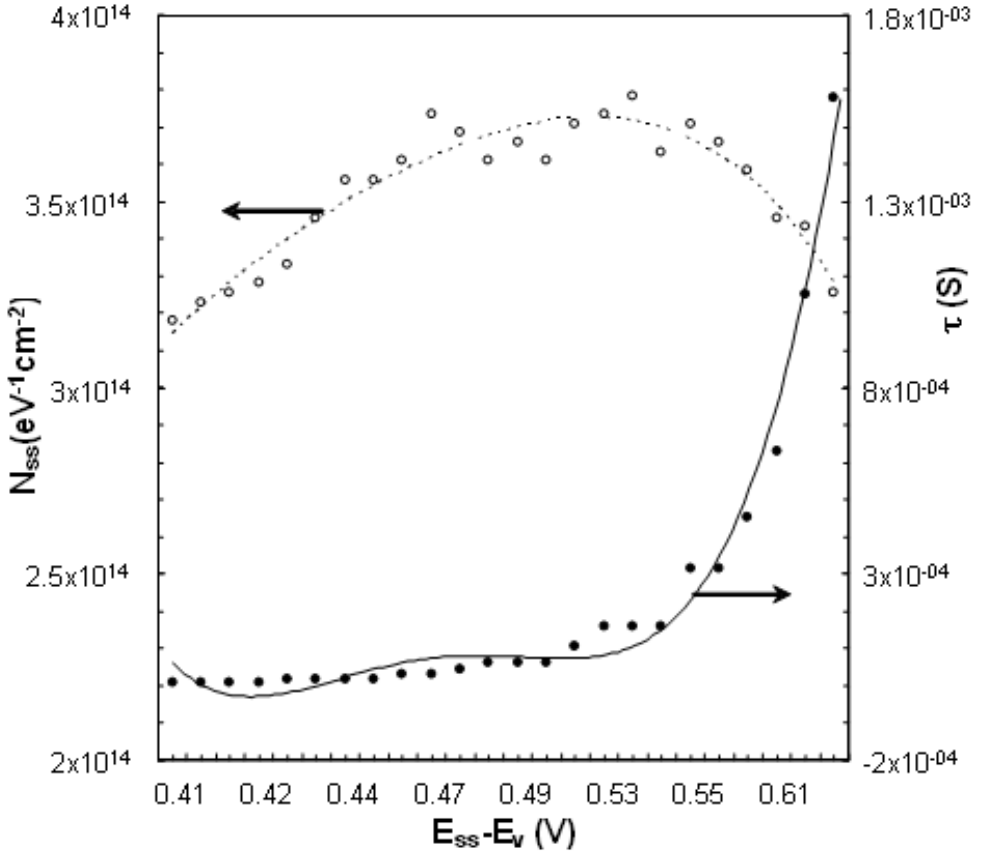

Figure 3. The energy distribution of interface states and their relaxation time obtained from conductance method for the Al/SiO_2/p-Si structure at various frequencies at room temperature
(Şekil 3. Oda sıcaklığında ve değişik frekanslarda Al/SiO_2/p-Si yapısı için iletkenlik yönteminden elde edilen Ara yüzey durumları ve onların gevşeme zamanı sabitinin enerji dağılımı)

The main value of N_{ss} was found about $3x10^{14}$ $eV^{-1}cm^{-2}$ and slightly changes. As can be seen in Figure 3, for each gate bias the G_p/ω vs. frequency curve show a peak and peak due to the interface state contribution shifts from low frequency to high as the bias changes from depletion toward the accumulation region as predict by the theory. For the peak value (Figure 2), $d(G_p/\omega)/d(\omega\tau)=0$ and this maximum condition gives $\omega\tau = 1.98$. Substituting this value in the above Eq. 1 one gets $N_{ss} = (G_p/\omega)_{max.}/(0.402qA)$ and interface state relaxation time $\tau=1.98/\omega_p$. It is observed that both N_{ss} and τ show increases with increasing energy and from the bottom the valance band toward the mid-gap of Si.

The energy distribution of surface states (N_{ss}) and them relaxation time (τ) have been determined in the energy range of (0.408)-(0.671) eV taking into account the surface potential as a function of applied bias obtained from the lowest measurable frequency C-V curve. The N_{ss} ranges from $3.18x10^{14}$ $eV^{-1}cm^{-2}$ to $3.25x10^{14}$ $eV^{-1}cm^{-2}$. Furthermore, the τ ranges from $1.05x10^{-5}$ s to $1.58x10^{-3}$ s and shows an exponential rise with bias from the top of the valance bend towards the mid-gap. Thus, it is seen that the both N_{ss} and τ is bias-

dependent. Such behavior of N_{ss} and τ were also observed in the literature in recent years [17].

Table 1. The experimental parameters obtained of the $Al/SiO_2/p$-Si structure at various frequencies at room temperature
(Tablo 1. Oda sıcaklığında ve değişik frekanslarda $Al/SiO_2/p$-Si yapının deneysel parametrelerinden elde edilenler)

V (V)	E_{ss}-Ev(V)	$N_{ss}(eV^{-1}.cm^{-2})$	τ (s)
0.10	0.671	$3.25x10^{14}$	$1.58x10^{-03}$
0.15	0.639	$3.43x10^{14}$	$1.05x10^{-03}$
0.20	0.609	$3.46x10^{14}$	$6.31x10^{-04}$
0.25	0.586	$3.58x10^{14}$	$4.50x10^{-04}$
0.30	0.569	$3.66x10^{14}$	$3.15x10^{-04}$
0.35	0.555	$3.71x10^{14}$	$3.15x10^{-04}$
0.40	0.544	$3.63x10^{14}$	$1.58x10^{-04}$
0.45	0.534	$3.78x10^{14}$	$1.58x10^{-04}$
0.50	0.526	$3.73x10^{14}$	$1.58x10^{-04}$
0.60	0.513	$3.71x10^{14}$	$1.05x10^{-04}$
0.70	0.502	$3.61x10^{14}$	$6.31x10^{-05}$
0.80	0.492	$3.66x10^{14}$	$6.31x10^{-05}$
0.90	0.484	$3.61x10^{14}$	$6.31x10^{-05}$
1.00	0.477	$3.68x10^{14}$	$4.50x10^{-05}$
1.20	0.466	$3.73x10^{14}$	$3.15x10^{-05}$
1.40	0.457	$3.61x10^{14}$	$3.15x10^{-05}$
1.60	0.449	$3.56x10^{14}$	$1.58x10^{-05}$
1.80	0.442	$3.56x10^{14}$	$1.58x10^{-05}$
2.00	0.436	$3.46x10^{14}$	$1.58x10^{-05}$
2.20	0.430	$3.33x10^{14}$	$1.58x10^{-05}$
2.40	0.424	$3.28x10^{14}$	$1.05x10^{-05}$
2.60	0.418	$3.25x10^{14}$	$1.05x10^{-05}$
2.80	0.413	$3.23x10^{14}$	$1.05x10^{-05}$
3.00	0.408	$3.18x10^{14}$	$1.05x10^{-05}$

5. CONCLUSIONS (SONUÇLAR)

The energy distribution profile of N_{ss} and τ have been obtained from frequency dependent C-V and G/ω-V characteristics. Experimental values of the C and G/ω show large frequency dispersion. This dispersion is result of the presence an interfacial insulator layer at MS interface and N_{ss} located semiconductor/insulator layer interface. The energy distributions of the N_{ss} and τ have been determined in the energy range of $(0.41-E_v)-(0.67-E_v)$ eV taking into account the surface potential as a function of applied bias obtained from the lowest measurable frequency C-V curve. The N_{ss} ranges from $3.18x10^{14}$ $eV^{-1}cm^{-2}$ to $3.25x10^{14}$ $eV^{-1}cm^{-2}$. Furthermore, the τ ranges from $1.05x10^{-5}$ s to $1.58x10^{-3}$ s and shows an exponential rise with bias from the top of the valance bend towards the mid-gap. In summary, there are two points can be noted. First, N_{ss} and τ show increases with increasing energy and from the bottom the valance band toward the mid-gap of Si. Second, especially at low frequencies all C-V and G/ω-V curves of diode show a dependence of R_s and therefore the measured capacitance C_m and conductance G_m were corrected for R_s.

ACKNOWLEDGEMENTS (EK BİLGİ)

This study was presented at The Condensed Matter Physics Conference of Balkan Countries, 26-28 May 2008, University of Mugla, TURKEY (CMPC BC2008).

REFERENCES (KAYNAKLAR)

1. Nicollian, E.H. and Goetzberger, A., (1965). MOS conductance Technique for measuring surface state parameters. Appl. Phys.Lett., vol. 7, pp:216–216.
2. Nicollian, E.H. and Brews, J.R., (1982). MOS Physics and Technology. John Wiley & Sons., New York
3. Kar, S. and Dahlke, W.E., (1972). Interface States in MOS Structures with 20-40Å Thick SiO_2 Films on Nondegenerate Si. Solid State Electronics, Vol. 15, pp:221.
4. Kar, S. and Narasimhan, R.L., (1987). Characteristics of the Si-SiO_2 interface states in thin (70–230 Å) oxide structures. J. Appl. Phys. 61(12), pp:5353–5359
5. Depas, M., Van Meirhaeghe, R.L., Lafere, W.H., and Cardon, F., (1994). Electrical characteristics of AllSiOz /n-Si tunnel diodes with an Oxide layer growth by rapid thermal oxidation. Solid-State Electronics 37(3), p:433.
6. Goetzberger, A., Klausman, E., and Schulz, M.J., (1979). Interface states on semiconductorlinsulator surfaces. CRC Git. Rev. SolidState Sci., vol. 6, pp:1-43.
7. Hung, K.K. and Cheng, Y.C. (1987). Characterization of Si–SiO_2 Interface traps in p-metal-oxide-semiconductor structures with thin oxides by conductance technique. J. Appl. Phys. 62 (10) (1987), pp:4204–4211
8. Tataroğlu, A., Altındal, Ş., Karadeniz, S., and Tuğluoğlu, N. (2003). Au/SnO2/n-Si (MOS) structures response to radiation and frequency. Microelectronic Journal. 34(11), pp:1043–1049.
9. Castagne, R. and Vapaille, A., (1971). Description of the SiO2-Si Interface Properties by Means of Very Low Frequency MOS Capacitance Measurements, Surf. Sci., Vol. 28, p:157.
10. Kelberlau, U. and Kassing, R., (1979), Theory of nonequilibrium properties of MIS capacitors including charge exchange of interface states with both bands. Solid-State Electron. 22 (1), pp:37–45.
11. Kuhn, M., (1970). A quasi-static technique for MOS C–V and surface State measurements. Solid-State Electron. 13 (6), 873–885.Solid State Electron., 13(6), p:873.
12. Kar, S. and Varma, S., (1985). Determination of silicon–silicon dioxide interface state properties from admittance measurements under illumination. J. Appl. Phys. 58 (11), pp:4256–4266.
13. Yücedağ, İ., Altındal, Ş., and Tataroğlu, A., (2007). On the profile of frequency dependent series resistance and dielectric constant in MIS structure. Microelectronic Engineering, 84(1), pp:180-186.
14. Szatkowski, J. and Sieranski, K., (1992). Simple interface-layer Model for the nonideal characteristics of the Schottky-Barrier diode Solid-State Electron., 35, pp:1013-1015.
15. Evangelou, E.K. Konofaos, N., Craven, M.R., Cranton, W.M., and Thomas, C.B., (2000). Characterisation of the $BaTiO_3$/p-Si interface and applications Appl. Surf. Sci., 166(1-4), pp:504-507.
16. Altındal, Ş., Kanbur, H., Yücedağ, İ., and Tataroğlu, A., (2008). On the energy distribution of interface states and their relaxation time and capture cross section profiles in Al/SiO2/p-Si (MIS) Schottky diodes. Microelectronic Engineering., 85(7), pp:1495-1501
17. Werner, J., Ploog, K., and Queisser, H.J., (1986). Interface-State Measurements at Schottky Contacts: A New Admittance Technique. Phys. Rew. Lett., 57, pp:1080-1083.