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# A LOW POWER REAL TIME IZHIKEVICH NEURON WITH SYNCHRONOUS NETWORK BEHAVIOR

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**ABSTRACT**

This paper presents a low power, compact VLSI implementation of a silicon neuron based on Izhikevich neuron model and synchronous network behavior of three coupled neurons, operating at biological timescale. The neuron circuit consists of two first order log domain filters, each corresponding to a variable of the neuron model, a positive feedback and resetting circuitry. The filters and as well as the other parts of the design involve source shifted transistors and active diode connections in order to operate at very low current levels yielding low power consumption and large time constants realized with small capacitances. The resetting circuitry contains cascaded simple differential pairs serving as comparators. The inphase and n-phase synchronization behaviors as a possible network dynamics of three coupled neurons are also presented. The coupling is provided by a synapse circuit which is again a first order log domain filter with sigmoid steady state and time constant functions. These sigmoid functions are obtained by using a simple differential pair and translinear loop current multipliers. The log domain design and current-mode operation in a 0.15 μm CMOS process results in low area and sub nano watt power consumption during real time scale operation which makes the circuit suitable for hybrid interface applications or large scale VLSI neuromorphic networks as a hardware simulation tool for computational neuroscience.

***Keywords: VLSI Neuron, Bioinspired, Low Power, Neuromorphic, Coupled Neurons.***

**ÖZET**

Bu çalışmada, Izhikevich sinir hücresi modelini esas alan düşük güçlü, kompakt ve gerçek zamanlı VLSI bir silikon sinir hücresi gerçeklemesi ile üç hücrenin kuplajından oluşan bir ağın senkron davranışı sunulmuştur. Sinir hücresi devresi, her biri bir değişkene karşılık gelen iki tane birinci derece logaritmik tanım bölgesi filtresinden, pozitif geribesleme ve resetleme alt devrelerinden oluşmaktadır. Filtreler ve diğer devre kısımları, düşük güç tüketimi sağlamak üzere düşük akım seviyelerinde çalışabilmek ve küçük kapasite değerleryle büyük zaman sabitleri elde edebilmek için, ötelenmiş kaynak gerilimli transistörler, aktif diyot bağları içermektedir. Resetleme alt devresi, karşılaştırıcı olarak kaskat bağlanmış basit fark kuvvetlendiricileri içermektedir. Muhtemel bir ağ dinamiği olarak, kuple edilmiş üç nöronun aynıfazlı ve n-fazlı senkronizasyon davranışları da sunulmuştur. Kuplaj, sigmoid sürekli hal ve zaman sabitine sahip bir birinci derece logaritmik tanım bölgesi filtresinden oluşan bir sinaps devresiyle sağlanmıştır. Bu sigmoid fonksiyonlar, basit bir fark kuvvetlendirici ve translinear çevrimli akım çarpıcılar kullanılarak elde edilmiştir. Logaritmik tanım bölgesinde 0.15 μm CMOS parametreli akım modlu bir tasarım, az yer kaplayan, nano watt altı güç tüketen ve gerçek zamanlı çalışan ve bu nedenle hibrit arayüz uygulamalarında ya da hesaplamalı sinir bilimde kullanılabilir büyük ölçekli tümdevre ağ tasarımlarında donanımsal benzetim gereci olarak kullanılabilecek bir tasarım ortaya çıkarmıştır.

***Anahtar Kelimeler: VLSI Nöron, Biyoesinlenilmiş, Düşük Güçlü, Nöromorfik, Kuplajlı Nöronlar.***

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## 1. INTRODUCTION

The computational power and efficiency of nervous systems of living organisms have been the source of motivation for engineers to design bioinspired circuits and real time large scale spiking neural networks recently [Serrano-Gotarredona et al., 2009; Vogelstein et al., 2007; Jin et al., 2010]. Such implementations, for instance, can be utilized both for large scale network simulations and hybrid interface systems. In the early works, the family of Integrate and Fire models (IF) were usually a popular choice as the neuron model due to their simple electronic realization [Mead, 1989] meanwhile the synaptic connections were modeled as instantaneous charge impulses [Bartolozzi et al., 2007]. However, it is argued that the performance of such implementations depends on the choice of the neuron model and synaptic connections and therefore spike based neuron models and synapses with temporal dynamics should be preferred for more realistic designs. In parallel with this scope, individual behavior of a single neuron should be dynamically rich as Hodgkin-Huxley (HH) model and computationally efficient as an Integrate and Fire (IF) neuron while the synaptic circuits should have temporal dynamics of their biological counterparts. For this purpose, low power and compact neurons and synaptic circuits have been designed recently. However, in some of the works, the neurons proposed have a fast time scale [Wijekoon et al., 2008; Schemmel et al., 2010] or poor dynamical behavior [; Wijekoon et al., 2009], firing patterns are unfair [Livi et al., 2009] or designs involve complexity [Yu et al., 2010]. Besides, the synaptic circuits offered usually suffer from nonlinearity and large chip area due to large capacitance values despite the advantage of less number of transistors [Bartolozzi et al., 2007].

A new neuron model with rich dynamics and computational efficiency has been proposed by Izhikevich [Izhikevich, 2003]. This model exhibits various firing patterns of cortical neurons by adjusting four parameters and is represented by two variables enabling a simple electronic design. Previous realizations of this model exist but the circuit in [Schaik et al., 2010] consumes much power and occupies much chip area. Similarly, in [Rangan et al., 2010], the circuit exhibits unsatisfactory firing patterns. On the other side, we have realized the same model successfully in [Demirkol et al., 2011] with low power and area consumption. In this work, we redraw the same circuit in 0.15 μm process rather than 0.35 μm, replace NOT gates with comparators that are composed of cascaded differential pairs, make a more accurate design and thus, come up with sub nano watt power consumption. Furthermore, we reduce the magnitude of the membrane variable $v$ to one tenth which lets us to use a smaller capacitance, related to the adaption variable equation, resulting in a smaller area occupation. Additionally, we couple three neurons via a biological chemical synapse that is adopted from [Pinto et al., 2000], involving sigmoid steady state and time constant functions. The synapse, by its nature, behaves linearly under repetitively input trains such as bursting. The coupling results also show that the neuron designed can successfully produce network dynamics.
We firstly introduce the neuron model in section II followed by circuit implementation in section III. The simulation results will be given in section IV and we conclude with section V.

## 2. THE NEURON AND THE SYNAPSE MODEL

The Izhikevich neuron model is described by two state equations and a pair of reset conditions as given below [Izhikevich, 2003]:

$$\dot{v} = 0.04v^2 + 5v + 140 - u + I_{in} \quad (1)$$

$$\dot{u} = a(bv - u) \quad (2)$$

$$if\ v \geq v_{peak}, v \leftarrow c, u \leftarrow u + d \quad (3)$$

where $v$ is the membrane potential, $u$ is the membrane recovery variable, $I_{in}$ is the external input current, $v_{peak}$ is the spike cutoff value, $a$ and $b$ are two parameters of the model where the remaining two parameters $c$ is the reset value of variable $v$ and $d$ is the increment amount of variable $u$ at reset time. A set of parameters that leads to a typical neuron behavior is, $a$ = 0.02, $b$ = 0.2, $v_{peak}$ = 30, $c$ = -65 and $d$ = 8. For these parameter values, regular spiking behavior is observed with an approximate period of 45 s where $v$ takes value between (-75, +30) and $u$ changes between (-8, 0). It should be noted that the parameters $a$ and $b$ are dimensionless and the rest of parameters have the same dimension with two variables.

To realize the model equations with log domain circuits, we need to express the variables in terms of currents that always take positive values. Therefore we shift the variables up and then, for low power consumption, scale the magnitudes such that the variables vary in pA range. We lastly adjust the time scale for real time operation and obtain the equation set as described below:

$$10\tau\dot{I}_v = 4I_v(I_v - 4.5pA)10^{12} + (21pA + I_{in} - I_u) \quad (4)$$

$$\tau\dot{I}_u = a(10bI_v - I_u) \quad (5)$$

$$if\ I_v \geq I_{peak}, I_v \leftarrow I_c, I_u \leftarrow I_u + I_{incr} \quad (6)$$

where $\tau$ stands for the time constant and equal to 1 ms, $I_{peak}$ is the spike cutoff value, $I_c$ is the reset value of $I_v$ and finally $I_{incr}$ is the amount of increment of $I_u$ at reset time. Note that the variables and parameters in (6) are currents in the pA range while $a$ and $b$ are still dimensionless. Here we note that we reduce the magnitude of the membrane variable $v$ to one tenth as different from other realizations [Schaik et al., 2010; Rangan et al., 2010; Demirkol et al., 2011].

To demonstrate that the neuron designed can present network dynamics, we couple three neurons via a biological chemical synapse model which is a modified form of the model in [Pinto et al., 2000] and also used for similar purposes in [Lee et al., 2007; Demirkol et al., submitted 2013]. The model is described by the equations given below:

$$I_{syn}(N_i, N_j) = g_{ij}S_i(E_{syn} - V_j) \quad (7)$$

$$\tau_S \frac{dS_i}{dt} = \frac{-S_i + S_\infty}{(1 - S_\infty)} \quad (8)$$

$$S_\infty(V_i) = 1/\left\{1 + \exp\left(\frac{(V_{1/2} - V_i)}{k}\right)\right\} \quad (9)$$

where $I_{syn}(N_i, N_j)$ is the synaptic current received by postsynaptic neuron $N_j$from presynaptic neuron $N_i$, $g_{ij}$ is the peak synaptic conductance, $S_i$ denotes the synaptic activity, $E_{syn}$ is the synaptic reversal potential, $S_\infty$ is the steady state activation function, $\tau_S$ is the time constant, $k$ is the synaptic slope factor and the parameter $V_{1/2}$ satisfies $S_\infty(V_{1/2}) = 0.5$. Here we determine the value of $g_{ij}$ such that the synaptic current $I_{syn}$ is less than %5 of the injected input current $I_{in}$ to provide a weakly coupling between the neurons.

We rewrite the synapse equations for a current mode operation with a similar approach above and obtain the equation set below:

$$I_{syn}(N_i, N_j) = \frac{I_{S_i}(I_{E_{syn}} - I_j)}{1pA/g_{ij}} \tag{10}$$

$$\tau_S \frac{I_{S_i}}{dt} = -I_{S_i}\frac{1}{(1-S_\infty)} + \frac{S_\infty}{(1-S_\infty)}10^{-12} \tag{11}$$

$$S_\infty(I_i) = 1/\left\{1 + \exp\left(\frac{(I_{1/2} - I_i)}{k}\right)\right\} \tag{12}$$

where $\tau_S$ stands for the time constant and equal to 1 ms, $I_{S_i}$ represents synaptic activity, $I_{E_{syn}}$ stands for synaptic reversal potential in terms of currents, and $g_{ij}$ and $S_\infty$ are dimensionless.

## 3. CIRCUIT IMPLEMENTATION

The basic building block of the neuron and synapse circuits is the first order log domain filter given in Figure 1. In this circuit, all the transistors operate in subthreshold region with an *i-v* relationship given by:

$$I_{DS} = I_s \frac{W}{L}\exp(\alpha V_{GS}) \tag{13}$$

where α is a parameter with an approximate value of 32. Using translinear principle, one can easily show that the state equation of this circuit in Figure 1 is,

$$C\dot{I}_{out} = -I_{out}(\alpha I_d) + I_{in}(\alpha I_b)(r_2 r_4 / r_1 r_3) \tag{14}$$

where $r_1$-$r_4$ are the aspect ratios of $M_1$-$M_4$ respectively. In our design, ground is the lowest level and $V_{DD}$ is the highest level of the supply voltage. For the circuit in Figure 1, the source voltages of $M_2$ and $M_4$ are shifted by an amount of $V_{sn}$ ($V_{sp}$ for PMOS transistors). We use source shifting technique during all the design for a proper DC behavior [Linares-Barranco et al., 2004]. A brief explanation of the technique exists in similar works [Demirkol et al., 2011; Demirkol et al., submitted 2013].

With a rearrangement of the equations (4) and (5), we obtain (15) and (16) in the form of (14) and can realize these equations utilizing the circuit in Figure 1.

$$C_v\dot{I}_v = -4I_v(4.5pA - I_v)10^{12}C_v/(10\tau) + (21pA + I_{in} - I_u)C_v/(10\tau) \tag{15}$$

$$C_u\dot{I}_u = -I_u(aC_u/\tau) + I_v(10abC_u/\tau) \tag{16}$$

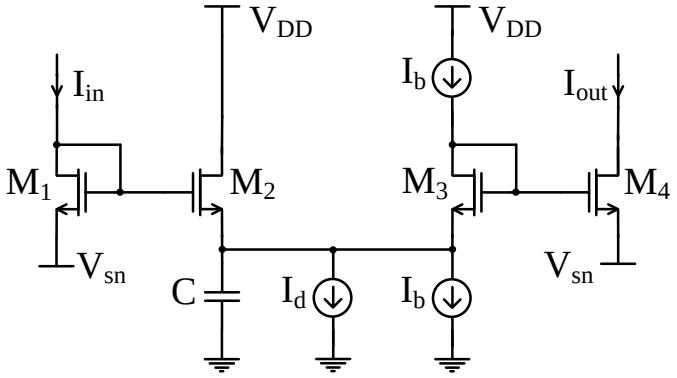


**Figure 1.** Log domain integrator.

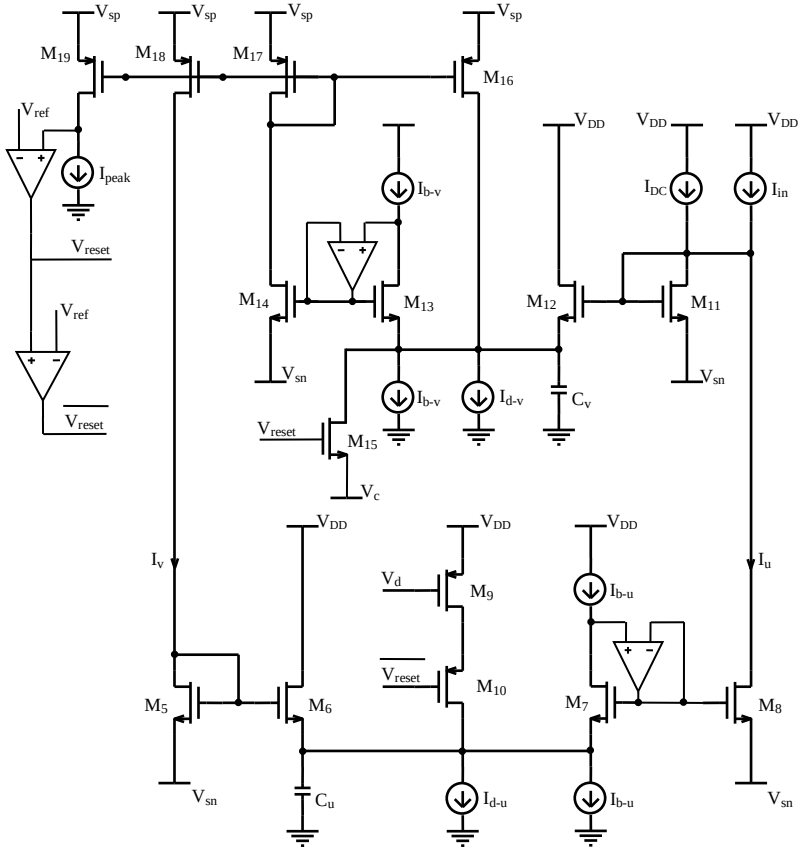


**Figure 2.** The overall neuron circuit.

The overall neuron circuit with additional reset circuitry is given in Figure 2. Different from [Demirkol et al., 2011], we use two active diode connections and two comparators, excluding not gates. When equation (14) is reconsidered, we see that the lower bound of the capacitance value is limited by the currents $I_b$ and $I_d$. Now it is clear that, scaling the magnitude of the membrane variable one to tenth introduces a coefficient of *10b* in (16) (instead of *b*) and enables us to lower the capacitance value in (16). In addition, the role of active diode connections is the same as explained in [Demirkol et al., 2011], performing similar AC and DC results [Demirkol et al., submitted 2013] even for lower current values thanks to the use of smaller size transistors. As a result, we determine the minimum current level as 100 fA and choose $C_v = 80fF$ and $C_u = 160fF$. The values of the DC currents are $I_{d-v} = 4.5pA$, $I_{b-v} = 250fA$, $I_{d-u} = a * 5pA$, $I_{b-u} = 10ab * 5pA$ and $I_{DC} = 21pA$. For typical values of the parameters $a$ and $b$, values of the bias currents are $I_{d-u} = 100fA$ and $I_{b-u} = 200fA$. The transistors $M_5$-$M_8$ realize the state equation in (16) related to $I_u$, while $M_{11}$-$M_{14}$ and $M_{16}$ realize the state equation in (9) related to $I_v$. The transistors $M_{10}$ and $M_{15}$ serve as a switch to reset the current $I_v$ to $I_c$ and $I_u$ to $I_u$+$I_{incr}$. The values of the currents $I_c$ and $I_{inc}$ are made adjustable through the voltages $V_c$ via $M_{15}$ and $V_d$ via $M_9$, respectively. Transistors $M_{17}$-$M_{19}$ compose multiple output current mirror generating replicas of the current $I_v$. The comparator producing $V_{reset}$ signal is composed of three cascaded differential pairs and the comparator generating $\overline{V_{reset}}$ is single differential pair. The diode connections of $M_7$ and $M_{13}$ are also supplied by simple differential pairs with 10 pA bias current and unbalanced input transistors in order to create an offset voltage between drain and gate nodes for improved DC behavior.

We next realize the equations (10-12) to create the synapse circuit. We realize (10) utilizing a transliear current multiplier circuit and realize (11) utilizing the log domain filter. To realize (12), we need a sigmoid function generating circuit accepting the spike signal as the input. Since the spike signal is a pulse like signal, we prefer to use the $V_{reset}$ voltage signal instead of the current spike signal in order to generate the sigmoid function easily utilizing a simple differential pair. The complete synapse circuit is given in Figure 3.

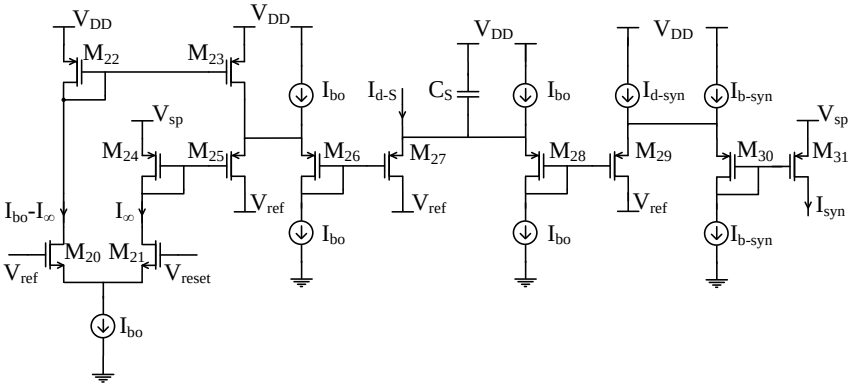


**Figure 3.** The synapse circuit.

The transistors $M_{20}$ and $M_{21}$ with $I_{bo}$ current source form the differential pair the branch current of which is given by (17) matching (12).

$$I_{\infty} = \frac{I_{bo}}{1+\exp(\alpha(V_{reset}-V_{ref}))} \quad (17)$$

To realize (12), we combine a translinear current multiplier loop composed of $M_{24}$-$M_{27}$ and a log domain filter composed of $M_{26}$-$M_{29}$. Here $I_{d\text{-}S}$ is equal to $\frac{{I_{bo}}^2}{(I_{bo}-I_{\infty})}$ generated by a translinear current multiplier loop not shown in Figure 3 for simplicity. The output of log domain filter is also combined with a second translinear current multiplier loop composed of $M_{28}$-$M_{31}$ in order to realize (10). Here $I_{d\text{-}syn}$ is equal to $1pA/g_{ij}$ and $I_{b\text{-}syn}$ is equal to $(I_{E_{syn}} - I_j)$. We also want to note that the synaptic activity current $I_S$ does not appear directly but appear indirectly as a voltage signal at the gate of $M_{28}$.

## 4. SIMULATION RESULTS

We simulated the neuron and the synapse circuit using 0.15 μm CMOS process parameters with Spectre simulator in Cadence design tool. Supply voltage is $V_{DD} = 1.5\,V$, $V_{ref} = V_{DD}/2$ and amonut of source shifting is 300 mV. All the transistors have $W/L = 450\,nm/450\,nm$. Differential pairs constituting the active diode connections and comparators are built with minimum size transistors. The tuning range of $V_c$ and $V_d$ are (355, 367) mV and (1.22, 1.35) V respectively. The estimated chip area for the neuron circuit is 275 $\mu m^2$ and for the synapse circuit is 130 $\mu m^2$. At resting state, i.e. zero input state, $I_v$ = 1.58 pA, $I_u$ = 3.36 pA and the current and power consumption of the circuit is 166 pA and 249 pW, respectively. While the circuit is in regular spiking regime with a period of 45ms, the circuit only consumes 270pW. Different from [Demirkol et al., 2011], such low power consumption is achieved by excluding NOT gates.

Figure 4 shows different type of firing patterns reproduced from the circuit. The input is a step current except in Figure 4(f) where it is a ramp current. Figures 4 (a-e) are reproduced according to parameter set in [Izhikevich, 2003]. Since $b > 0$ in this design, the neuron circuit behaves as a resonator rather than an integrator. Therefore, we expect to see a *Class II* behavior as depicted in Figure 6(f). Here, the neuron starts to fire at a non-zero frequency and the frequency of spiking changes slightly with increasing input current. Meanwhile, the neuron can be modified to behave as an integrator by simply shifting the *u* variable up and subtracting *v* variable from the drain node of $M_5$ instead of adding in Figure 2, which corresponds to $b < 0$ behavior. Thus, a *Class I* behavior is obtained under a ramp input current as depicted in Figure 5. All the results, when compared with numerical simulation results in [Izhikevich, 2003], show the success of the design.

The synaptic output currents for inputs of regular spiking and bursting are given in Figure 6. We adjust the peak of the synaptic current to 0.5 pA in order to obtain a weakly coupling between neurons. When the input spikes arrive to the synapse

frequently such as a bursting pattern, the synapse integrates the inputs linearly according to (7-9) and the peak of the output current increases as depicted in Figure 6 (b).

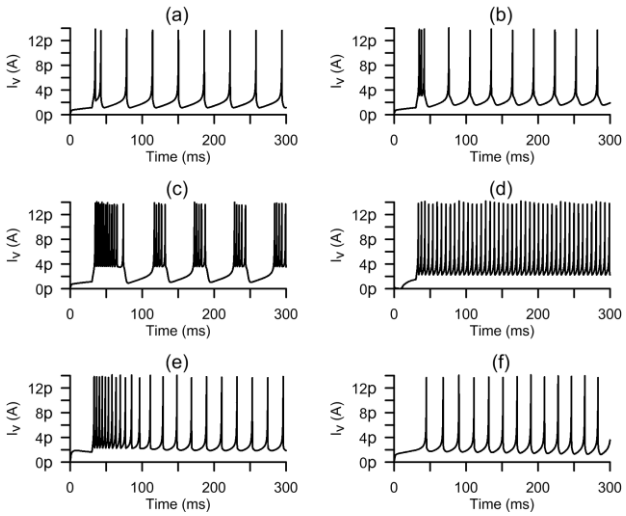


**Figure 4.** Firing patterns. (a) Regular Spiking, (b) Intrinsically Bursting, (c) Bursting, (d) Fast Spiking, (e) Low Threshold Spiking (Spike Frequency Adaption), (f) Class II Behavior.

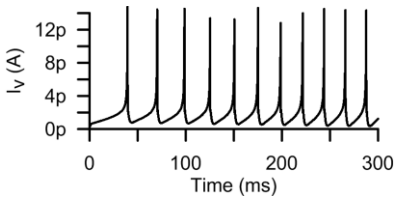


**Figure 5.** Class I behavior.

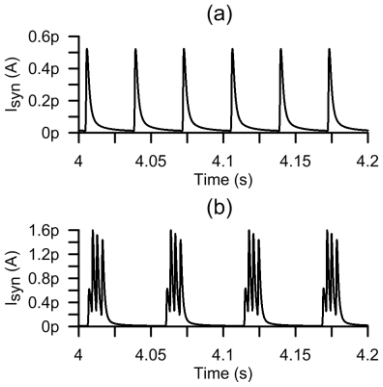


**Figure 6.** Synaptic currents for inputs of (a) regular spiking and (b) bursting.

Table 1. Comparison between the proposed work and literature.

| | Area | Power | Time Scale | Patterns |
|---|---|---|---|---|
| [Livi et al., 2009] | 913 $\mu m^2$ | 2.67 nW | real | fair |
| [Wijekoon et al., 2009] | 4900 $\mu m^2$ | - | real | poor |
| [Schaik et al., 2010] | 20.000 $\mu m^2$ | 20 µW | real | good |
| [Rangan et al., 2010] | 2980 $\mu m^2$ | 7 nW | x10 | not fair |
| [Schemmel et al., 2010] | - | 100 µW | $x10^5$ | good |
| [Yu et al., 2010] (estimated) | 0.4 $mm^2$ | 50 µW | x10 | good |
| [Demirkol et al., submitted 2013] | 490 $\mu m^2$ | 9.3 nW | real | very good |
| This work | 275 $\mu m^2$ | 270 pW | real | very good |

A comparison of some silicon neurons from the literature with the proposed work is given in Table 1. It can be concluded from Table 1 that, the designed neuron is both very compact and a low power consuming circuit.

In order to show that the neuron designed can exhibit network dynamics, we couple three neurons (n=3) according to the network coupling diagram given in Figure 7. We investigate the network dynamics for both regular spiking and bursting behavior. Moreover we create both excitatory and inhibitory coupling and expect to see inphase synchronization, i.e. zero phase difference, for excitatory coupling and n-phase synchronization, i.e. 120 degrees of phase difference, for inhibitory coupling. Firstly, we make the neurons oscillate independently with initial phase differences and activate coupling after the first second of the simulation. After a sufficient time, we observe the proper type of synchronization. Additionally, we consider the worst case to determine the initial phases. For instance, if we expect n-phase synchronization, we set almost no initial phase difference between neurons and vice versa.

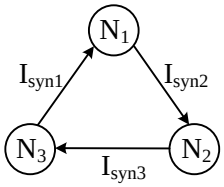


**Figure 7.** Network coupling diagram.

Simulation results of the network dynamics is given in Figure 8-11. Figure 8 presents excitatory coupling and Figure 9 presents inhibitory coupling for regular spiking

behavior. Similarly, Figure 10 and Figure 11 presents excitatory and inhibitory coupling for bursting behavior, respectively. Left column of the Figures 8-11 are initial states of the neurons while the right columns are representing the final synchronized states. As a result, all the expected synchronization behaviors both for regular spiking and bursting neurons are obtained successfully.

In [Lee et al., 2007], in phase and n-phase behavior is investigated for two bursting neurons. However, the initial states of the neurons are not set properly and the results do not match with numerical simulations results depicted in the same work. In [Yu et al., 2010], only inphase behavior of two regular spiking neurons are presented but no any synaptic equations or circuits are presented in that work. Therefore, the network dynamics exhibited in this work, which agree with expectations, make the neuron and synaptic circuit a good candidate to build larger networks.

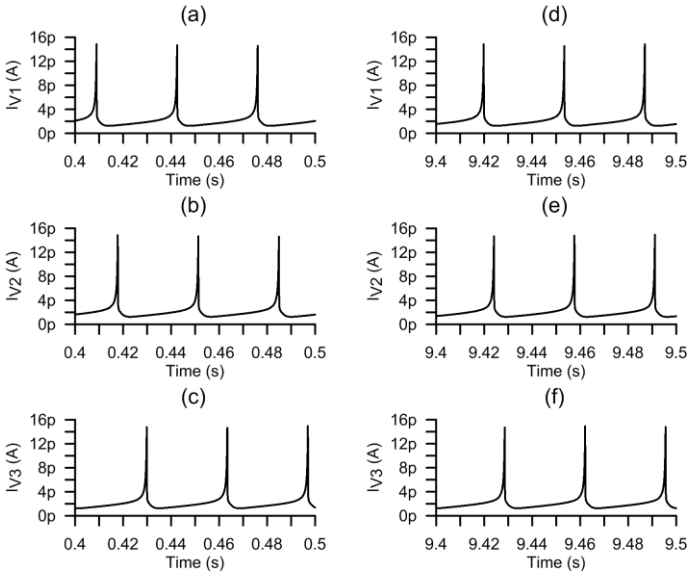


**Figure 8.** Excitatory coupling results for regular spiking. (a) initial state of neuron 1, (b) initial state of neuron 2, (c) initial state of neuron 3, (d) final state of neuron 1, (e) final state of neuron 2, (f) final state of neuron 3.

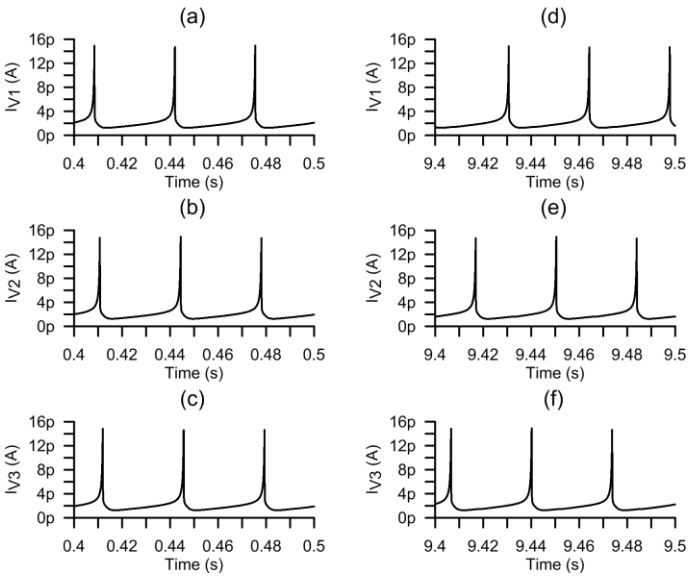


**Figure 9.** Inhibitory coupling results for regular spiking. (a) initial state of neuron 1, (b) initial state of neuron 2, (c) initial state of neuron 3, (d) final state of neuron 1, (e) final state of neuron 2, (f) final state of neuron 3.

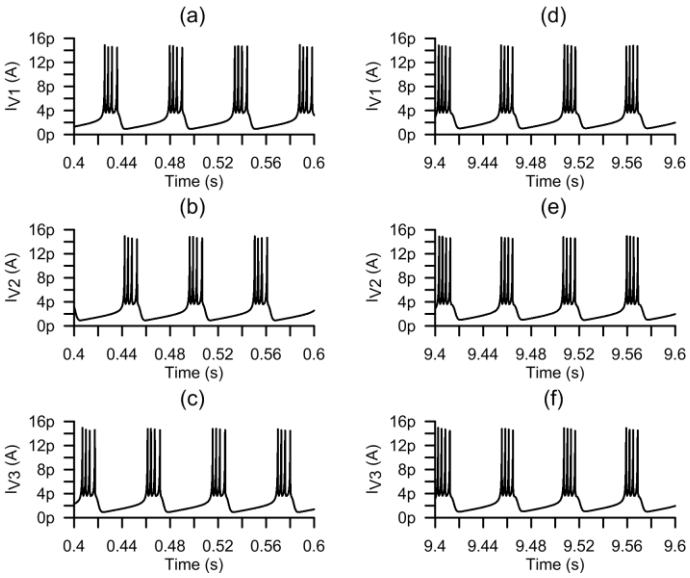


**Figure 10.** Excitatory coupling results for bursting. (a) initial state of neuron 1, (b) initial state of neuron 2, (c) initial state of neuron 3, (d) final state of neuron 1, (e) final state of neuron 2, (f) final state of neuron 3.

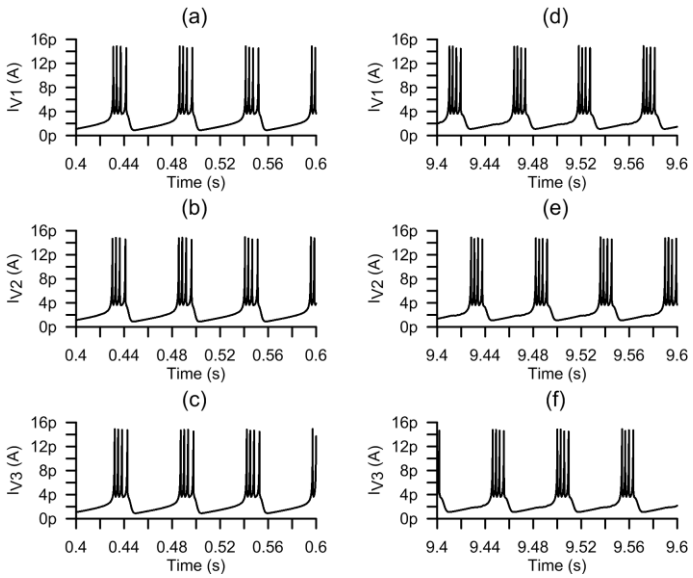


**Figure 11.** Inhibitory coupling results for bursting. (a) initial state of neuron 1, (b) initial state of neuron 2, (c) initial state of neuron 3, (d) final state of neuron 1, (e) final state of neuron 2, (f) final state of neuron 3.

## 5. CONCLUSION

In this work, we presented a low power, compact and real time VLSI implementation of the Izhikevich neuron model and typical firing patterns of a cortical neuron were observed successfully with additional *Class I* and *Class II* behavior. We also presented a simple compact but realistic synapse circuit in order to show that the neuron is capable of generating network dynamics. Inphase and n-phase synchronization patterns of three coupled neurons were observed successfully for excitatory and inhibitory coupling, respectively.

Low power and compact real time design makes the neuron circuit suitable for building human interface electronics systems. Since the neuron relies on a mathematical model, it is also possible to design large scale VLSI networks as a hardware simulation tool for computational neuroscience.

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