BALKAN JOURNAL OF ELECTRICAL & COMPUTER ENGINEERING, Vol. 10, No. 2, April 2022

A 0.6-V 11-μW PVT tolerant DTMOS inverter based OTA

Mesut Atasoyu

***Abstract*—This paper presents the design of a process-voltage-temperature (PVT) variation tolerant inverter-based operational transconductance amplifier (OTA) employing both a dynamic threshold MOS (DTMOS) technique and a constant voltage biasing (CVB) scheme. The proposed inverter-based OTA offers a higher bandwidth due to implemented DTMOS technique, which realizes higher input transconductance value than a conventional inverter-based OTA design. Simulation results show that the proposed OTA achieves superior slow-slow (SS) corner performance under PVT variations than the conventional inverter-based OTA while consuming only 11-muW and providing a figure of merit (FoM) of 7.0-MHz.pF/muA. As a result, DC gain and unity-gain bandwidth (UGBW) of the proposed OTA improve by 27$\%$ and 32$\%$ at SS corner under the PVT variations, respectively.**

***Index Terms*—DTMOS, inverter based OTA, PVT tolerant.**

I. Introduction

Mobile devices demand low-power analog to digital converter (ADC) techniques, and continuous-time (CT) circuit techniques are exploited due to low-power constraint rather than discrete-time [1, 2]. Continuous-time analog-to-digital converters (CT-ADCs) should have high linearity on a low supply voltage [1]. Integrators are the main block in CT-ADCs, and an operational transconductance amplifier (OTA) in integrators is a power-hungry unit. Inverter-based OTAs offer higher power efficiency than conventional OTA amplifiers due to their bias current reuse mechanism. Recently, low power capable inverter-based OTAs have been reported [1–4]. Inverter-based OTA functioning in the sub-threshold region (digital-like amplifier) [4] is to be used in the second and third integrators of CT-ADCs [1]. However, inverter-based OTAs are vulnerable to process, voltage, and temperature (PVT) variations, which degrade CT-ADC performance [3, 5]. On the other hand, sufficient DC gain of inverter-based OTA at lower supply voltage is remaining a problem [4, 6].

It is important to say that proper biasing of inverter-based OTAs is a difficult task under PVT variations. Previous PVT compensation techniques in [3], have mitigated PVT variations with auto RC tuning and constant g_m current source circuitry. In [6] using variable current sources at the output stage by controlling common-mode voltage. In [7], a low-dropout voltage regulator controls the supply voltage. In [8], the main inverter amplifier PVT compensation was realized by controlling the bulk voltage of the inverter gate amplifier.

MESUT ATASOYU is with Department of Electrical and Electronics Engineering at Ataturk University.
E-mail: mesutatasoyu@atauni.edu.tr
https://orcid.org/0000-0002-0029-7436
Manuscript received October 7, 2021; accepted Apr 14, 2022.
DOI: 10.17694/bajece.1005797

This work proposes the PVT tolerant inverter-based OTA using the constant biasing voltage (CVB) mechanism, composed of a current source with a diode-connected MOS device. On the other hand, in this bias method, the drain and source voltage (V_{DS}) of inverter gate transistors are clamped to a constant voltage. Furthermore, the unity-gain bandwidth (UGBW) of the proposed OTA is improved with the dynamic threshold MOS technique (DTMOS) [9], thus sub-threshold DTMOS provides additional g_{mb} improves the current drivability of the MOS device [10].

This paper is organized in the following manner. Section II explains the principle and circuit implementation of the PVT invariant inverter-based OTA. Section III reports the performance results of the inverter-based OTAs presented in detail. Section IV concludes final discussions on the proposed OTA design.

II. Circuit Implementation

The OTAs in this work are biased in the weak inversion region. The DTMOS technique is implemented in a triple-well process. An NMOS bulk is connected to a p-weel by adding a deep n-well layer in a triple-well process. In the conventional CMOS process, an NMOS transistor gate and bulk can not connect to each other due to short circuit concerns. However, the designing of a PMOS transistor is the same for these two processes. The DTMOS technique on the design of an inverter-based OTA increases the input transconductance of the OTA due to bulk transconductance value g_{mb}. Moreover, the DC-gain performance of inverter-based OTA is enhanced due to increased drain current drivability of the input transistors of the inverter-based OTA as the DTMOS technique modulates threshold voltages (V_{th}) of these transistors.

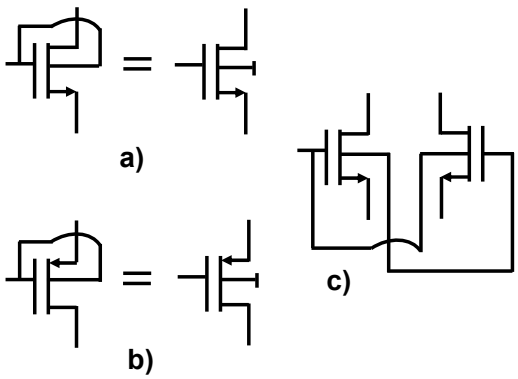

Fig. 1: The symbols of DTMOS transistors.

Fig. 1 shows the symbols of DTMOS transistors. Fig. 1a and Fig. 1b is the symbol of DTMOS NMOS, and DTMOS PMOS transistors, respectively. Fig. 1c is the cross-coupled DTMOS (CDTMOS) symbol for NMOS and PMOS transistors in the same way, but an NMOS CDTMOS symbol is shown in this figure. The DTMOS operated in subthreshold region can provide 16% more input transconductance [11] as given below equation:

$$g_{mb} = (n-1)^2 * g_m \tag{1}$$

where n is the subthreshold slope factor and taken as a value of $\approx$ 1.4 [11]. In this case, the input transconductance improves 32 % due to the input stage of the inverter-based OTA composed of an NMOS and PMOS transistor. In this work, the current starved inverter-based OTAs were simulated in 65nm CMOS technology, and their schemes were shown in Fig. 2 and Fig. 3. Fig. 2a shows the schematic of the conventional inverter-based OTA, two inverter gates combined of M_{2-5} transistors consist of the differential input and output stage, the biasing circuity is consists of $M_{0,1}$ and $M_{6,7}$ transistors, and the common-mode feedback (CMFB) circuity is consists of M_{8-10}. Fig. 3a shows the schematic of the proposed OTA, two inverter gates combined of M_{2-5} transistors consist of the differential input and output stage, the biasing circuity is consists of $M_{0,1}$ and $M_{6,7}$ transistors, and the common-mode feedback (CMFB) circuity is consists of $M_{8,9,10}$. The CVB biasing scheme is consists of M_{C1-C4}. Fig. 2b and in Fig. 3b illustrate the small-signal equivalent circuits of the inverter-based OTAs used for the differential gain calculations of the conventional and proposed inverter-based OTAs. The differential AC gain formulas was given in the below equations, assuming $g_m * r_o \gg 1$:

$$G_{M[conv]} = g_{m2} + g_{m4} \tag{2}$$

$$R_{O[conv]} = (g_{m2} * r_{o2} * 2r_{o1}) \,//\, (g_{m4} * r_{o4}) \tag{3}$$

$$G_{M[proposed]} = g_{m2} + g_{mb2} + g_{m4} + g_{mb4} \tag{4}$$

$$R_{O[proposed]} = (g_{m2} * r_{o2} * 2r_{o1}) \,//\, (g_{c1} * g_{m4} * r_{o1} * r_{o4})$$

$$A_{V,differential_{[conv,proposed]}} = -G_M * R_O \tag{5}$$

The following equations for UGBW calculations of the conventional inverter-based OTA and proposed OTA are:

$$UGBW_{[conv]} = (g_{m2} + g_{m4})/C_L \tag{6}$$

$$UGBW_{[proposed]} = (g_{m2} + g_{mb2} + g_{m4} + g_{mb4})/C_L \tag{7}$$

In the voltage transfer characteristic of an inverter gate, the switching threshold voltage (V_{sw}) is the value of a point where input and output voltage are equal. In the ideal case, the desired value of V_{sw} is (V_{DD}=0.6V)/2. At this value, the noise margin is maximized [12]. On the other hand, the value of V_{sw} at V_{DD}/2 may be degraded due to process variations. To ensure V_{sw} voltage stability, common-mode feedback (CMFB) structure adopted from [13] is necessary to control the output common-mode voltage value at (V_{DD}=0.6V)/2. Transistors of CMFB circuitry are $M_{9,10}$ transistors operated in the triode region, and M_8 transistor, driven by V_{CM} voltage source has a value of V_{DD}/2.

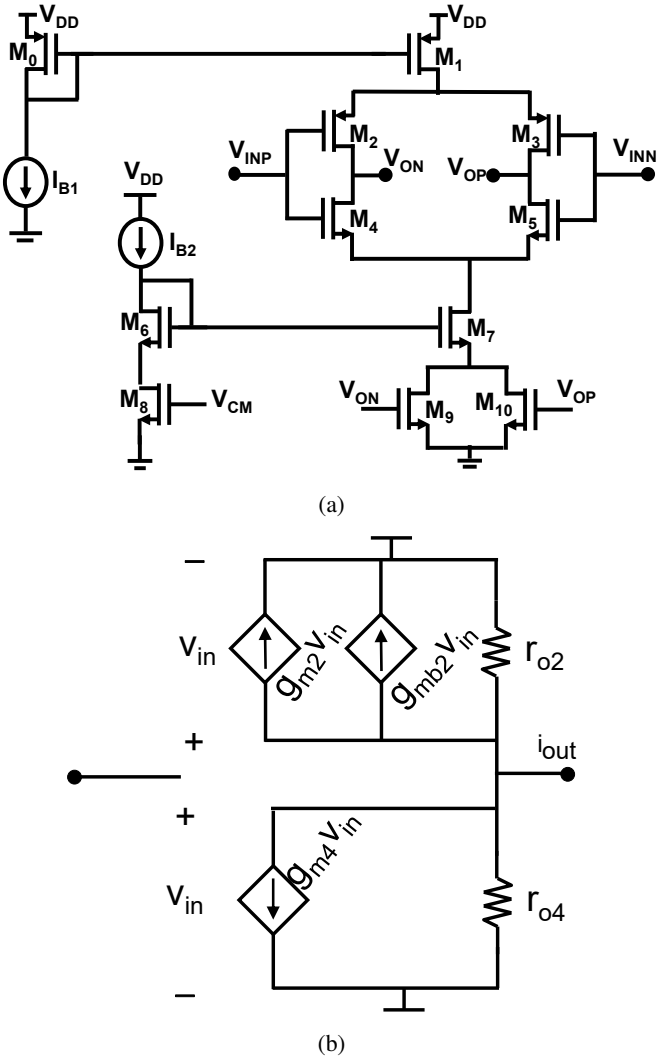

Fig. 2: (a)The schematic of the conventional inverter based OTA and (b)corresponding differential-mode small signal equivalent model of (a).

All transistor channel lengths are 1.33μm to provide sufficient intrinsic gain, except for M_{C3} device, which has a value of L=10μm. All gate widths of transistors were sized using g_m/ID methodology with drain current normalization coefficients (I_D^*) of 65nm PMOS and NMOS transistors where were taken from [14]. I_D^* was extracted experimentally in the 65-nm CMOS process for NMOS the value of 0.49-μA and PMOS the value of 0.15-μA [14]. The inversion coefficient (IC) is a transistor sizing parameter, experimental values of IC for NMOS and PMOS transistors in this work obtained from [14]:

$$IC = \frac{I_D}{I_D^* \frac{W}{L}} \tag{8}$$

where I_D is drain current, W is the gate width of a MOS transistor, and L is the channel length of a MOS transistor. IC levels for different operating regions of MOS transistors: IC $values < 0.1$ correspond to the sub-threshold region, values

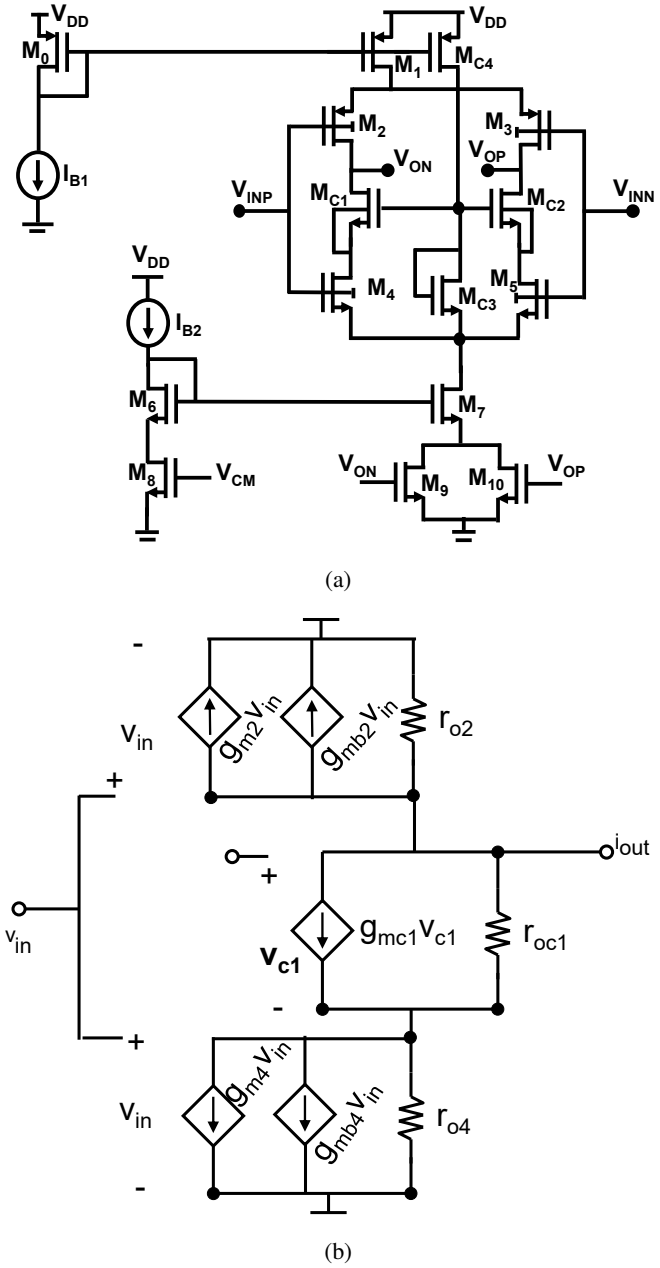

Fig. 3: (a)The schematic of the proposed inverter-based OTA and (b)corresponding differential-mode small-signal equivalent model of (a).

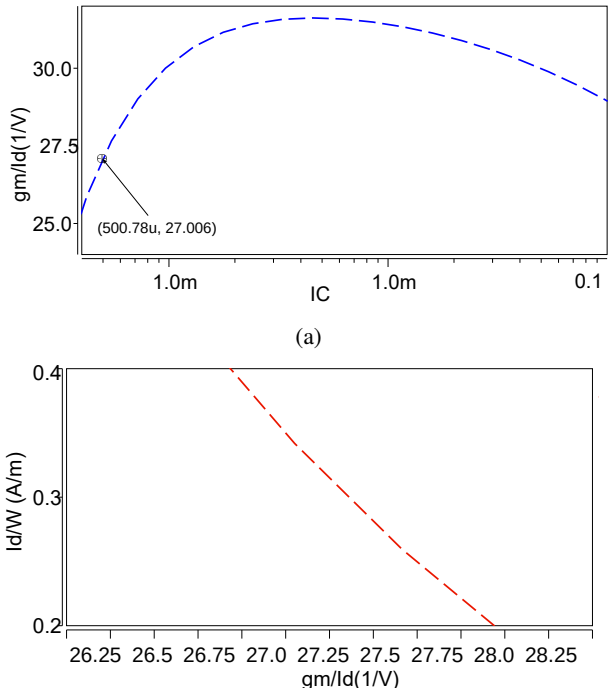

Fig. 4: The schematics of the inverter based OTAs.

of $0.1 <$ IC < 10 correspond to the linear region, IC $values > 10$ correspond to the saturation region. A transistor can operate in weak inversion, where IC values are less than 0.1. The IC value is 0.05 for the NMOS transistor sizing in this work. The corresponding value of an NMOS transistor current density (I_D/W) is 0.033 determined from Fig. 4. W value of an NMOS transistor calculates from the following equation:

$$W = \frac{I_{bias}}{I_D/W} \tag{9}$$

where I_{bias} is an applied biasing current. The CVB biasing scheme or the clamped V_{DS} biasing scheme is dedicated to the PVT compensation of the proposed OTA. The CVB scheme is composed of M_{C3} diode-connected MOS device sized with W=130nm and L=10μm, the current source transistor M_{C4} was sized with W=1μm, and $M_{C1,C2}$ voltage-clamp transistors are sized with W=27μm, as given in Table. I.

TABLE I: Transistor Sizes

Devices	(W(μm))
$M_{0,1}$	162
$M_{2,3}$	81
$M_{4,5}$	27
M_{6-10}	54
$M_{C1,C2}$	27
M_{C3}	0.13
M_{C4}	1

III. Simulation Results

The inverter-based OTAs were implemented in 65-nm CMOS technology. The simulated AC gain and the UGBW of conventional and proposed amplifiers are 35.9-dB and 5.82-MHz, 50.6-dB and 7-MHz, respectively. Regarding the phase margin (PM), the conventional and proposed OTAs are 90.0° and 85.7°, respectively, as given in Fig.5.

Figure 6 shows the transient analysis of the proposed OTA. The proposed OTA was designed with a capacitive feedback network, and the input signal was a square signal, which has a step of 600mV_{pp} and period of 1μS, for the transient simulations. As for the slew rate, the proposed OTA has better performance of the slew rate over the conventional OTA.

To verify the effectiveness of the proposed inverter-based OTA, the corner analysis in HSPICE was performed under

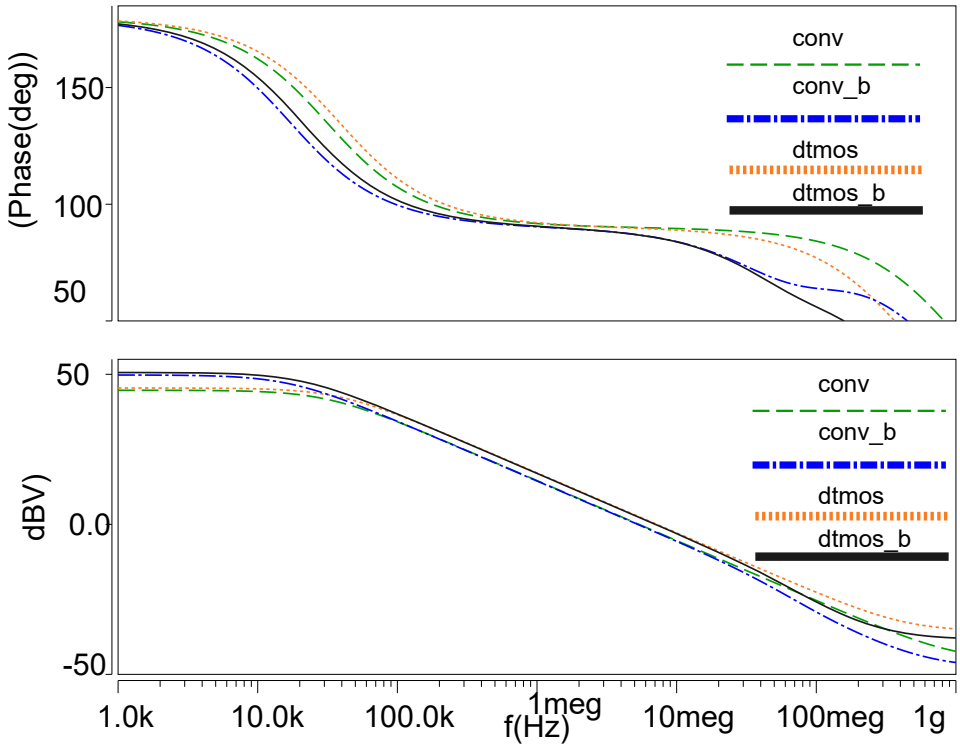

Fig. 5: AC response of the proposed inverter-based OTA. Both the inverter-based OTAs including CMFB circuits are biased with 10-μA current for 10-pF capacitive load under 0.6-V supply.

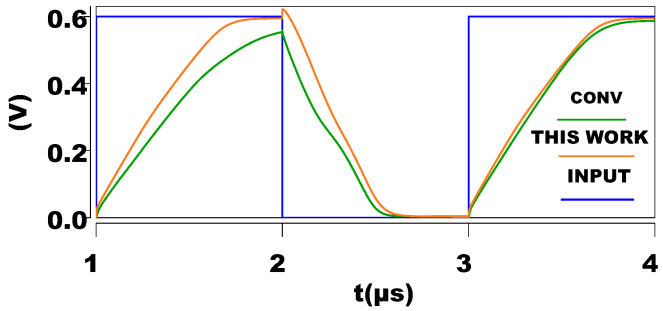

Fig. 6: Transient analysis of the proposed inverter-based OTA.

PVT variations setting up slow-slow (SS) corner for -40° and 0.54-V, typical-typical (TT) corner for 27° and 0.60-V, and fast-fast (FF) corner for 80° and 0.66-V [6]. On the other hand, especially in the SS process corner, an inverter-based OTA performance highly deteriorates. As a comparison of SS corner performance for the proposed OTA, the conventional OTA, the conventional OTA with CVB (Conv + CVB), the only DTMOS technique (DTMOS), the cross-coupled DTMOS (CDTMOS) with CVB (CDTMOS + CVB), and the Class-AB OTA [15] were performed. The proposed OTA has better AC gain and better UGBW performance in the SS corner, as shown in Table. II. The potential UGBW value which is highly dependent on PVT variation in an inverter based OTA design, [3]. As a result of the corner analysis under PVT variations, the gain degradation (from TT corner to SS corner) of the tested designs as follows: 34.6% for the Conv, 30.78% for the Conv+CVB, 6.6% for the DTMOS, 12.6% for the proposed (DTMOS+CVB), and 13.9% for the CDTMOS+CVB. The UGBW degradation of the tested designs as follows: 87.7% for the Conv, 87.16% for the Conv+CVB, 70.25% for the DTMOS, 70% for the proposed (DTMOS+CVB), and 70.36% for the CDTMOS+CVB. However, the proposed OTA has the worse performance at the FF corner, as obtained result in [3].

Table. III summarizes the simulation results and provides a comparison with state-of-the-art inverter-based OTAs. The widely used one of the figures of merit (FoM) has been calculated for the performance evaluation of OTAs in Table. III:

$$FoM = UGBW * C_L/I_{supply} \quad (10)$$

where I_{supply} is the total current consumption. The proposed OTA design achieves better FoM performance and as the FoM value of 7.0 MHz.pF/μA.

IV. Conclusion

In this paper, an improved PVT inverter-based OTA design was suggested. Compared to the conventional inverter-based OTA, the proposed circuit shows better AC gain, UGBW, and PVT tolerant design performances, thus having better FoM performance while consuming almost the same power budget. The proposed OTA operates in the sub-threshold region to enable low supply voltage circuit operation at the lowest 0.6V. The gain value of 50.6-dB, UGBW value of 7.0-MHz, and providing the FoM of 7.0 MHz.pF/μA. The proposed inverter-based OTA design is one of the promising solutions for low

TABLE II: The OTA performances across different process corners under PVT variations.

	Gain(dB),UGBW(MHz)		
	SS (0.54-V, -40°)	TT (0.6-V, 27°)	FF (0.66-V, 120°)
Conv	(34.6, 0.68)	(44.6, 5.3)	(35.9, 5.82)
Conv+CVB	(34.4, 0.67)	(49.7, 5.22)	(34.2, 5.52)
DTMOS	(42.4, 2.13)	(45.4, 7.16)	(31.2, 6.59)
The proposed (DTMOS+CVB)	(44.2, 2.09)	(50.6, 7.0)	(28.9, 6.10)
CDTMOS+CVB	(41.4, 1.55)	(48.1, 5.23)	(26.5, 4.65)
Class-AB OTA [15]	(37.96, 0.064)	(43.96, 0.112)	(43.55, 0.197)

TABLE III: Simulation performance results

Parameter	Conventional	([5])	Proposed	[15]	[16]	[17]	[18]
Power supply(V)	0.6	0.6	0.6	0.6	1.0	1.0	0.6
Technology(μm)	0.65	0.18	0.65	0.13	0.18	0.13	0.18
Power consumption(μW)	10	48.65	11	1.8	50	15	0.18
Load capacitance (pF)	10	8	10	6	140	50	20
DC gain (dB)	38.9	41.93	50.6	43.86	78.6	58.7	75.4
Unity-gain bandwidth (MHz)	2.7	15.55	7.0	0.112	2.02	10.43	0.074
Phase Margin(°)	90.0	88.06	85.7	88.8	85.4	78.8	78.86
Bias current(μA)	10	52	10	3.05	50	15	0.3
FoM ([17])	5.3	2.39	7.0	0.226	5.6	34.77	4.95

voltage and low power continuous-time ADC design in deep sub-micron CMOS technology.

ACKNOWLEDGEMENT

REFERENCES

[1] B. Gönen, S. Karmakar, R. van Veldhoven, and K. A. Makinwa, "A continuous-time zoom adc for low-power audio applications," *IEEE Journal of Solid-State Circuits*, vol. 55, no. 4, pp. 1023–1031, 2019.

[2] P. C. C. de Aguirre, E. Bonizzoni, F. Maloberti, and A. A. Susin, "A 170.7-db fom-dr 0.45/0.6-v inverter-based continuous-time σ-δ modulator," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 67, no. 8, pp. 1384–1388, 2019.

[3] Y. Guo, J. Jin, X. Liu, and J. Zhou, "An inverter-based continuous time sigma-delta adc with latency-free dac calibration," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 67, no. 11, pp. 3630–3642, 2020.

[4] L. Lv, X. Zhou, Z. Qiao, and Q. Li, "Inverter-based subthreshold amplifier techniques and their application in 0.3-v delta-sigma modulators," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 5, pp. 1436–1445, 2019.

[5] P. de Aguirre and A. Susin, "Pvt compensated inverter-based ota for low-voltage ct sigma-delta modulators," *Electronics Letters*, vol. 54, no. 22, pp. 1264–1266, 2018.

[6] A. Ismail and I. Mostafa, "A process-tolerant, low-voltage, inverter-based ota for continuous-time sigma-

delta adc," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 24, no. 9, pp. 2911–2917, 2016.

[7] L. Breems, M. Bolatkale, H. Brekelmans, S. Bajoria, J. Niehof, R. Rutten, B. Oude-Essink, F. Fritschij, J. Singh, and G. Lassche, "A 2.2 ghz continuous-time δ-σ adc with- 102 dbc thd and 25 mhz bandwidth," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 12, pp. 2906–2916, 2016.

[8] P. C. C. de Aguirre and A. A. Susin, "A 0.6-v, 74.2-db dr continuous-time sigma–delta modulator with inverter-based amplifiers," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 65, no. 10, pp. 1310–1314, 2018.

[9] F. Assaderaghi, D. Sinitsky, S. A. Parke, J. Bokor, P. K. Ko, and C. Hu, "Dynamic threshold-voltage mosfet (dtmos) for ultra-low voltage vlsi," *IEEE Transactions on Electron Devices*, vol. 44, no. 3, pp. 414–422, 1997.

[10] M.-E. Hwang and K. Roy, "A 135mv 0.13 μw process tolerant 6t subthreshold dtmos sram in 90nm technology," in *2008 IEEE Custom Integrated Circuits Conference*. IEEE, 2008, pp. 419–422.

[11] P.-H. P. Wang, H. Jiang, L. Gao, P. Sen, Y.-H. Kim, G. M. Rebeiz, P. P. Mercier, and D. A. Hall, "A near-zero-power wake-up receiver achieving- 69-dbm sensitivity," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 6, pp. 1640–1652, 2018.

[12] M.-E. Hwang, "Supply-voltage scaling close to the fundamental limit under process variations in nanometer technologies," *IEEE transactions on electron devices*, vol. 58, no. 8, pp. 2808–2813, 2011.

[13] R. Wei, W. Wang, X. Xiao, and Q. Chen, "A low-power σ-δ capacitance-to-digital converter for capacitive sensors," *IEEE Access*, vol. 7, pp. 78 281–78 288, 2019.

[14] M. Manghisoni, L. Gaioni, L. Ratti, V. Re, and G. Traversi, "Assessment of a low-power 65 nm cmos technology for analog front-end design," *IEEE Transactions on Nuclear Science*, vol. 61, no. 1, pp. 553–560, 2014.

[15] F. Centurelli, A. Fava, M. Olivieri, P. Tommasino, and A. Trifiletti, "A low-voltage class-ab ota exploiting adaptive biasing," *AEU-International Journal of Electronics and Communications*, vol. 122, p. 153282, 2020.

[16] X. Zhao, Y. Wang, D. Jia, and L. Dong, "Ultra-high current efficiency single-stage class-ab ota with completely symmetric slew rate," *AEU-International Journal of Electronics and Communications*, vol. 87, pp. 65–69, 2018.

[17] J. M. Algueta-Miguel, A. Lopez-Martin, M. P. Garde, A. Carlos, and J. Ramirez-Angulo, "$\pm$0.5 v 15μ w recycling folded cascode amplifier with 34767 mhz· pf/ma fom," *IEEE Solid-State Circuits Letters*, vol. 1, no. 7, pp. 170–173, 2018.

[18] Q. Zhang, Y. Wang, X. Zhao, and L. Dong, "Single-stage multipath class-ab bulk-driven ota with enhanced power efficiency," *AEU-International Journal of Electronics and Communications*, vol. 107, pp. 39–48, 2019.

Mesut Atasoyu Mesut Atasoyu received the Bachelor of Science (B.Sc), in Electrical and Electronics Engineering, from Ataturk University, Turkey, in 2009. He completed his Master of Science (MSc) in 2014 and a Ph.D. degree in Electronics Engineering from İstanbul Technical University. In 2022, He joined the Department of Electrical and Electronics Engineering, Ataturk University, as an assistant professor. His research interests lie in analog and digital integrated circuit design with nano-device modeling.