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MASTER SLAVE PHASE SYNCHRONIZATION METHOD WITH XOR AND PHASE/FREQUENCY DETECTOR PLL

XOR VE FAZ/FREKANS DEDEKTÖR PLL İLE MASTER-SLAVE FAZ SENKRONİZASYON METODU

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Abstract

Phase-locked loop (PLL) is a technique which has contributed significantly toward the technology advancement in communication. Phase and frequency synchronization problems have been present in electronic engineering since the first coherent modulation systems were developed. This paper gives basic details of PLL. It provides brief summary of the basic PLL principle applicable to control systems and digital communication. It also reports components of PLL and comparison among them. PLLs are responsible for recovering the correct time basis and synchronizing the processes. According to the application needs, different clock distribution strategies were developed, with the master-slave being the simplest and most used choice. PLL techniques is chosen for synchronization, since it is one of the most active synchronization techniques. This article contains Simulink of the MATLAB, simulation method and circuit design and mathematical solutions to synchronize PLL.

Keywords: Charge pump, phase locked loop, phase/frequency detector, voltage controlled oscillator, XOR phase detector.

Öz

Faz kilitli döngü (PLL), iletişimde teknolojinin ilerlemesine önemli ölçüde katkıda bulunan bir tekniktir. İlk uyumlu modülasyon sistemleri geliştirildiğinden beri elektronik mühendisliğinde faz ve frekans senkronizasyon sorunları mevcuttur. Bu makale, PLL'nin temel ayrıntılarını vermektedir. Kontrol sistemleri ve dijital iletişim için geçerli olan temel PLL ilkesinin kısa bir özetini sağlar. Ayrıca PLL bileşenlerini ve bunlar arasındaki karşılaştırmayı da bildirir. PLL'ler, doğru zaman esasını kurtarmaktan ve süreçleri senkronize etmekten sorumludur. Uygulama ihtiyaçlarına göre, master-slave en basit ve en çok kullanılan seçim olmak üzere farklı saat dağıtım stratejileri geliştirildi. Senkronizasyon için en aktif senkronizasyon tekniklerinden biri olduğu için PLL teknikleri seçilmiştir. Bu makale, MATLAB'ın Simulink'i, simulasyon yöntemi ve devre tasarımı ve PLL'yi senkronize etmek için matematiksel çözümler içermektedir.

Anahtar Kelimeler: Faz kilitli döngü, faz/frekans dedektörü, şarj pompası faz kilitli döngü, voltaj kontrollü osilatör, XOR Faz dedektörü.

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1. INTRODUCTION

Phase locking is a powerful technique that can be used to create effective solutions in a variety of applications. This study looked into MIMO systems since they are employed in a wide range of electronic warfare and radar applications. Many studies have looked into various methods of PLL phase synchronization in order to meet the needs of combining numerous software-defined radios into a suitable multi-channel receiver (Hsieh & Hung, 2006). Because of its ability to enhance data rates or improve system performance through multiplexing, multiple-input multiple-output (MIMO) technologies are gaining a lot of attention. Generally speaking, a Phase Locked Loop (PLL) is a feedback-based circuit that produces a signal that replicates its input signal (which is typically a sinusoidal signal of variable frequency) in frequency by locking in to and continuously adjusting its phase difference with the input signal (which is usually a sinusoidal signal of variable frequency). The Phase-Locked Loop circuit is composed of three main parts: a phase detector, a low pass filter, and a voltage-controlled oscillator.

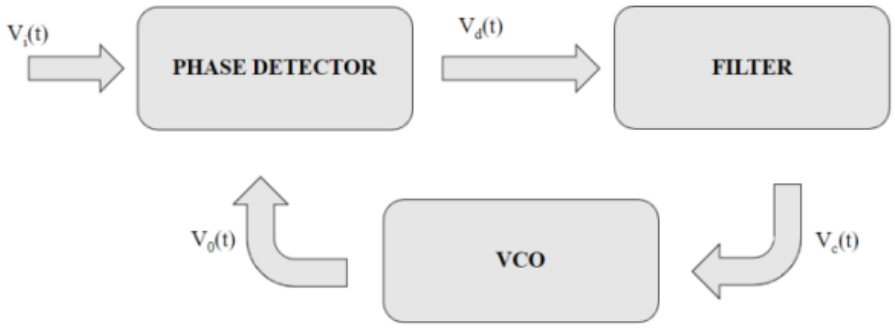

Figure 1. PLL Block Diagram

Additionally, a phase-locked loop (PLL) with a divider circuit in its feedback path can be used to multiply the frequency of an input signal. The PLL has received extensive research and is frequently used in communication circuits. A frequency multiplying PLL was chosen for the research topic due to its potential for additional uses such as modulation and demodulation. To generate stable frequencies or to recover a signal from a noisy communication channel, phase-locked loops are widely used in radio, telecommunications, computers, and other electronic applications. If the phase error of a phase-locked loop with the architecture shown in Figure 1 is less than the time interval (t1, t2), the loop is in a phase synchronous state (Piqueira, 2020). To synchronize this transformation with the input signal's fundamental frequency, the phase angle must be known and should be zero (De Brabandere & Loix, 2006). Temperature, thermal expansion, incompatible cable lengths, unrelated phase noise, ADC sample clock, and phase noise all cause shifts, and research are conducted to find answers to these issues. φ is the phase difference between input and output. θi is the input phase which come from the input sourse θo is the output phase which created from VCO. Phase difference formula is given in equation 1.

$$\varphi = \theta\mathrm{i} - \theta\mathrm{o} = 0, \forall \mathrm{t} \in (\mathrm{t1}, \mathrm{t2}) \quad (1)$$

After small perturbations, the model in a locked state approaches the same locked state (of the VCO phase, input signal phase, and filter state) (Leonov & Kuznetsov, 2015).

2. PLL DESIGN

PLL is primarily a servo system that controls the phase of its output signal in such a way that the phase error between output phase and reference phase is minimized. Figure 1 depicts the functional block diagram of a PLL, which consists of a phase detector (PD), a loop filter (LF), and a voltage-controlled oscillator (VCO) (Hsieh & Hung, 2006).

2.1. Phase Detector

There are numerous circuits that can be used as phase detectors, some of which employ analogue techniques, while others employ digital circuitry. However, the critical distinction is whether the phase detector is sensitive to only phase or to both frequency and phase. The generation of an output signal as a result of the phase difference of the input signals is defined as the operation of an ideal phase detector. PD generates an error signal proportional to the phase error, that is, the difference in the phases of the phase-locked loop's input and output signals. The three primary PLL applications are analog PLL, digital PLL, and all-digital PLL. In this study, master-slave synchronization is accomplished using an XOR phase detector and a phase/frequency detector. In a single-phase off-nominal frequency operation and in a three-phase unbalanced situation, the PLL technique eliminates the source of error. The PLL is not window-based, and thus there are no corrections or windowing issues (Karimi & Bakhshai, 2010).

2.1.1. XOR phase detector

A convenient method is to employ an XOR gate, a type of digital logic gate and given in figure 2. Thus, the sinusoidal waveform is first converted to a square wave (compatible with the digital logic). The comparator is based on the XOR gate and has two inputs. When both inputs are at the same level, either low or high, the XOR gate outputs logic 0. When one of the inputs is high and the other is low, it outputs a logic 1 signal.

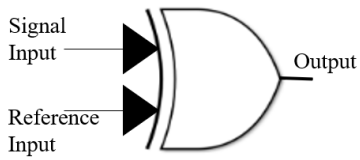

Figure 2. XOR Phase Detector

The disadvantages of this approach are that it is phase limited (-90, +90) degrees and does not sense signal edges (Lata & Kumar,2013). Unlike an analog mixer, KPD is not affected by the amplitude of the input signal and remains constant over a phase range. The XOR PD is duty cycle sensitive and will lock with a phase error if the input duty cycle is not 50%. The width of the output pulses varies according to the phase difference between the inputs, providing DC voltage to the VCO's input (Pawar & Shobba, 2017).

2.1.2. Phase / Frequency detector

The Phase Frequency Detector enables a wide range of frequency locking, potentially the entire tuning range of the VCO.

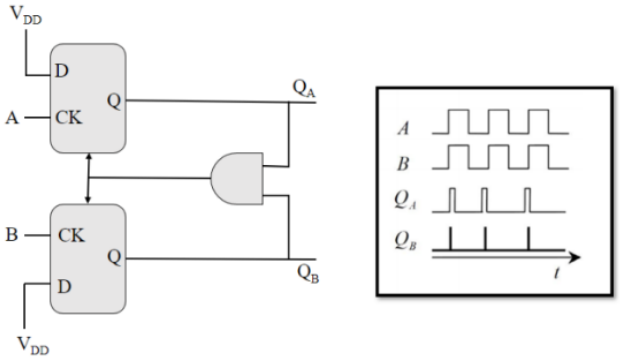

Figure 3. Phase Frequency Detector

The frequency of the VCO must be increased to match the input and shematic version is given in figure 3. Similarly, when the VCO input (B) switches to the high position, the QB output increases (Ayat & Babei, 2010).

2.1.3. PFD and charge pump PLL

The phase error information provided by PFD is converted into a voltage by the charge pump with the loop filter. A charge pump PLL circuit is shown in Figure 4. It is formed by two current sources, which are I_{up} and I_{dn}, as well as a switch for each current source. Before it reaches the VCO, the charge pump's current output is filtered by a low pass filter. The PFD architecture is completely dead zone-free, uses very little power, and operates at a high frequency (Majeed & Abdul, 2013).

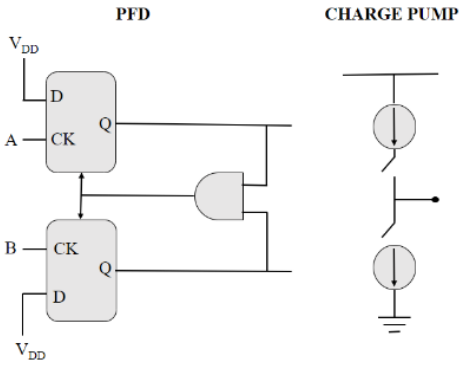

Figure 4. Charge Pump PFD

2.2. Loop Filter

The dynamic behavior of a Phase Locked Loop is determined by the Loop Filter and its transfer function is F(s). The phase detector is the loop filter's input, and the VCO control voltage is the loop filter's output. Basic loop filter is given in figure 5. The PLL filter is required to filter out any undesired high-frequency components that may pass through the phase detector and into the VCO tune line. The filter has an impact on the loop's ability to change frequencies quickly. If the filter has a low cut-off frequency, the changes in tune voltage will be slow, and the VCO will be unable to change its frequency as quickly. If the filter is not designed properly, oscillations can form around the loop, resulting in large signals on the tune line.

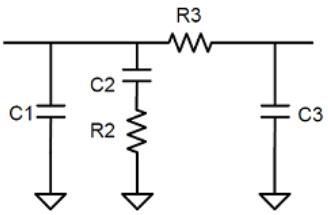

Figure 5. Loop Filter Schematic

Loop filter transfer function is given in Equation 2.

$$Z(s) = \frac{R2 \cdot C2 \cdot s + 1}{A3 \cdot s^3 + A2 \cdot s^2 + A1 \cdot s}$$
$$\mathrm{A1} = C1 + C2 + C3 \quad (2)$$
$$A2 = (R2 \cdot C2 \cdot C3) + (R2 \cdot C1 \cdot C2) + (R3 \cdot C3 \cdot C1) + (R3 \cdot C3 \cdot C2)$$
$$\mathrm{A3} = C1 \cdot C2 \cdot C3 \cdot R2 \cdot R3$$

Z(s) is the transfer function of the loop filter. Loop filter is a passive filter so R2 and R3 are a resistor. C1, C2 and C3 are the capacitor of loop filter. A1, A2 and A3 are the simplified version of the loop filter equation. In some applications, very precise transient responses are required. Higher-order filters can be used to improve PLL performance in these cases, resulting in nonlinear loops with orders greater than two. Such systems are not investigated here because nonlinear terms can cause undesirable behaviors such as error oscillation and chaos, which reduce the synchronization ranges, depending on parameter value combinations (Piqueira & Caligares, 2007).

2.3 Voltage Controlled Oscillator

The voltage controlled oscillator is the third block, which is a positive feedback amplifier (VCO). The VCO produces simultaneous square and triangular wave outputs (Li & Han, 2017), which change in response to the input control voltage (created by the loop filter) until the two frequencies are equal. Basic voltage controlled oscillator shematic is given in figure 6. As a result, the loop must first tune the VCO frequency to the input frequency. Frequency pull-in is the term for this process. The VCO phase must then be adjusted to match the input phase. Phase lock-in is the term for this procedure. Frequency pull-in and phase lock-in are both parts of acquisition, which is a highly nonlinear and difficult to analyze process. The PLL achieves the phase-locked condition after acquisition, in which it tracks the input phase. The VCO frequency is equal to the input frequency in this phase-locked condition.

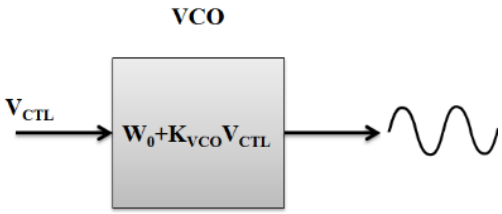

Figure 6. Voltage Controlled Oscillator

Phase stability, large frequency deviation, high modulation sensitivity K_v, frequency linearity versus control voltage, and the ability to accept wide-band modulation are the main requirements for the VCO. All four requirements are in direct opposition to the phase stability requirement

(Hsieh & Hung, 2006). Because the VCO frequency of the larger division ratio oscillates thousands of times per second, while the frequency of the reference oscillator is only a few hertz, simulating the dynamic behavior of the PLL circuit with a transient model is a slow process that takes a long time and a lot of resources. In order to avoid this problem, behavior simulation of the PLL circuit based on a mathematical model has been widely used (Li & Wu, 2017).

3. PLL IMPLEMENTATION

3.1. PLL Implementation with XOR Phase Detector

Assuming logic 1="+1" and 0="-1", the XOR PD will lock when the average output is 0. Generally, π/2 is a stable lock point and -π/2 is a metastable point Sensitive to clock duty cycle. Below is the Simulink schematic created using the XOR phase detector. Simulink implementation of the XOR detector and PLL is given in figure 7. The Power Spectral Density Estimate graph of this system is given in Figure 8.

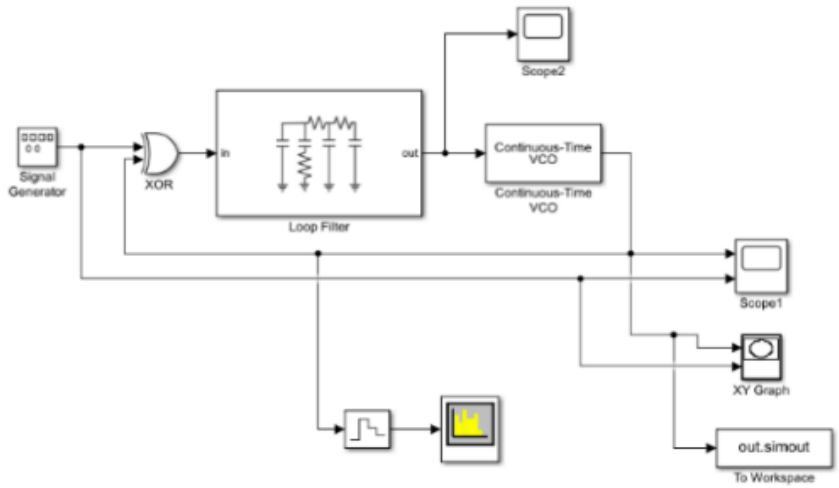

Figure 7. PLL Implementation with XOR Phase Detector

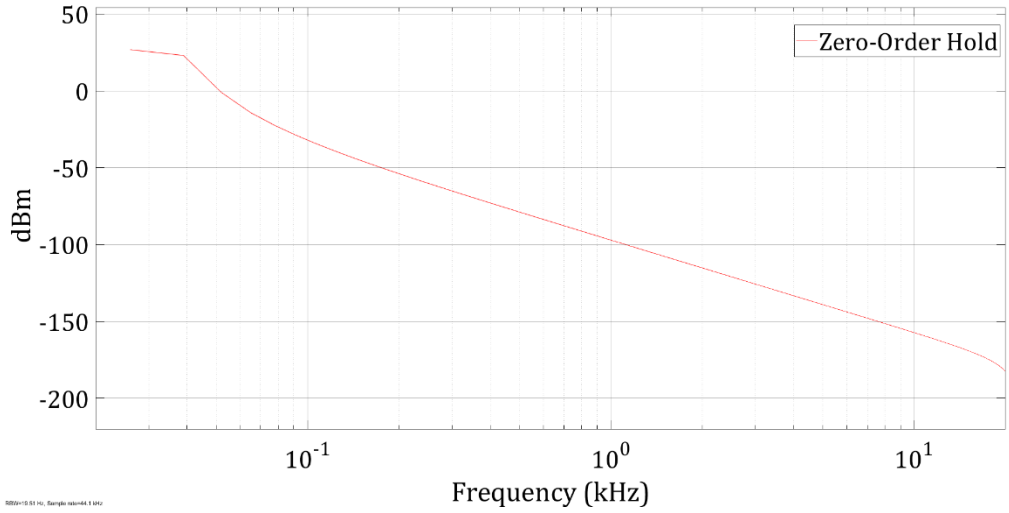

Figure 8. Power Spectral Density Estimation for XOR Phase Detector

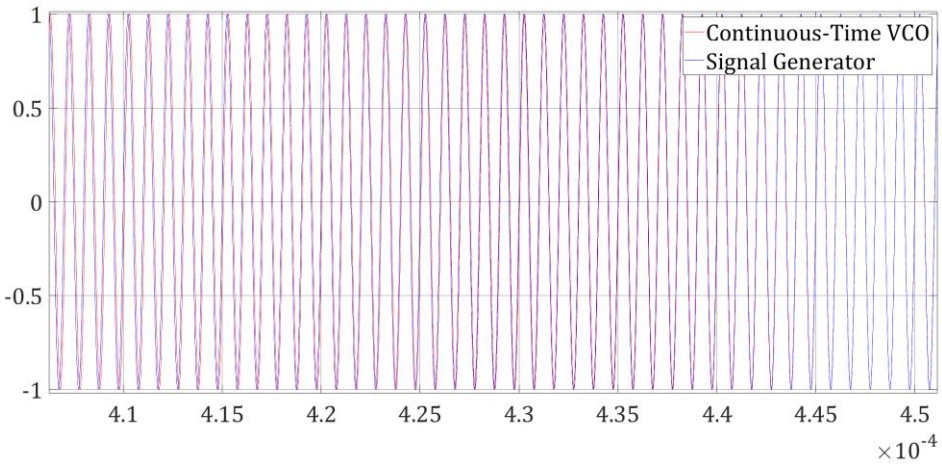

Figure 9. VCO and Input (Signal generator) Result at The Scope

3.2 PLL Implementation with Phase/Frequency Detector and Charge Pump

By comparing the phases of input signals, this PFD detects frequency differences. The clock edges of input signals detect a phase difference. This charge pump consists of two switched current sources that, depending on the PFD output, pump charge into or out of the loop filter. When the feedback signal precedes the reference, the PFD detects a rising edge on the reference frequency and generates a UP signal (Kailuke & Agrawal, 2014). Control pulses (typically referred to as UP and DOWN) generated by the phase detector drive the charge pump; the width of the UP and DOWN pulses is determined by the phase difference between the reference input and the internal VCO-derived signal. Detailed Simulink diagrams for PFD are shown in Figure 10 below. The PFD and charge pump are employed in this design. The VCO was implemented as a continuous VCO.

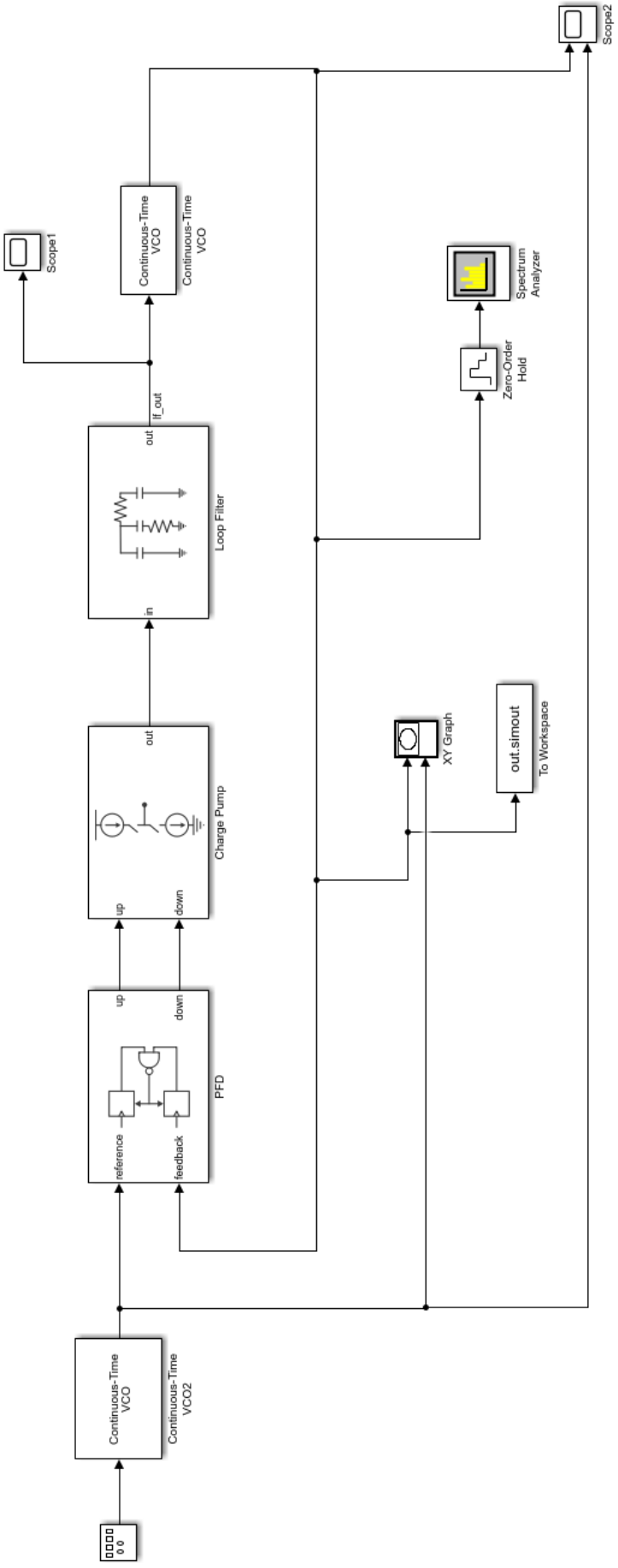

Figure 10. PLL Implementation with PFD and Charge Pump

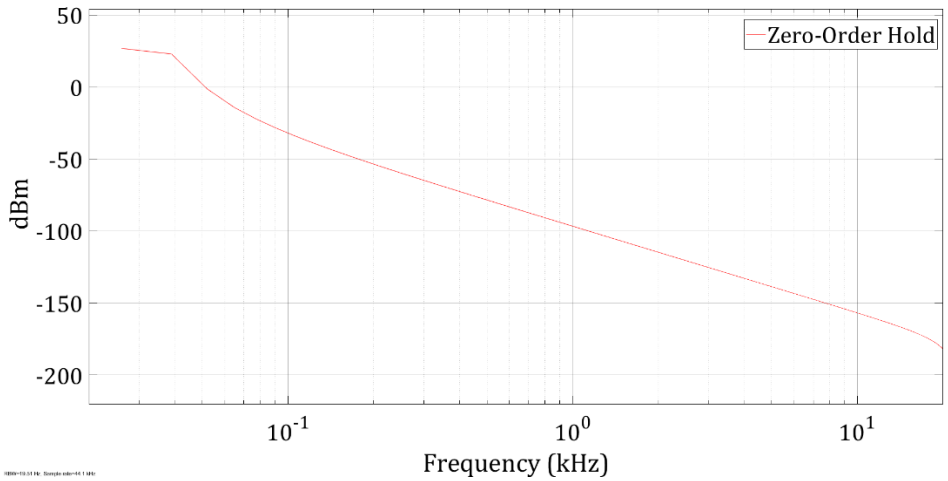

Figure 11. Power Spectral Density Estimation for Charge pump PFD Detector

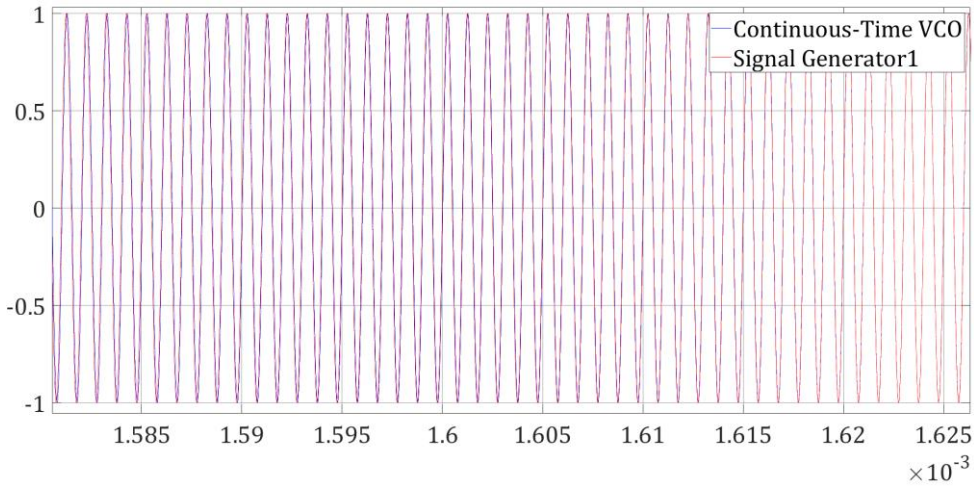

Figure 12. VCO and Input (Signal generator) Result at The Scope

4. SYNCHRONIZATION METHOD

When using master-slave in a test system, this high phase stability can be achieved (Piqueira, 2020). In this application, the master-slave method is used to synchronize. When using this method, the slave accepts the first VCO output master as an input, and the input is thus synchronized with the signal generator. For the PLL created with two different phase detectors, this synchronization method was tried. XOR phase detector and Phase/frequency detector are the two types. This research makes use of MATLAB Simulink. The results are presented in the form of a graph and a table below. If the natural frequencies aren't identical, the phases may not be synchronized, necessitating the use of additional optimization techniques (Hsieh & Hung, 2006).

4.1 Master-Slave Synchronization

The XOR and PFD PLL types are used to investigate master-slave synchronization architectures, using the model presented in which a phase detector compares the phases of two periodic signals, one coming from the outside, with being the phase of $v_i(t)$, and the other, from an internal oscillator, with θ_0 being the phase of $v_0(t)$, with the output $v_d(t) = v_i(t) \cdot v_0(t)$ (Piqueira, 2020). In telecommunication networks with single-chain master-slave clock

distribution architecture, the existence and stability conditions for the synchronous state are determined (Monteiro & Santos, 2003).

4.1.1 XOR phase detector and master –slave implementation

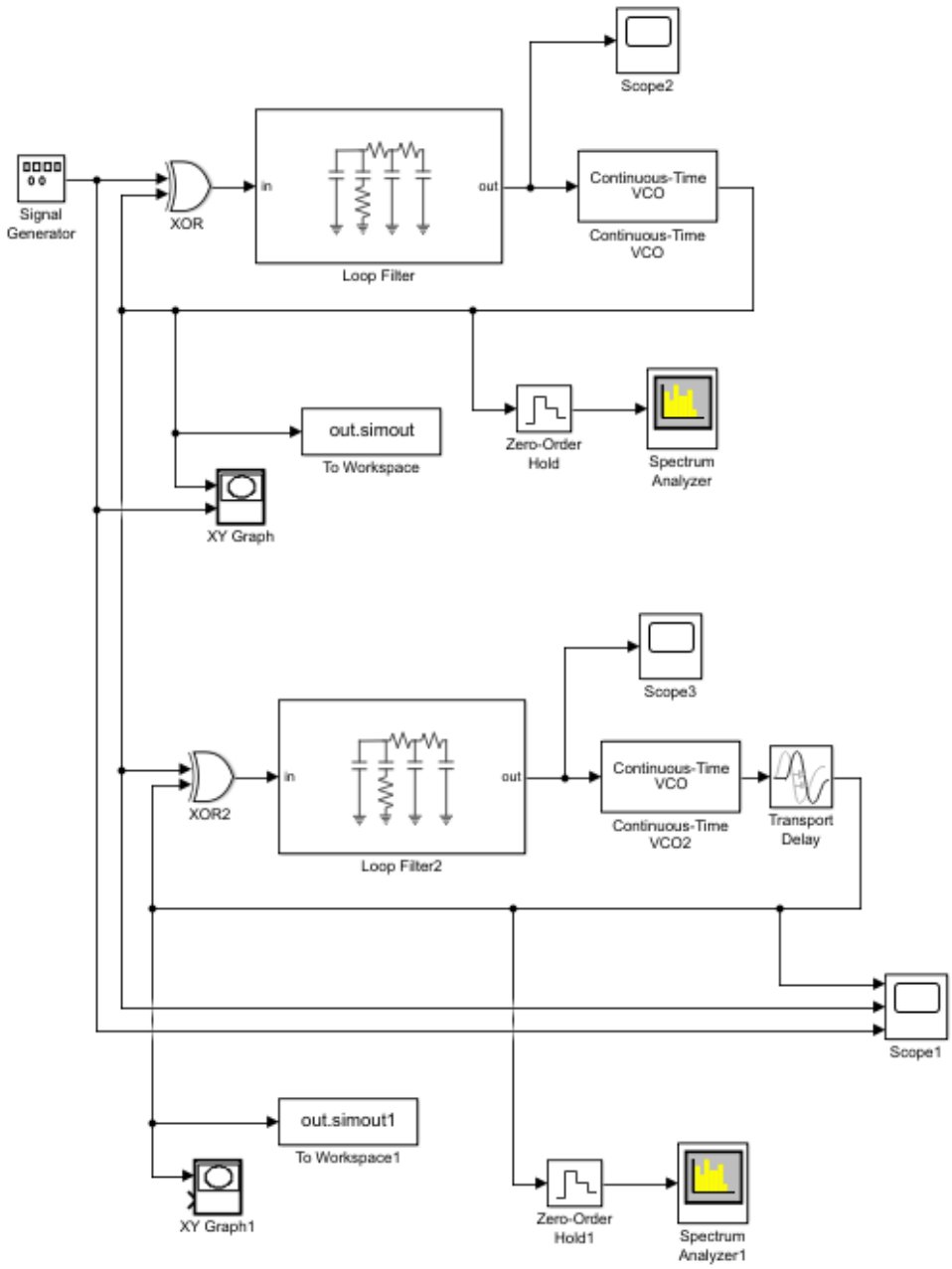

Figure 13. Master –Slave Implementation with XOR Phase Detector

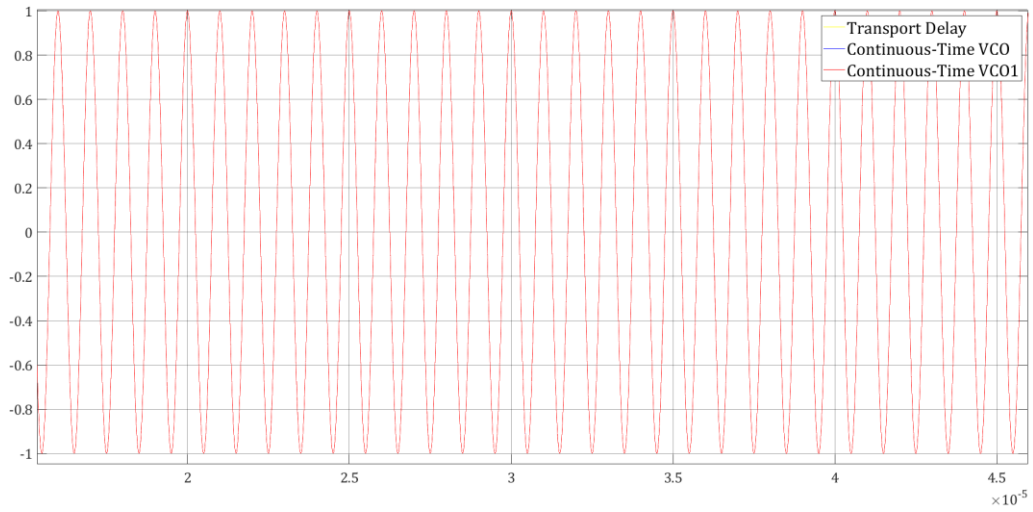

Figure 14. Master and Slave VCO and Input (Signal generator) Result at The Scope

Figure 13 shows the master-slave application of the system created with the XOR phase detector. Figure 14 shows the result of this system, which uses the output of the first VCO as the input of the other PLL. The results of the first input master VCO and slave VCO are shown in this diagram.

4.1.2 Phase/Frequency detector and charge pump master –slave implementation

With many different possible designs available for PFD a Master-Slave topology was found to be one of the best for this implementation. For the master-slave application, the VCO output of the first system is taken as the input for the other PLL. The Simulink scheme of this system is given in figure 15 below.

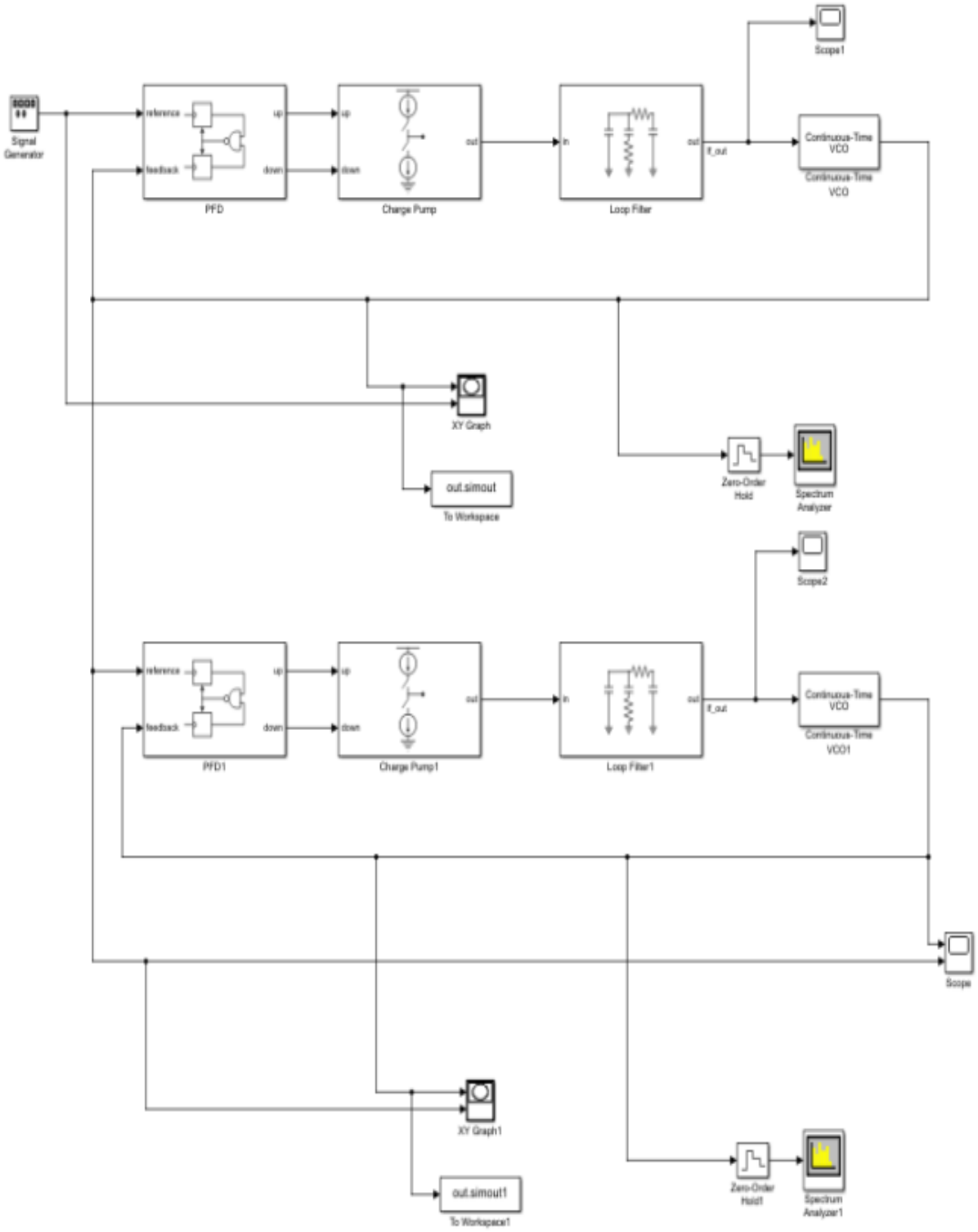

Figure 15. Master –Slave Implementation with PFD and Charge Pump

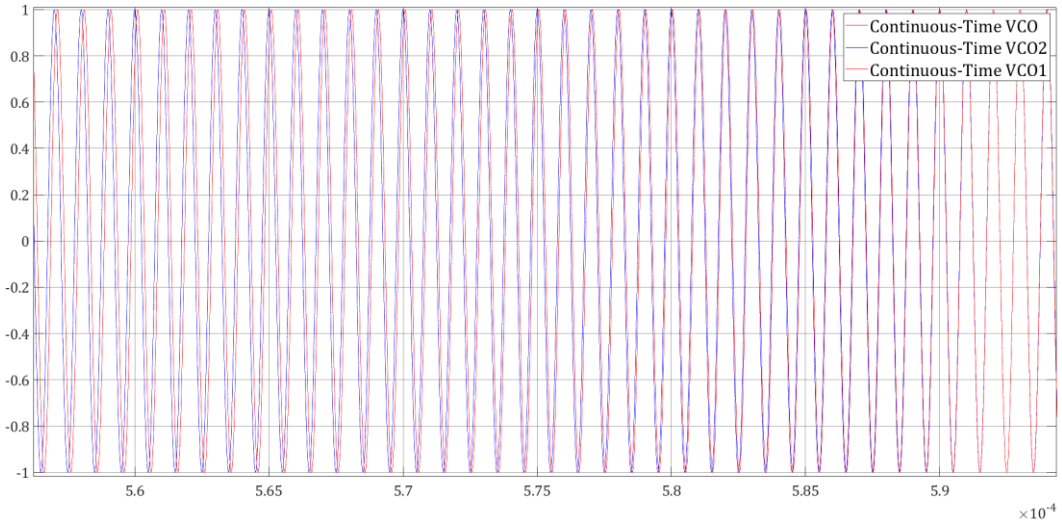

Figure 16. Master and Slave VCO and Input (Signal generator) Result at The Scope

Figure 15 shows the result of this system, which uses the output of the first VCO as the input of the other PLL. The results of the first input master VCO and slave VCO are shown in this diagram. It can also be used for PFD and charge pump master-slave synchronization, as can be seen in figure 16.

5. CONCLUSIONS

This paper provides an overview of the PLL technique, which is used for master-slave synchronization. The graphs also show the results of the PLL technique and the master-slave relationship. MATLAB-Simulink was used to present and report detailed block schematics. A detailed comparison of all the blocks has been reported. According to the advantages of an XOR phase detector that is sensitive to both the clock duty cycle and the input duty cycle, it can lock with a phase error if the input duty cycle is less than 50%. It is not sensitive to edges, according to the disadvantages. The Phase Locked Loop (PLL) is a key circuit that is often utilized in many types of demodulation circuits. PLL is utilized in defensive systems in high-end applications. In general, PLL operates by comparing the input signal to the frequency of an oscillating signal. PLL is used in defense systems to track the target frequency (assumed to be in the frequency range when the missile is fired). PLL, which is utilized in a variety of applications including radar, can be employed in conjunction with these studies in radar applications. As a result, data may be lost, and it detects only phase differences between inputs, not frequency differences. One of the benefits of a PFD charge pump is that it detects both phase and frequency differences between input and output. The PFD is not affected by the input duty cycle. When the connection between PLL and frequency is examined the phase-locked loop allows for the generation of steady high frequencies from a low-frequency reference. The PLL approach can help any system that requires stable high frequency tuning. Wireless basestations, wireless handsets, pagers, CATV systems, clock-recovery and -generation systems are examples of these uses. A GSM cellphone or base station is a nice example of a PLL application. It can be worked for different frequency applications in PLL applications by looking at the examples above. In addition, future studies will use and test the relationship between PLL and frequency, as well as its implementation in various applications.

Contribution of The Authors
Contributions of authors to the article are equal.

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Statement of Interest Conflict
There is no interest confliction between the authors.

Statement of Research and Publication Ethics
Research and publishing ethics are taken into account in this study.

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