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Comparison of PWM and PCM Based Digital-Analog Converter Structures

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Abstract: In this work performance limitations of various pulse-width modulation architectures are compared. First, classical pulse-width modulation based analog digital converter is analyzed. Then, pulse-count modulation based digital-analog converter is explored. The structures are implemented on Altera™ Stratix III FPGA. A sawtooth test signal is generated to analyze the performance of the DAC structures. Maximum effective resolution is calculated depending on the architecture selected. The paper is especially useful for the practicing engineers who deal with embedded system design and develop pulse-width modulation and pulse count modulation based digital-analog converters on microcontrollers and FPGA systems.

Keywords: *Pulse width modulation (PWM); pulse count modulation (PCM); digital-analog conversion; low pass filter; embedded systems.*

1. Introduction

Pulse width modulation digital-analog conversion is a popular data conversion technique for embedded systems. The advantage of the system is that, the system only requires pulse-width modulator inside the controller and an external RC filtering is required to acquire desired analog signal at the output [1]. Since most of the microcontrollers include pulse-width modulators inside, only an RC filter is required to achieve desired analog signal. The implementation is popular for its low cost and easy configuration [2-5]. The resolution of the PWM DAC is limited by counter range of the PWM generator and switching noise after the filter. As a result, the resolution of the PWM DACs is not adequate for many of the embedded system requirements whenever high resolution is needed.

In [5] an alternative implementation for the PWM DAC, pulse-count modulation (PCM) is defined. The PCM method increases performance; however, the implementation is not possible using internal PWM modules of the microcontrollers. Delta-sigma PWM DACs provide high resolution [6-8]; however, the implementation of delta-sigma conversion is not possible by using basic PWM modules of general-purpose microcontrollers, rather, it requires digital and analog full custom design blocks which is not suitable for low-cost general-purpose design.

In this work, PWM and PCM DAC structures are implemented using an FPGA board and effective resolution of the DAC structures are analysed depending on the switching noise at the outputs of the structures.

2. PWM and PCM Digital-Analog Converter Logic Systems

General PWM digital-analog converter (PWM DAC) structure is shown in Fig 1. Here, f_{sys} is the clock frequency of the general system. Duty cycle of the PWM modulator is the input of the system, which is entered as digital value, and analog value at the output is proportional to the duty cycle at the system. PWM modulation frequency must be filtered out to have the desired analog value at the output [2-5]. By employing a simple RC low-pass filter at the output of the PWM modulator, desired analog is output is achieved. A second order RC filter stage provides better implementation of the PWM DAC [5, 9]. Although it is possible to use higher order filters they are not preferred due to increased design cost. Generally, second order filter is sufficient to obtain the desired output [9].

The duty cycle of a pulse width modulator contains the desired analog signal data. The output of the DAC can swing between GND and V_{MAX}. The maximum output voltage at the output node and least significant bit (LSB) amplitude is given as:

$$V_{MAX} = V_{DD}\left(1-\frac{1}{2^m}\right) \quad (1.a)$$

$$V_{LSB} = V_{DD}\frac{1}{2^m} \quad (1.b)$$

where m is the resolution of the m-bit DAC, i.e., m is the bit size of the DAC digital input; V_{DD} is the supply voltage of the digital system. The normalized value of the analog signal $s(t)$ can be represented as duty cycle of the PWM:

$$s(t) = Duty(t) = \frac{Digital\ input}{2^m} \quad (2)$$

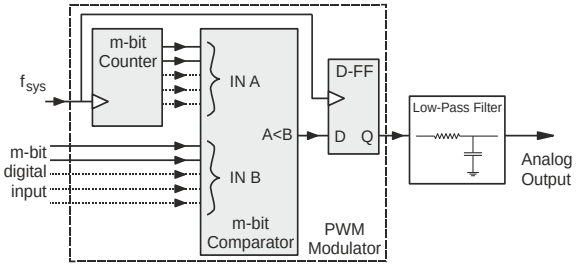

Figure 1. Pulse Width Modulator Structure

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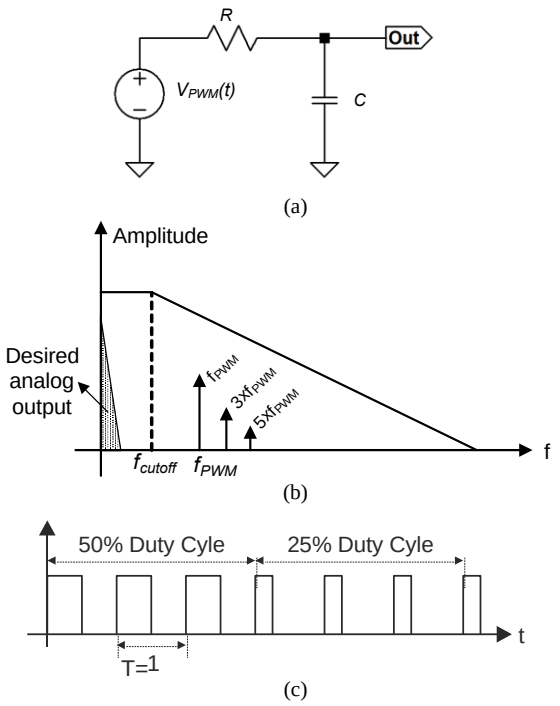


Figure 2. (a) PWM digital-*to*-analog converter; (b) frequency domain representation of PWM signal; (c) time representation of the PWM modulation

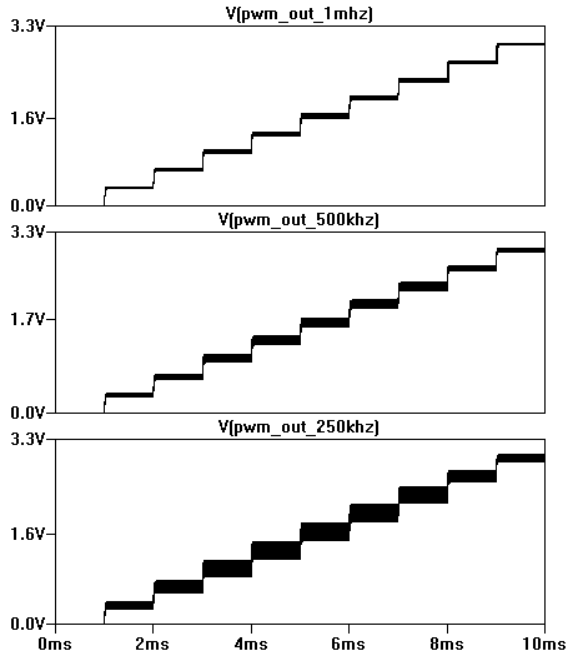


Figure 3. Analog *output* generated using various PWM frequencies

he PWM output is composed of two signals, i.e., the desired analog output and pulse-width modulator frequency. Since the analog signal band-width is much smaller than the modulator frequency, the analog signal component of the PWM DAC, i.e. *Duty*(*t*) signal is quasi-stationary. Hence, the quasi-stationary part of the signal contains the analog output data. Therefore, the modulator frequency must be filtered out. Fig. 2(a) shows circuit equivalent of PWM DAC; Fig. 2(b) shows the PWM signal in frequency domains, and, Fig. 2(c) shows the time domain switching characteristics. The modulator signal is filtered out using a first order RC filter to have the desired analog output in Fig 2(a). As an example, if the desired analog signal is 0.3V, then the duty cycle of the modulator has to be 30%, if 0.5V analog signal is required, then the duty cycle has to be 50%. The values are normalized to the supply voltage of 1V. The transfer function of simple RC filter at the output of PWM DAC as shown in Fig. 2(a) is:

$$\frac{V_{Out}(j\omega)}{V_{PWM}(j\omega)} = \frac{1}{1+ j\omega RC} \tag{3}$$

The cutoff frequency for the desired analog signal can be calculated as:

$$f_{cutoff} = \frac{1}{\tau} = \frac{1}{RC}(rad/s) \tag{4}$$

In Fig. 3, analog outputs are generated using various modulation frequencies. The analog signal is generated sweeping the duty cycle from %0, %10, ... %90 at each milliseconds. Here, supply voltage is selected to be 3.3V. In each of the step outputs, the analog signal band-width is selected to be 20 kHz, and, using (4), *R* and *C* values are selected to be 0.8 nF and 10 kΩ. As can be seen from Fig. 3, removal of modulator noise from the analog signal is very critical to reach a desired output resolution level, if modulation frequency is increased, then output noise level is less at the output. On the other hand, if PWM modulator frequency is increased, then PWM resolution decreases since,

$$f_{PWM\_MAX} = \frac{f_{sys}}{2^m}, \tag{5}$$

where *m* is the resolution of the PWM modulator.

The effective resolution of the PWM DAC depends on the pulse-width modulator resolution, desired output frequency band (f_{cutoff}), and the filter performance for the pulse-width modulator frequency suppression. The remaining pulse-width modulator frequency component appears as noise at the output and limits the resolution of the DAC. Even if *m*-bit counter is utilized for the PWM module as shown in Fig. 1, it does not guarantee m-bit resolution. The reason is that, if PWM DAC output noise is higher than the V_{LSB} as given in (1.b), then the effective resolution will be less than *m*-bits.

For most of the applications, a first order RC filter stage is not sufficient for the removal of the PWM noise. In general, second order filter is employed to reach higher resolution levels. Here, in order to reach for the desired resolution requirements an empirical cutoff frequency calculation for a second order RC filter is given. Different types of low-pass filter structures is also suitable for filtering the switching noise. However, second order RC filter is the simplest topology.

A possible implementation of a second order RC filter is shown in Fig. 4(a). Here, in order to reduce the loading effect, the resistor in the second stage is selected as 2R. Regarding to this, the second stage capacitor value is selected to be C/2. The filter transfer function of the circuit in Fig. 4(a) is:

$$\frac{V_{out}(s)}{V_{PWM}(s)} = \frac{1}{(RC)^2 s^2 + \frac{5}{2}RCs + 1} \tag{6}$$

The frequency response of the second order RC circuit in Fig. 4(a) for component values of R = 5k and C = 1nF is shown in Fig.4(b). Here, frequency is 30 kHz. Using the configuration in Fig. 4.(a) cutoff frequency can be extracted using SPICE simulations as:

$$f_{cutoff} \approx \frac{0.1575}{RC} (\text{Hz}) \quad (7)$$

The calculation is based on the assumption that second order filter asymptotically -40dB/decade amplitude decrease at the output which is represented as in Fig 4.b. The line cut at 0dB point gives empirical equation (7) whenever component values are selected as shown in Fig.4.a. The calculation eases filter

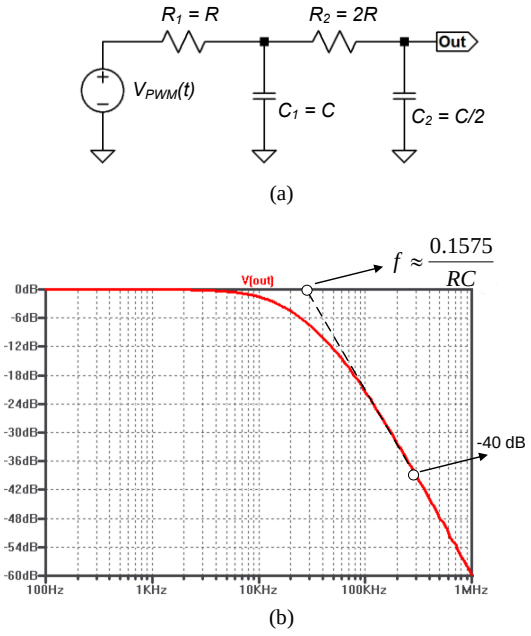


Figure 4. (a) Second order RC *filter*; (b) frequency response

design process.

The second order RC filter shown in Fig. 4(a) has R and 2R resistor values and C and C/2 capacitance values, which provides easy implementation. In addition, the cut-off frequency in (7) provides a fast calculation method without complex filter calculations.

As mentioned, PWM DAC output is severely affected by the switching noise of the pulse-width modulator. As a result, effective resolution of PWM DAC is quite limited. To overcome this limitation, a small modification over the PWM structure can be made to have pulse-count modulation scheme. The pulse count modulation (PCM) scheme is shown in Fig. 5. In this structure, only comparison bits are crossed from MSB to LSB. Equivalent duty cycle is the same as PWM DAC. However, PCM switching frequencies are much higher than PWM DAC. So that, much better effective resolution can be handled. The hardware modification is very easy whenever FPGA implementation or VLSI implementation is available. However, the case is more complicated whenever microcontroller implementation is considered.

PWM and PCM duty cycle scheme for 4-bit modulator is shown in Fig. 6. As the total duty cycle is same over whole period, analog signal output is same for both of the structures. Moreover, switching noise after the RC filter is much less whenever PCM is implemented. PCM switching harmonics are shown in Fig. 7. The switching frequencies of both PWM and PCM can be compared. It is obvious that, higher frequency components can be filtered out much easier in PCM since switching harmonics are at much higher frequency points whenever compared to the PWM frequency plot which is shown in Fig. 2.b. Since the harmonics of the PCM modulator resides at much higher frequencies compared to PWM structure, filtering out the switching noise from the desired signal is much effective. As a result, much better effective DAC resolution is possible

3. Experiments and Discussions

To experiment the PWM and PCM DAC, both of the structures is constructed using an FPGA board with Altera™'s CycloneIII FPGA. The modulator output is filtered out using second order RC filter as shown in Fig. 4(a). The cutoff frequency of the filter is calculated using (7) as 30 kHz, where R1 = 5k, R2 =10k, C1=1nF and C3 = 0.5nF. The system frequency f_{sys} is 50 MHz in the system setup.

To compare same structures, a test pattern of sawtooth wave is digitally generated using PWM and PCM DACs with 9-bit PWM and PCM modulators, i.e. *m* is selected to be 9. The signal outputs of the two of the DAC structures are shown in Fig. 8.

It is obvious that PCM DAC switching noise after the filter gives much better results compared to PWM DAC output. PCM DAC effective resolution is approximately 9-bits. PWM effective resolution is much less, even same size PWM and PCM modulators are implemented. However, PWM effective resolution can also be improved to have better results. To increase effective resolution, *m* is modified to 7. If f_{PWM} which is given in (5), is increased, then, switching noise decreases. As a result, 6 to 7 bits of resolution is also achieved using PWM DAC as well. PCM DAC provides 2 to 3 bits of more effective resolution in the provided test setup. The effective resolution is calculated as maximum switching noise measured at the output of the DAC is less than least significant bit amplitude of the DAC.

PCM DAC implementation can also be possible for microcontroller implementations, whenever SPI™ port is used as PCM modulator source and periodically SPI port is driven by PCM data by reversing the data output as given in the scheme as shown in Fig. 5, which is planned to be next implementation to test the microcontroller performance of PCM DAC structures as well.

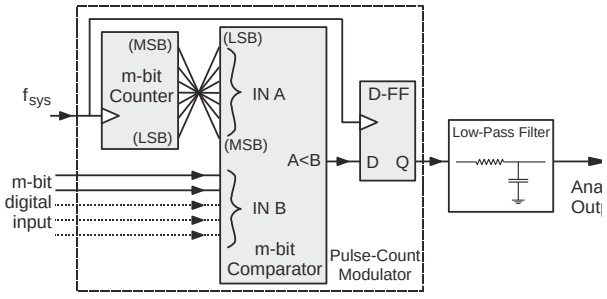


Figure 5. Pulse *Count* Modulation DAC Structure

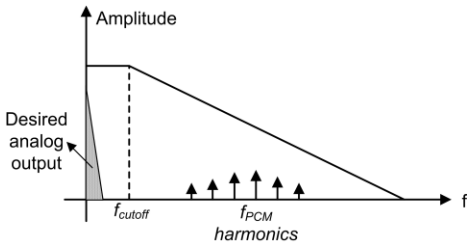
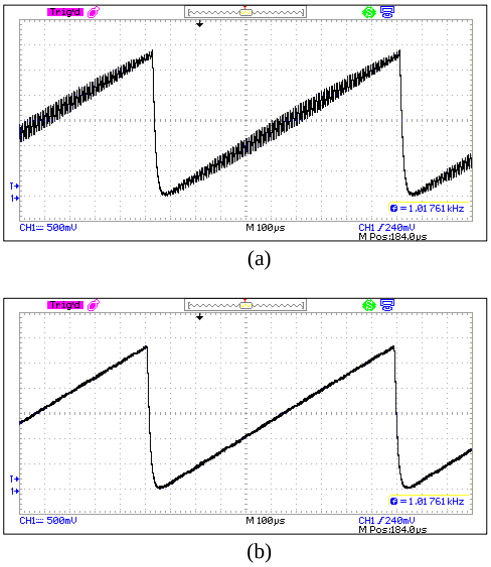


Figure 7. Pulse Count Modulation switching harmonics

4. Conclusions

PWM and PCM DACs are constructed using an FPGA development board. Two of the DAC structures requires same hardware resources. However, PCM DAC provided 9-bit effective resolution whereas PWM exhibited up-to 7-bits of resolution due to the fact that PCM switching noise can be more effectively suppressed. PCM DAC can be an alternative solution for FPGA and VLSI implementations whenever a simple and efficient DAC structure with moderate analog frequency band is required.



(a)

(b)

Figure 8. (a) PWM DAC output; (b) PCM DAC output (m = 9)

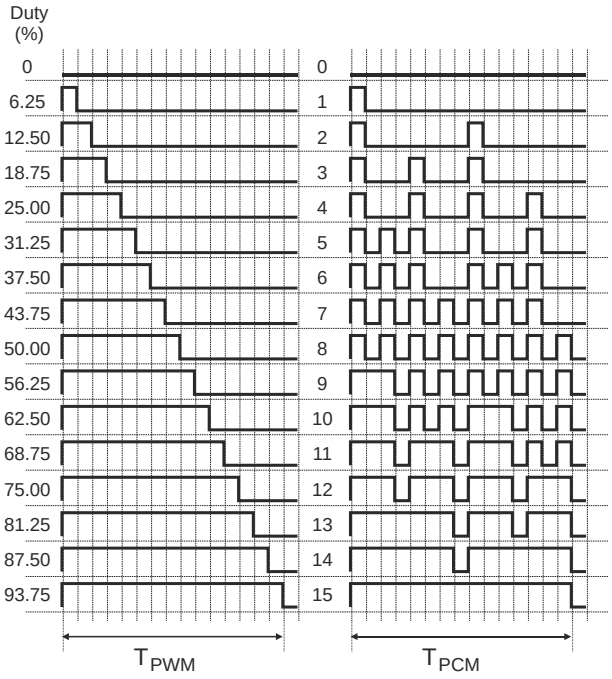


Figure 6. Duty cycle switching scheme of PWM and PCM modulators

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