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Design and Implementation of High Speed Artificial Neural Network Based Sprott 94 S System on FPGA

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Abstract: FPGA-based embedding system designs have been preferred for industrial applications and prototyping because of the advantages of parallel processing, reconfigurability and low cost. Due to having characteristic structure of the parallel processing of Artificial Neural Networks (ANNs), these systems provide the advantage of speed and performance when they are implemented with FPGA-based hardware. The hardware implementation of transfer functions used for modeling non-linear systems is a challenging problem. Therefore, this problem creates convergence problems. In this paper, non-linear Sprott 94 S system has been modeled using ANNs running on FPGA. All related parameter values and processes are defined with IEEE-754-1985 32-bit single precision floating-point number standard. ANN-based Sprott 94 S system design has been developed using VHDL synthesized using Xilinx ISE Design Tools. In test stage, ANN-based Sprott 94 S system has been tested using 3X100 data set and obtained error analysis results have been presented. The constructed design has been performed for Xilinx VIRTEX-6 family XC6VHX255T-3FF1923 FPGA chip using Place&Route process and chip usage statistics have been given. The clock frequency of ANN-based Sprott 94 S system which has pipeline processing scheme has been obtained with the value of 304.534 MHz. Accordingly, the proposed FPGA-based ANN system has produced 3X3.284 billion outputs in 1 second.

Keywords: *FPGA, VHDL, Nonlinear Systems, ANN, Sprott 94 S System*

1. Introduction

Currently, **F**ield **P**rogrammable **G**ate **A**rray (FPGA) chips have been used many areas since they have advantages like parallel processing, reconfigurablity, high speed comparable to other **H**ard**W**are (HW) systems, possibility of the verification the designs by testing before the implementation of the HW, very low-cost than Application Specific Integrated Circuits (ASIC) HW for prototyping. Control [1], sensors [2], image processing [3], signal processing [4], converter systems [5], computer graphics [6], medicine [7], radio frequency systems [8], Artificial Neural Networks (ANNs) [9] are among the usage areas of FPGAs. ANNs, which are one of the research areas of FPGA-based HW, are parallel information processing systems in their nonlinear structure. These systems need speeding up the computational process in real time engineering applications. There are also other ways to implement the ANNs as HW: Digital Signal Processing (DSP) chips and ASIC. Once an ANN is implemented as an ASIC HW, the network configuration cannot be modified later. Since the DSP chip performs given tasks in a serial fashion, DSP chip implementations cannot exploit the parallelism in ANN applications. The Transfer Functions (TFs) that used in ANNs have been divided into two parts, namely linear and nonlinear [10]. Because of having exponential operations in nonlinear TFs, the implementation of these functions in HW could be difficult when high speed and precision are required. In this paper, high speed discrete-time ANN-based system has been modelled using FPGA chips. Logarithmic Sigmoid (LogSig) TF has been used for the hidden layer of ANN-based system. In the work, 32-bit single precision floating-point standard has been used and the system is coded with **V**ery **H**igh Speed Integrated Circuit (VHSIC) **D**escription **L**anguage (VHDL). In Section 2, general information about FPGA chips and ANNs have been given. In Section 3, the Sprott 94 S system has been presented. In Section 4, the structure and test process of the designed ANN-based discrete-time Sprott 94 S system on FPGA have been given. Besides, chip statistics and performance results obtained from implementation have been presented. Finally, the results of the study have been interpreted and some orientations have been announced for future work in Section 5.

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2. General Information

2.1. FPGA Chips

FPGA chips, which provide flexibility in programmable systems using prebuilt resources, are high performance, reprogrammable and capable of parallel processing devices. Nowadays, these chips have various clock frequencies and HW features. IEEE-754-1985 64-bit, 32-bit or 16-bit floating-point and IQ-Math fixed point representations have been used in these chips by coding with VHDL, Verilog and Handle-C. Figure 1 shows Virtex-6 FPGA board produced by Xilinx. In general, FPGA chips consist of Input/Output-Blocks (I/O-Bs) that are dedicated to communicate with the outer world, Configurable Logic Blocks (CLBs) that perform logic functions and interconnects that can be programmable. CLBs contain Look up Tables (LUTs), multiplexers and flip-flop units [11].

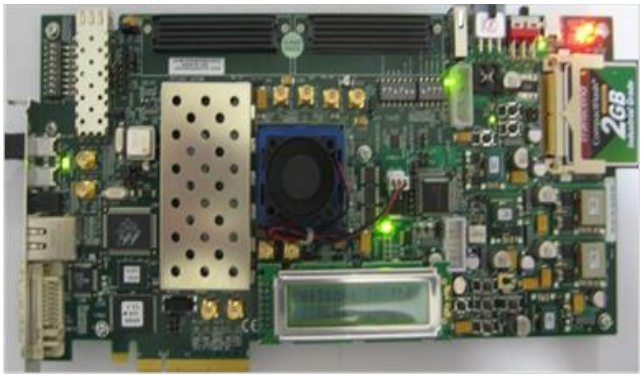

Figure 1. Xilinx Virtex-6 FPGA board

2.2. Artificial Neural Networks

Recently ANNs are artificial intelligence structures developed for modelling nonlinear systems by mimicking the learning skills of human brain. ANN-based systems are utilized in numerous areas such as motors [12], control [13], medical [14], optimization [15, 16], signal-image processing [17, 18], prediction [19, 20]. TFs used in ANNs are divided into two parts: linear and nonlinear. While pure linear, positive linear, hard limiting, and symmetric hard limiting TFs are the examples of linear TFs, radial basis, logarithmic sigmoid and hyperbolic tangent sigmoid TFs are the examples of nonlinear TFs [21]. There are ANN structures like Feed Forward Neural Networks (FFNN), Recurrent Neural Networks (RNN) and Cascade-Correlation Neural Networks (CCNN) in literature. The structure of FFNN has been given in Fig. 2.

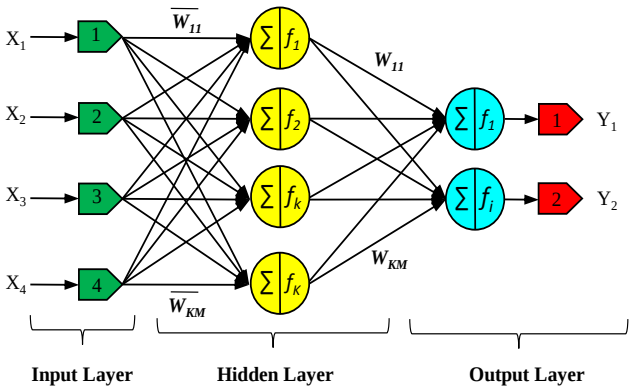

Figure 2. The structure of multilayer feed forward artificial neural network with one hidden layer

ANNs generally consist of three layers namely, an input layer, one hidden layer and an output layer. As the input layer accepts the input variables to ANN from environment, the output layer transmits the environment. The hidden layer is the section where the proposed nonlinear system is modelled using neuron cell mathematically. Each artificial neuron consists of five parts namely inputs, weights, bias, TF and output.

The general structure of neuron has been presented in Figure 3. Firstly, the input data I_1, I_2…..I_n are multiplied with their corresponding weights w_1, w_2…..w_n and then summed together. If the neuron has bias value then the x value has been reached by summing the obtained value with the bias value. The result has been fed in the transfer function and the obtained value; y has been transferred to the output.

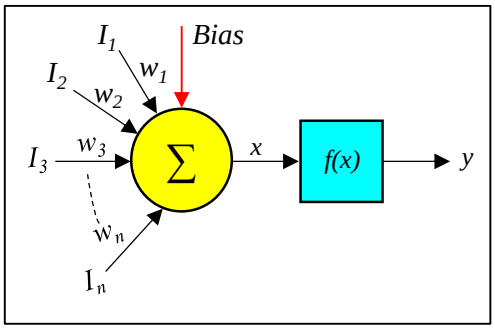

Figure 3. The general structure of neuron with bias

3. The numerical model of Sprott 94 S system

In general, chaotic systems are described with differential equations. The differential equations for Sprott 94 S [22] nonlinear autonomous system are given in Equation (1). In this equation, α and β are the system parameters and x, y and z are dynamic variables of this system. The variations in system parameters have changed the dynamic characteristic of the system [23]. For this reason, these parameters are quite important for determining the system behaviour. The Sprott 94 S system is simulated with the system parameters of α=-4.0 and β=1.0. The initial conditions of the system have been set $x_0=y_0=z_0=0.05$ for producing chaotic signals. The system is described by the following nonlinear Equation (1):

$$\begin{aligned} dx/dt &= -x(t) - \alpha \cdot y(t) \\ dy/dt &= x(t) + z(t)^2 \\ dz/dt &= x(t) + \beta \end{aligned} \quad (1)$$

The numeric simulation of the system has been executed using **Mat**rix **Lab**oratory (Matlab)-Simulink software for extracting the phase portrait of Sprott S system. The numeric simulation model of the system is presented in Figure 4.

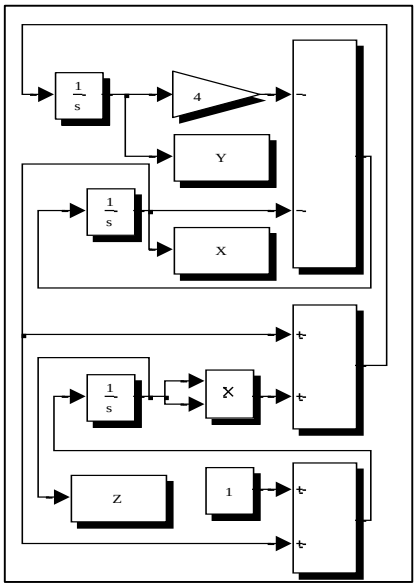

Figure 4. The Matlab-Simulink model of Sprott S system

The output graphic of Sprott S system obtained from Matlab-Simulink model is given in Figure 5. In addition, phase portraits of Sprott 94 S system were displayed in performing numerical simulation, as shown in Figure 5 for parameters of α =-4.0 and β=1.0 and initial conditions $x_0=y_0=z_0=0.05$. As shown in Figure, the system exhibits chaotic behaviour.

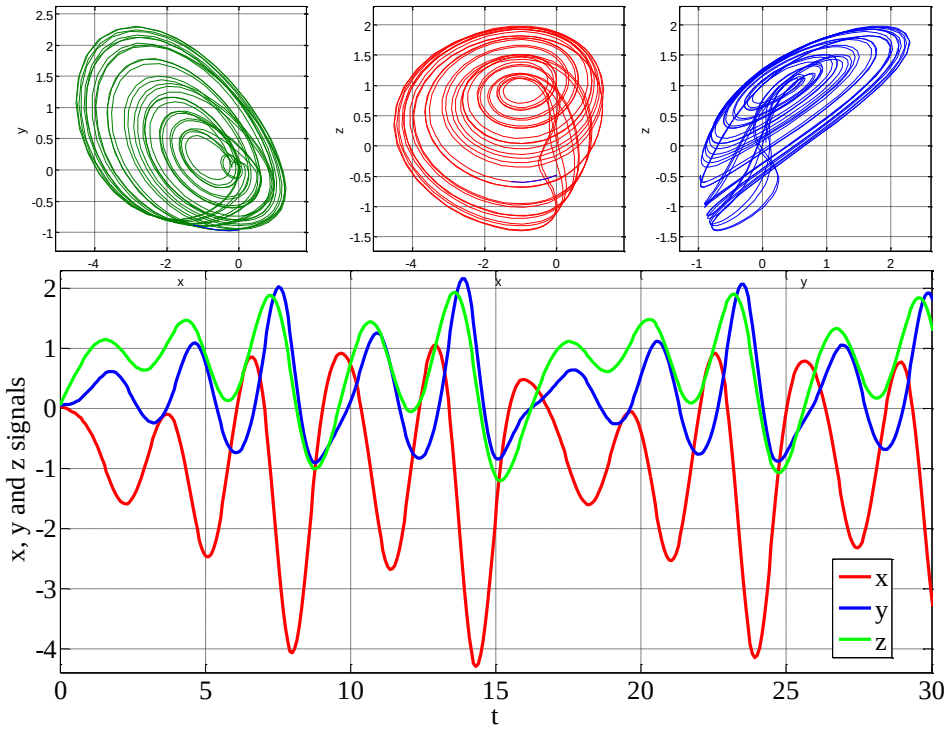

Figure 5. Sprott 94 S system: x, y and z time series and phase portraits obtained from Matlab-Simulink modeling results: x-y phase portrait, x-z phase portrait and y-z phase portrait

4. Discrete-Time ANN Based Implementation of Sprott 94 S System on FPGA

In this work, ANN-based Sprott 94 S system has been modelled using Matlab for implementing the discrete-time of the system on FPGA. For the ANN-based Sprott 94 S system, the structure of Feed Forward Multi-Layer Neural Network has been used. ANN-based system has 3 inputs and 3 outputs, respectively and pureline transfer function has been used for the output layer. The hidden layer has 7 neurons consisting Logarithmic Sigmoid (LogSig) transfer function which is one of the nonlinear transfer functions realized difficult by HW 10,000 samples have been generated by using fifth order Runge-Kutta-Butcher (RK-5-B) algorithm [24]. The generated samples have been divided into two groups: 8,000 samples for training and 2,000 samples for the test process. 100,000 epochs have been defined in training process with Levenberg-Marquardt (LM) algorithm. At the end of the training, the performance value (Mean Square Error (MSE)) has reached 2.30E-13. After the performed training and test processes, FPGA-based ANN has been evaluated using the obtained values of weight and bias coded inVHDL.

In the presented work, Look-Up-Table (LUT) and COordinate Rotation DIgital Computer (CORDIC) based approximations [25] have been united for the implementation of LogSig transfer function used in the hidden layer of ANN on FPGA. The calculations between the values of $-\pi/4$-$\pi/4$ in other words $e^{0.7853981}$-$e^{-0.7853981}$ are possible using the values of *Sinh(x)* and *Cosh(x)* generated by CORDIC unit. In the proposed work, the received values to transfer function can be calculated between e^{-48} and $e^{+47.25}$ using CORDIC-LUT-based approximation.

In Figure 6, the neuron structure used in hidden layer and FPGA-based multilayer feed-forward ANN structure have been given. The input values of X_{p1}, X_{p2} and X_{p3} have been multiplicated by the corresponding weight values $\overline{W_{11}}$, $\overline{W_{21}}$ and $\overline{W_{31}}$ using the units of *Mult1*, *Mult2* and *Mult3* on FPGA. Since these operations have parallel and pipeline processing scheme, the result of the first multiplication has been summed with the bias value for avoiding the latency process. Then, the obtained value by summing two intermediate values has been transmitted to LogSig transfer function.

The value of *-x* signal has been obtained with negation process for LogSig transfer function. After that, the obtained value has been divided by $\psi=0.75$ for degrading the value to be calculated by CORDIC unit and the obtained ψ value has been converted to fixed point number standard. The fractional (λ) and integer (ω) parts of the ψ value have been separated each other by transmitting to two pipeline channels. After the latency process, e^{ω} value which corresponds to ω, has been obtained from LUT. In the second pipeline part, the calculation of λ value has been performed using CORDIC, taken $\psi \geq \lambda$ into consideration. In here, first of all 2-bits have been added to the most significant bit (MSB) of λ (16-bit) for compability of ψ (18-bit). Then, the obtained value λ has been multiplied by ψ to send result value, τ to CORDIC unit. *sin(τ)* and *cos(τ)* have been transmitted to adder unit by calculating them in CORDIC unit. In there, e^{τ} value has been obtained by summing these two signals and has been sent to multiplier unit by converting to float-point standard. Then, the values of e^{τ} and e ω have been multiplicated to reach e^{-x} value. e^{-x} value has been summed with FP 1.0 value and the transfer function value of *LogSig(x)* has been calculated by dividing the obtained value into *FP 1.0* value (in 32-bit single precision IEEE-754-1985 floating-point number standard).

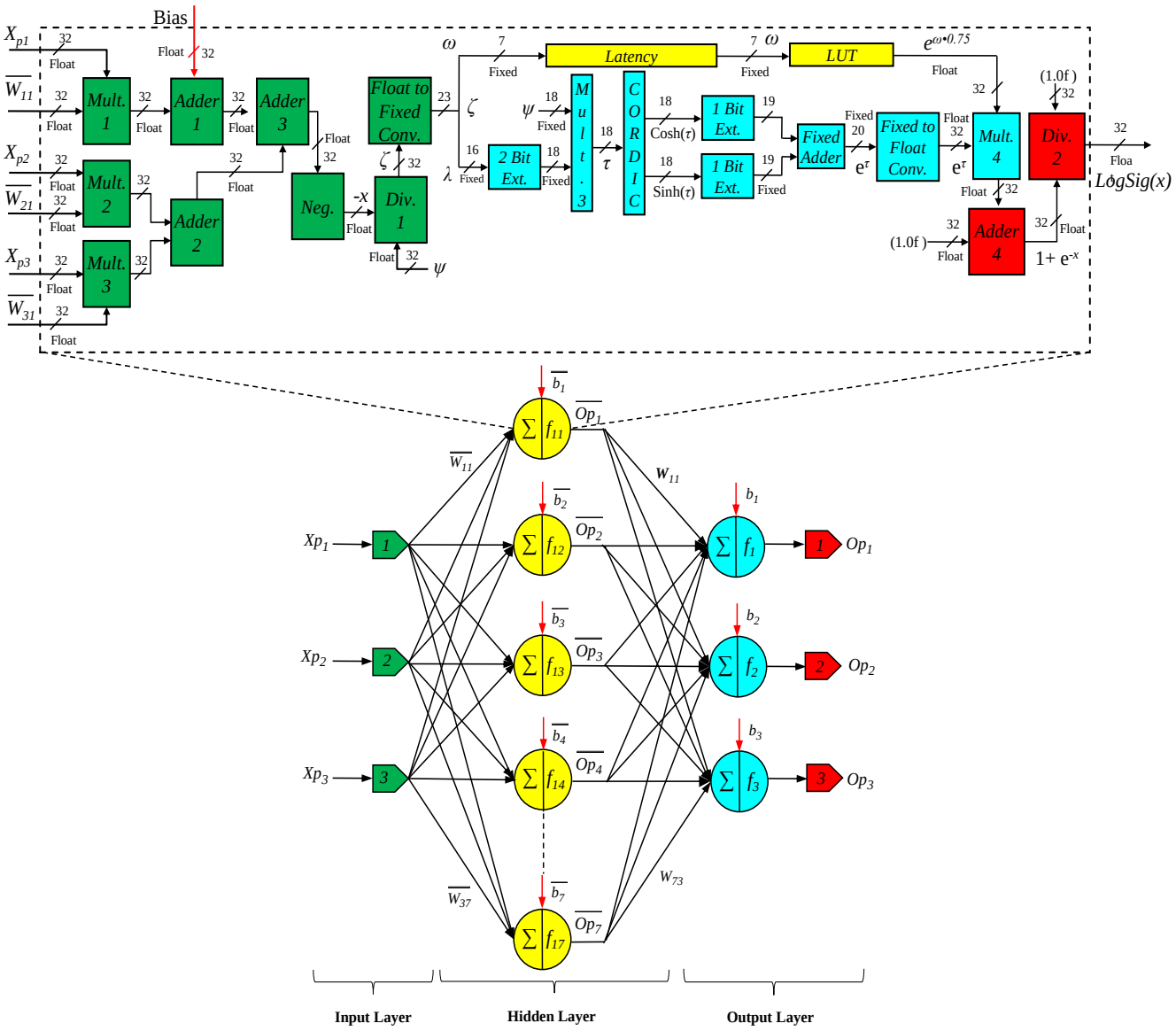

Figure 6. The neuron structure of hidden layer and FPGA-based Sprott 94 S system feed forward-multilayer ANN

ANN-based Sprott 94 S system on FPGA has been coded with VHDL. 32-bit IEEE-754-1985 single precision floating-point number standard has been used in the implementation. The Place&Route process has been performed by synthesizing with Xilinx ISE Design Tools (DTs) 14-1 simulation program for Xilinx Virtex–6 family XC6VHX255T-3FF1923 chip. The statistical parameters of clock speed and FPGA chip utilization summary have been investigated and given in Table 2. Furthermore the minimum pulse period of ANN-based Sprott 94 S system has been obtained 3.284 ns using Xilinx ISE DTs 14-1 simulation program.

The discrete time series results of *x*, *y* and *z* of the presented ANN-based Sprott 94 S system obtained from the implementation on Virtex-6 FPGA chip using Xilinx ISE DTs have been shown in Figure 7. Just after 137 clock cycle, ANN-based Sprott 94 S system produces the first outputs. After the first outputs, system outputs have been produced once per a 137 clock cycle. Although 32-bit IEEE-754-1985 floating-point number standard has been used in the design, the simulation results of Xilinx ISE Design Tools 14-1 have been shown in Hexadecimal number standard to examine the discrete time series of *x*, *y* and *z* more comfortable.

Table 1. FPGA chip utilization summary for the ANN-based Sprott 94 S system

Xilinx FPGA Chip	Slice Register Number	DSP48E1s Number	LUTs Number	Occupied Slices Number	Bounded IOBs Number	Max. Clock Frequency (MHz)
VIRTEX-6	75,551	7	76,308	23,278	195	304.534
%	23	1	48	61	40	--

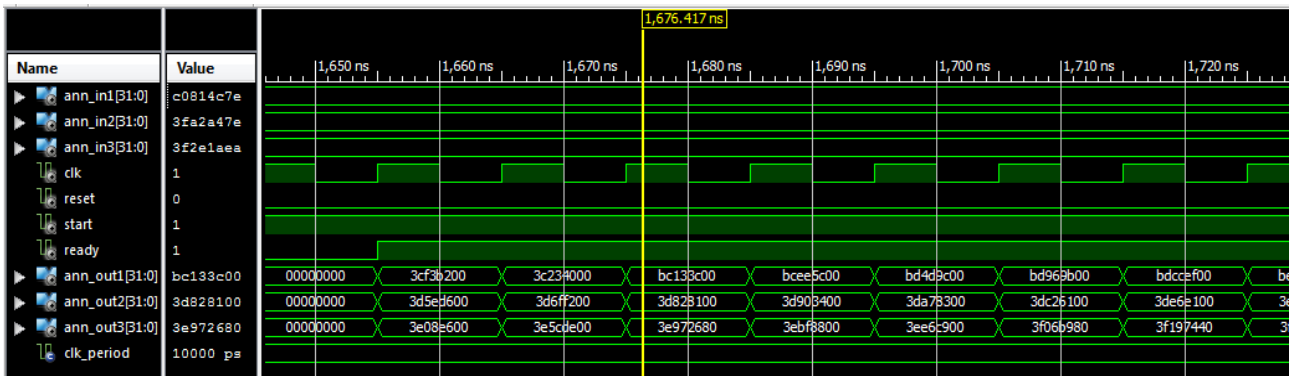

Figure 7. ANN-based Sprott 94 S system dicrete time series on FPGA

The binary values of the designed ANN-based Sprott 94 S system in 32-bit single precision IEEE–754-1985 floating-point number standard related to *x*, *y* and *z* discrete time signals obtained the implementation on Virtex-6 FPGA chip using Xilinx ISE DTs 14-1 have been saved in a file during the simulation test process.

After the conversion of the saved values to the real number system, the discrete time series produced by ANN-based Sprott 94 S system using the first 3x100 data set have been presented in Figure 8.

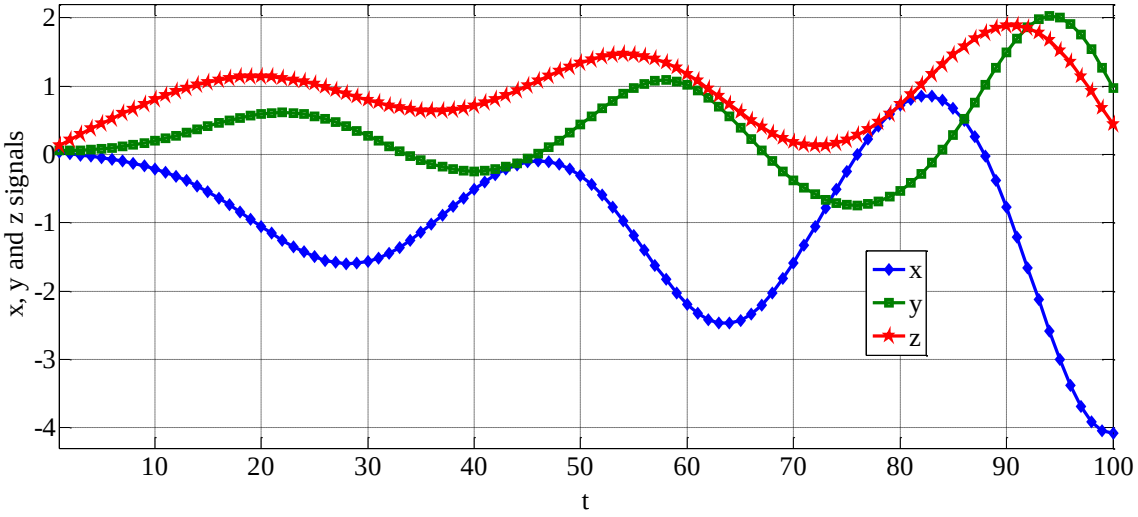

Figure 8. The discrete time series of ANN-based Sprott 94 S system designed on FPGA using Xilinx ISE Design Tools 14-1

The error analyses of **M**ean **S**quared **E**rror (MSE), **R**oot **M**ean **S**quared **E**rror (RMSE), **N**ormalized **M**ean **S**quared **E**rror (NMSE), **M**ean **A**bsolute **E**rror (MAE) and **M**ean **A**bsolute **P**ercentage **E**rror (MAPE) have been performed to specify the error rate of FPGA-based design constructed for ANN-based Sprott 94 S system using IEEE-754-1985 32-bit single precision floating-point number standard. RK5-Butcher algorithm has been selected as a reference in the performed error analyses studies and the first 3x100 data set generated from ANN-based Sprott 94 S system on FPGA has been used. The results of the obtained analyses have been presented in Table 2.

Furthermore, absolute error analysis results of ANN-based Sprott 94 S system implemented on FPGA have been presented graphically in Figure 9. According to obtained results, the minimum error value of *y* 2.37623E-06 and maximum error value of *y* 1.98885E-03 have been observed for 3X100 data set generated by ANN-based Sprott 94 S system.

Table 2. MSE, RMSE, NMSE, MAE and MAPE analysis of ANN-based Sprott 94 S system on FPGA

Signals	MSE	RMSE	NMSE	MAE	MAPE
x	1.369E-07	3.699E-04	1.231E-07	3.416E-04	2.148E-03
y	5.991E-07	7.740E-04	1.383E-06	6.253E-04	3.285E-03
z	4.314E-07	6.568E-04	2.172E-06	6.191E-04	9.921E-04

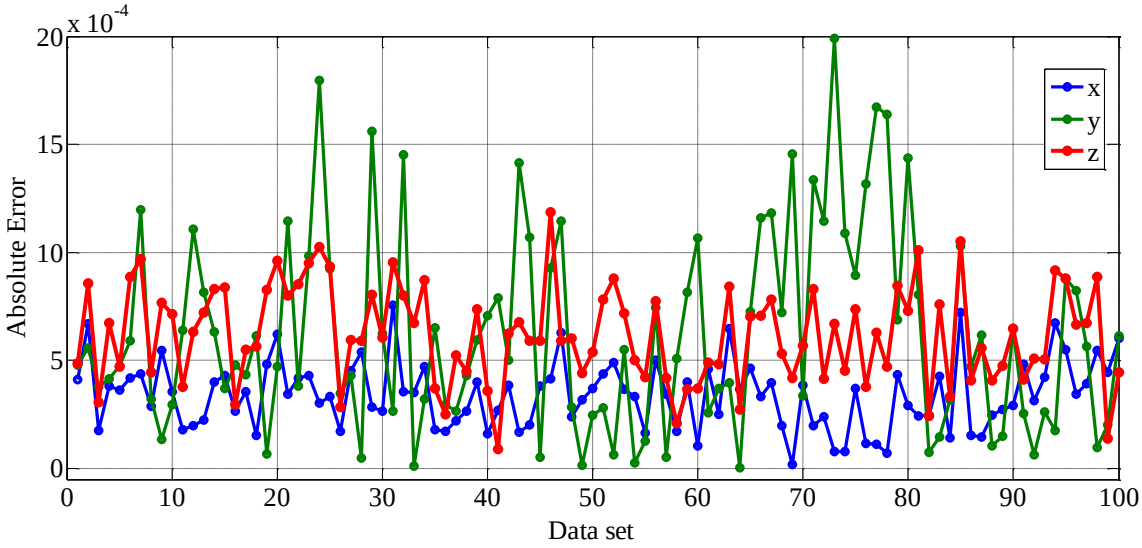

Figure 9. The absolute error analysis results of ANN-based Sprott 94 S system implemented on FPGA

5. Conclusion

In the presented work, nonlinear Sprott 94 S system has been modelled using the approximation of LogSig transfer function on FPGA. The performed modelling of ANN's architecture has been developed using VHDL with IEEE-754-1985 32-bit single precision floating-point arithmetic. The design of ANN-based Sprott 94 S system has been synthesized using Xilinx ISE Design Tools and tested using 3X100 data set. The error analysis results related to obtained tests have been presented. The performed design has been implemented with the Place&Route process for Xilinx VIRTEX-6 family, XC6VHX255T-3FF1923 FPGA chip and chip utilization statistics have been given. The ANN-based Sprott 94 S system having pipeline processing scheme on FPGA can be used with a clock frequency up to 304.534 MHz and ANN-based system has produced 3X3.284 billion outputs in 1 s. As further work, different nonlinear systems can be modelled using FPGA-based ANNs. Thus the performance and error analysis can be performed using obtained results. In future, embedded secure communication applications can be performed using the proposed ANN-based Sprott 94 S system on FPGA.

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