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A STUDY ON TEMPERATURE DEPENDENCE OF CURRENT TRANSPORT IN P^+PP^+ Si DEVICES

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SUMMARY

In this work, the current voltage (I-V) characteristics of p^+pp^+ devices prepared from p-type silicon having a resistivity of 11.50 Ω-m at the room temperature and grown in [111] direction are studied between 110-297 K. It is found that this structure obeys the Ohm's law at low voltages and the square law at high voltages. From the current voltage measurments it is seen that, at the Ohm' law region, the resistivity and, at the square law region, the hole mobility decreased with increasing the temperature. In order to change the temperature, a temperature control system and a cryostat are designed.

P^+PP^+ SI YAPILARINDA AKIM İLETİMİNİN SICAKLIĞA BAĞLILIĞI ÜZERİNE BİR ÇALIŞMA

ÖZET

Bu çalışmada, oda sıcaklığında 11.50 Ω-m özdirençli ve [111] doğrultulu p-tipi silisyumdan yapılan p^+pp^+ yapılarının akım - gerilim (I-V) karakteristikleri 110-297 K sıcaklık bölgesinde çalışıldı. Yapının düşük gerilimlerde Ohm kanununa ve yüksek gerilimlerde kare kanununa uyduğu bulundu. Ohm kanunu bölgesindeki akım-gerilim ölçümlerinden özdirencin ve kare kanunu bölgesindeki akım-gerilim ölçümlerinden de boşluk hareketliliğinin sıcaklık artışıyla azaldığı görüldü. Sıcaklığı düzgün bir şekilde değiştirebilmek için bir sıcaklık kontrol sistemi ve kroyostat düzenlendi.

INTRODUCTION

The current voltage (I-V) characteristics of space-charge-limited currents (SCLC) diodes established with applying the rectifying and ohmic contacts to the both sides of a silicon wafer showed that the current decreased with increasing the temperature in the SCLC region; so, it had indicated that the carrier mobility decreased with increasing the temperature [1,2] . Okazaki and Hiramatsu [3] pointed out the temperature dependences of the carrier mobility by measuring the I-V characteristics of the p^+pp^+ devices at various temperatures between 255-365 K prepared from the p-type silicon.

Various techniques for the determination of the carrier mobility and related references were given by Jacoboni et al. [4] . The temperature dependence of the mobility in p-type silicon had been investigated by Mitchel and Hemenger [5] at low temperatures between 20-50 K.

In this research, p-type silicon crystals having a resistivity of 11.50 Ω-m at the room temperature and grown in [111] direction are used and the p^+pp^+ devices established. The I-V characteristics of the structures are measured at the various temperatures between 110-297 K and the temperature dependences of the sample resistance and hole mobility are examined.

MATERIALS AND METHODS

1. Basic Equations

The current density in the syemetric p^+pp^+ devices is given with the relation.

$$J = e\mu_p pE - eD_p \frac{dp}{dx} \tag{1}$$

where e is the electronic charge, μ_p is the hole mobility, p is the hole density, E is the applied field and D_p is the diffusion constant for holes. As seen, the equation (1) contains diffusion and drift terms. Diffusion currents are approximately equal and have opposite direction because of the carrier density gradients in injecting contacts at the both sides of the sample. So, the diffusion term in the equation (1) can be neglected and by using the Poisson equation

$$-\frac{d^2\Psi}{dx^2} = \frac{dE}{dx} = \frac{e(p-N_a)}{\varepsilon\varepsilon_o}, \tag{2}$$

the current density is written as follows:

$$J = \varepsilon\varepsilon_o\mu_p E \frac{dE}{dx} + e\mu_p N_a E \tag{3}$$

where ψ is the potential function, N_a is the ionised acceptor density ε is the dielectric constant of semiconductor and ε_o is the free space permitivity. It is known that the current density given by equation (3) can be written as

$$J_\Omega = e\mu_p N_a \frac{V}{d} \qquad (4)$$

at low voltages and

$$J_{SCLC} = \frac{9}{8} \varepsilon\varepsilon_o \mu_p \frac{V^2}{d^3} \qquad (5)$$

at the high voltages [6], where V is the applied voltage to the structure and d is the width of p-region. According to equations (4) and (5), the structure gives the ohmic current which is proportional to the voltage at low voltage values and the SCLC which is proportional to the square of voltage at high voltage values.

As seen in equation (4), the temperature dependence of ohmic currents will arise from the hole mobility μ_p and the ionised acceptor density N_a. The temperature dependence of the mobility for the low doping is, theoritically,

$$\mu_p = CT^{-3/2}, \qquad (6)$$

where C is a constant and T is the absolute temperature [7]. The ionized acceptor density is given by

$$N_a = 2 \left(\frac{2\pi m_p^* kT}{h^2}\right)^{3/2} \exp(-E_f/kT) \qquad (7)$$

where m_p^* is the effective mass of hole, k is the Boltzmann's constant, h is Planck's constant and E_f is Fermi level measured from the top of the valence band. If the equations (6) and (7) are substituted into the equation (4),

$$J = 2C \left(\frac{2\pi m_p^* k}{h^2}\right)^{3/2} e\frac{V}{d} \exp(-E_f/kT) \qquad (8)$$

is obtained as a result. Accorting to the equation [8], the ohmic current density varies exponentially with T^{-1} and the increase of current.

The temperature dependence of SCLC, with respect to the equation (5), will simply arise from the temperature dependence of the mobility. It is strongly related with the scattering mechanisms of carriers. The hole mobility depeding on the temperature is

$$\mu_p = \frac{e\tau_p}{m_p^*} = \frac{\sqrt{8\pi}}{3} \frac{e\hbar^4 C_{11}}{m_p^{*5/2} k^{3/2} D_v^2} T^{-3/2} \qquad (9)$$

If the effective scattering only comes from lattice vibrations [7], where τ_p is the mean free time for holes, C_{11} is the longitudinalelastic constant of semiconductor and D_v is the deformation potential constant of the valence band. It is clear that the factor of $T^{-3/2}$ is equal to the constant C at the equations (6) and (8) given before. According to the equation (9), the mobility decreases with the increase of temperature and SCLC decreases with increasing the temperature.

The mean free time for the scattering from impurity atoms based on the scattering theory of the carriers by Coulomb potential of impurity ions. It is shown that the hole mobility in silicon reaches a constant value if the impurity concentration is less than 10^{22} m^{-3} [4]. Silicon crystal used in this research has a carrier density of 10^{19} m^{-3}.

2. Experimental Procedure

2. 1. The Sample Preparation

In the experiments, p-type silicon crystals are used which have resistivity of 11.50 Ω-m at the room temperatureand grown in [111] direction. The wafer thicknesses are reduced to aporoximately 80-100 μm by mechanic polishing by using SiC powder.Then, to remove the surface damages and the surfaca dirts, the crystals are chemi cally etched by CP-4 (2 part HNO_3 + 1 part HF + 1 part CH_3COOH). In order to establish p^+pp^+ devices, the metal Al (99.99 % pure) is evaporated to the crystal surfaces in the vacuum of 10^{-5} torr and Al/p-Si/Al system is annealed at the eutectic temperature [7] in the same vacuum.

2. 2. The Experimental System

2. 2. 1. The Temperature Control System

A block diagram of the temperature control system is shown in Figure 1. This system compares the thermocouple e.m.f. with the reference voltage (V_{RF}) and controls the heating unit. The circuit diagrams of the systems are given in Figures 2, 3, and 4. Figure 2 cotains the circuit of the power supply of ± 12 V, thermocouple amplifier and zero-voltage-dedector. Figure 3 is a circuit having the limitations between 2-7 V at 150 mA and avarages the power control signal. Figure 4 is a circuit of the heater power supply and it is controled by the circuit in Figure 3.

2. 2. 2. Cryostat

A diagram of the cryostat is shown in Figure 5. The connections to the sample, heater and thermocouple are made through the connect or at the top of the sample holder. More information about the experimental system is given by Tüzemen [8].

3. Experimental Measurments and calculations

A typical I-V characteristics of p^+pp^+ Si devices which are measured by clasical DC method at various temperatures are seen in Figure 6. There are two regions in these characteristics: the first, $I \alpha V$ region at low voltages, and the second, $I \alpha V^2$ region at high voltages.

At the first region, the I-V relation is given by Ohm's law and the inverse of V in the I-V relations will give the sample resistances (Table 1) which are worked out by using the linear regression method at various temperatures.

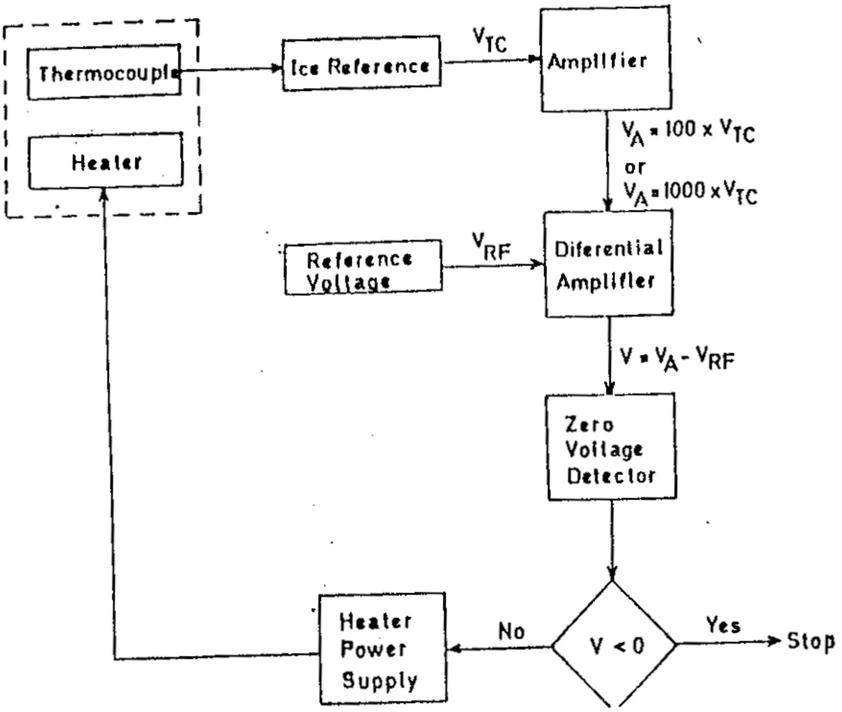

Figure 1. A block diagram of the temperature control system.

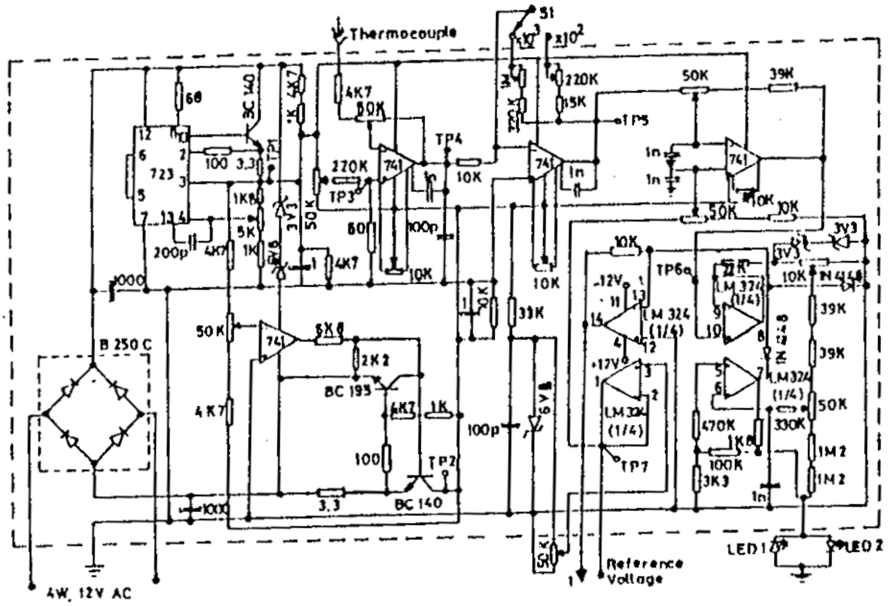

Figure 2. The circuit containes the power supply of ±12 V, thermocouple amplifier, diferential amplifier and zero-votage-detector.

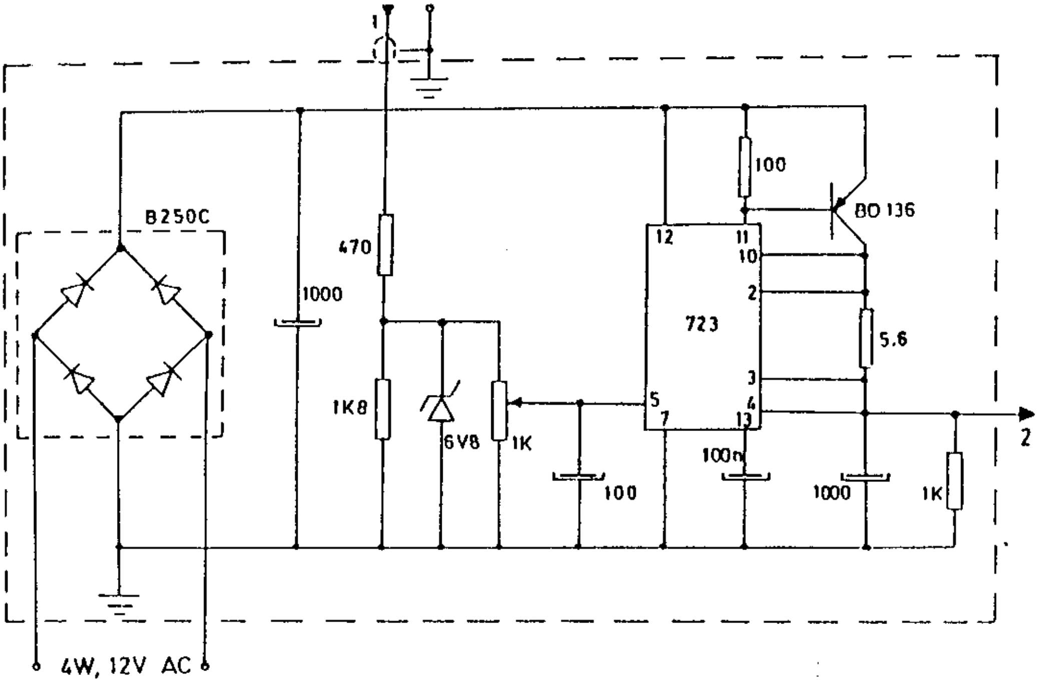

Figure 3. The power supply of 150 mA current limitations between 2-7 V which averages power control signal.

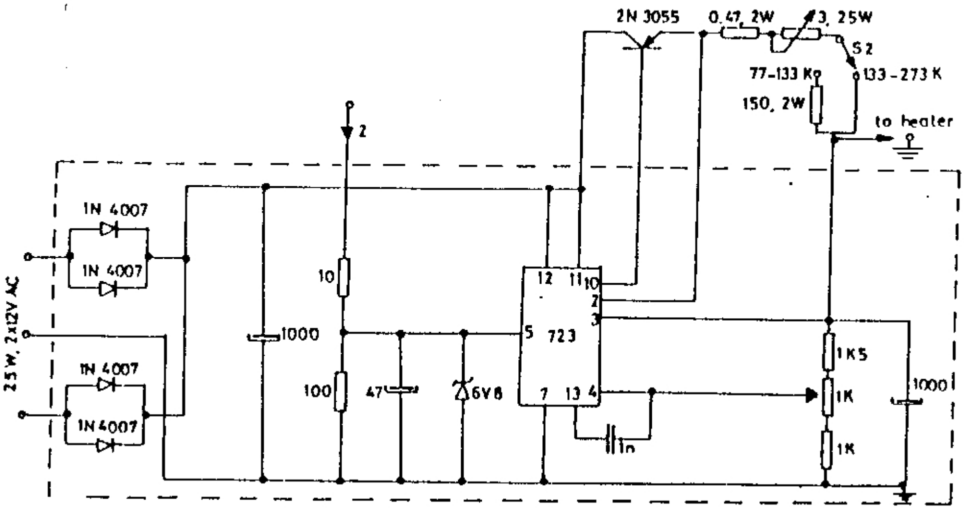

Figure 4. The circuit diagram of heater power supply.

Table 1

The I-V relations in the $I \alpha V$ region and the sample resistances for p^+pp^+ Si devices at various temperatures.

T(K)	I-V relations	R (Ω)
110	$I = -1.87\times10^{-7} + 4.66\times10^{-5}V$	21436 ± 30
181	$I = -1.067\times10^{-7} + 6.734\times10^{-5}V$	14850 ± 10
263	$I = -1.08\times10^{-7} + 8.20\times10^{-5}V$	12197 ± 5
297	$I = -2.21\times10^{-7} + 1.90\times10^{-4}V$	5258 ± 5

The I-V relation at $I \alpha V^2$ region is theoritically given by

$$I = A \frac{9}{8} \varepsilon\varepsilon_o\mu_p \frac{V^2}{d^3} \tag{10}$$

where A is geometric area of the sample. If we take the square roots of both sides of the equation (10), we have the relation

$$\sqrt{I} = (A \frac{9}{8} \frac{\varepsilon\varepsilon_o\mu_p}{d^3})^{1/2} V \tag{11}$$

where the cofficient of the voltage, from which the hole mobilities of the sample at various temperatures (Table 2) is calculated using the values $A = 7.06\times10^{-6}$ m^2, $d = 37$ μm, $\varepsilon = 11.8$ [7] and $\varepsilon_o = 8.85\times10^{-12}$ F/m^2, is obtained by linear regression method.

Table 2

The $\sqrt{I}$-V relations in the $I \alpha V^2$ region and the hole mobilities for p^+pp^+ Si device at various temperatures.

T(K)	$\sqrt{I}$-V relations	μ_p(cm^2/V-s)
153	$\sqrt{I} = -3.15\times10^{-3} + 3.89\times10^{-2}V$	925 ± 10
181	$\sqrt{I} = -2.99\times10^{-3} + 3.80\times10^{-2}V$	879 ± 10
263	$\sqrt{I} = -5.47\times10^{-4} + 3.09\times10^{-2}V$	582 ± 5
297	$\sqrt{I} = -4.27\times10^{-4} + 2.67\times10^{-2}V$	431 ± 5

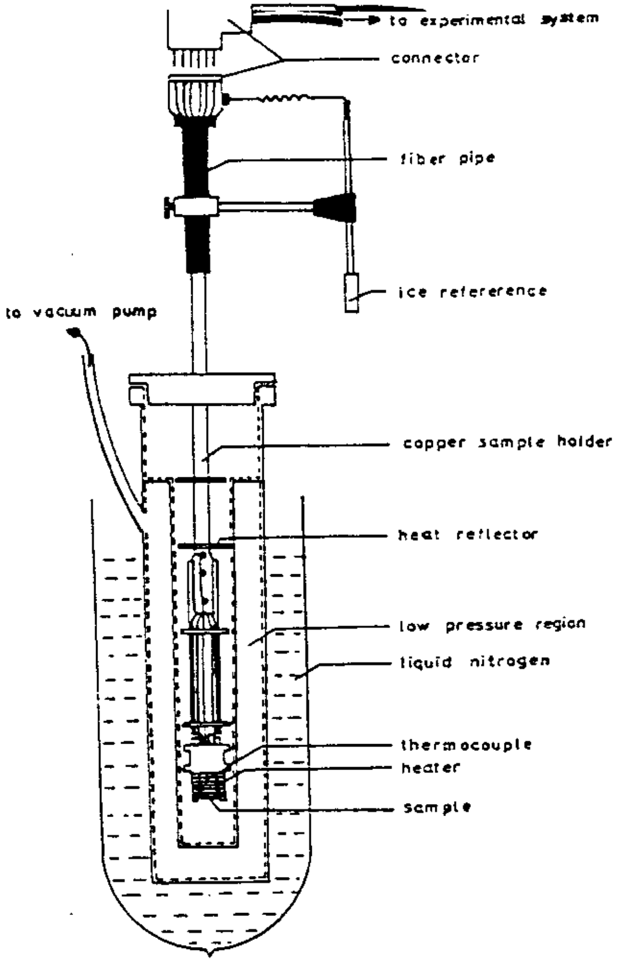

Figure 5. The diagram of cryostat.

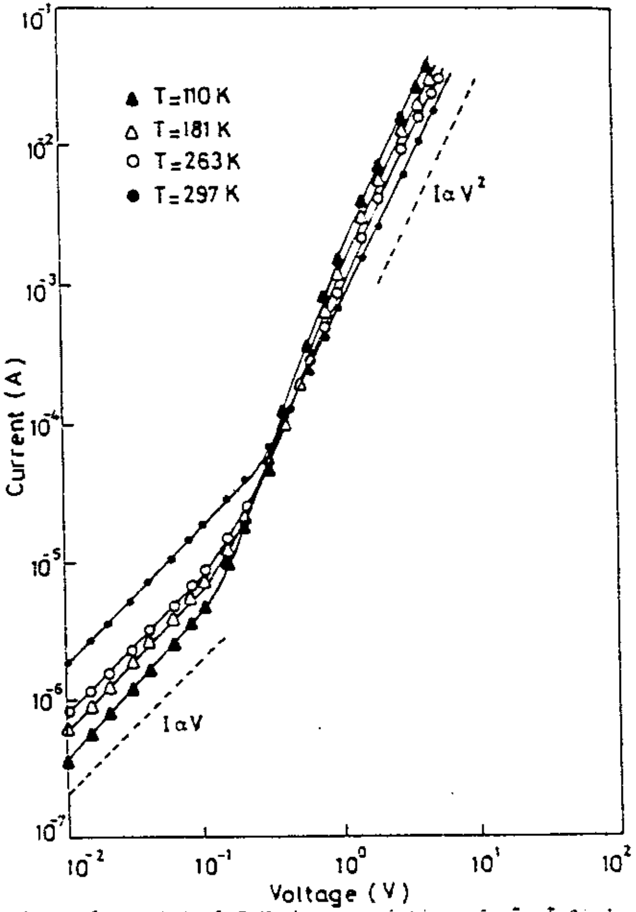

Figure 6. A tipical I-V characteristics of p^-pp^+ Si device at some selected temperatures. The diode area and the thickness are $A = 7.05 \times 10^{-5}\ m^2$ and $d = 37\ \mu m$, respectively.

DISCUSSION

The I-V measurments of symmetric p^+pp^+ devices show that they behave like a resistance obeying the Ohm's law at low voltages and obey the square law at high voltages. The transition to square law region from the Ohm's law region is sharp at a certain voltage. The current, in the region obeying the Ohm's law is increased with increasing the temperature and in the region obeying the square law is decreased with increasing the temperature as seen in Figure 6. These properties of the I-V charecteristics are in good agreement with the theoritical considerations.

The knowledge about the sample resistance and the effective carrier density causing the current transport can be obtained from the $I \alpha V$ region of the charecteristics. In this region, the carrier density increases and the sample resistance decreases at higher temperature as shown in Table 1. In the $I \alpha V$ region, if we accept all the carriers coming from the ionized acceptors, we can write current in a from as

$$I = A \frac{e\mu_p p}{d} V \tag{12}$$

where p is the free carrier density. So, the sample resistance is

$$R = \frac{d}{Ae\mu_p p} . \tag{13}$$

Where the hole mobility $\mu_p = 431\ cm^2/V.s$, electronic charge $e = 1.6x10^{-19}$ C, sample thickness d = 37 μm and R = 5258 Ω at the room temperature (Table 1) are substituted into equation (13), the hole density which is effective at the current transport is found as $p = 1.44x10^{17}\ m^{-3}$. This result is less than the thermal hole density $p = 1.21x10^{19}\ m^{-3}$ found from the value of the sample resistivity $\rho = 11.50$ Ω-m. The reason of the difference can be explain with the small transport probability of carriers at tunneling to the narrow barrier consisting of grain boundaries during the alloying (9). Because the carriers have small energies at the ohmic region. Thus, the number of the carriers which contibute to the current transport are low.

At the $I \alpha V^2$ region, the decrease of the current with increasing the temperature can be explain by means of the decrease of the mobility with increasing the temperature because of the I - V relation (10). The temperature dependence of the mobility is mostly related with the scattering processes in the crystal. In this work the scattering comes from lattice vibrations because of the low impurity concentrations in the crystal. At high temperatures. the scattering effects increase because of the lattice vibrations and the mean free scattering time τ decreases. The mobility is described by $e\tau/m^*$ and the decrease of τ leads to the decrease of the mobility. The values of the mobility calculated from the I - V charecteristics are given in Table 2 at various temperatures. μ_p is equal to 925 ∓ 10cm^2/V.s at 153 K, and 431 ∓ 5cm^2/V.s at 297 K. The values of the mobility at the room temperature (287 K) is good agreement with values given in the literature [3,4].

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