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Research Paper

Design of Power and Area Efficient Carry Skip Adder and FIR filter Implementation

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Abstract: Adders are used in processing units such as Arithmetic and Logic Units (ALUs) as an essential building block, and in many blocks of microprocessor chips critical path, adders occupy an important place. Hence reducing power, area and increasing the speed of adders are significantly important. This paper proposes a modified structure of Carry Skip Adder (CSKA) with a reduction in consumption of power and area without affecting the speed when compared with the conventional adder structures. In order to get better effectiveness of the modified CSKA by including concatenation, incrementation schemes, and variable latency for the proposed hybrid structure, which reduces the power utilized without affecting the operating speed of the adder. The modified structure in CSKA helps in improving the slack time, which further reduces the voltage with the parallel structure. Experimental results show that the 32-bit implementation of the proposed adder has a significant power reduction of 42% and 38.3%, area reduction of 27%, and 18.3% with respect to Conventional CSKA and CI CSKA adder with a little over ahead in delay. The proposed adder is used to implement a 5-tap FIR filter which shows a significant reduction in power consumption and area.

Keywords: Carry Skip Adder, Power Consumption, FIR, Binary to Excess Code convertor.

1. Introduction

Adders are a significant unit in ALU operation for improving the performance of the processors, i.e., increasing the speed and reducing the energy consumed considerably may affect the processor performance [1]. It is fascinating to accomplish high speed by utilizing low power/energy seems to be an excellent test for the inventors of general-purpose processors [2]. Anyone can select any type of adder among the different adder structures/families to reduce the power and increase the speed [3]. The additional adders with various delays, area, and consumption of power like Parallel Prefix Adders (PPAs), Ripple Carry Adder (RCA), Carry Select Adder (CSLA), Carry Increment Adder (CIA), etc. With reduced area and power consumption, the RCA is a modest structure but has the worst critical path delay [4]-[16]. CSLA has high speed, power consumption, and area is also increased compared with RCA [18]-[21]. The PPAs quickly generate carry similar to carry look-ahead adder. Based on the algorithms used and performance, the PPA structure is classified [22]. It has to be understood that the PPA structure has more complexities than any other adder structure, including the kogge stone adder [23]. The importance of power reduction of CMOS VLSI circuits is explained in [24]-[25]. The carry skip adder affords cooperation between an RCA and a CLA. The carry skip adder splits the words to be inserted into blocks. Inside each block, RCA produce carry

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and sum bit [26]. Reduction in consumption of power and area usage, CSKA is considered an effective adder[27].

CSKA structure seems to have attractive features when compared to other adders. The proposed adder structure uses binary to excess-1 code converters (BEC) of n bit. The main advantage of using a BEC converter instead of RCA in the proposed adder is the area and power consumption are reduced without affecting the addition speed.

2. Existing Carry Skip Adder technique

Figure 1 shows M-bit existing -CSKA Ripple carry adder in each stage.

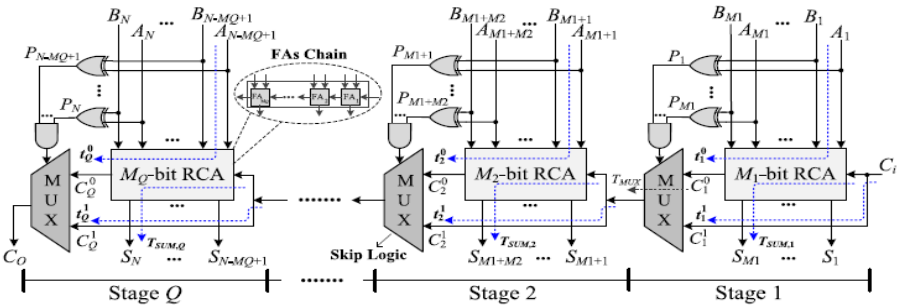

Figure 1 Structure of M-bit Conventional CSKA [1]

Considering the process of the concatenation of full adders (FA) in every stage, there will be a skip in the carry logic. In RCA, there are N number of Full Adders connected having larger propagation delay for adding two M-bit numbers A and B, So the worst case delay is given by

$$P_i = A_i \oplus B_i \quad \text{i= 1, . . . , N} \qquad (1)$$

Pi is called propagate term, as shown in equation (1).

CSKA, in each stage, has to carry input in skip logic (multiplexer) and the carry output (FA chain) in the Ripple Carry Adder block. The propagation signals, which are used as the selection lines in the multiplexer, are generated at the product of each stage, as represented in figure 1.The fixed size stage(FSS) and variable size stage(VSS) are used to implement the CSKA, which produces high-speed operation for the VSS structure, and the stage size used is similar to the RCA block.

3. Proposed CSKA Structure

The CSKA is used in various computational framework designs to direct the propagation delay occurring due to carry, which is skipped to generate the sum over the carry blocks. Ripple carry adder independently (for Cin=1 and 0) is used by CSKA to produce the resulting sum. Nonetheless, the CSKA, which is normally used, doesn't enhance the features of area and speed because of using multiple combinations of RCA for generating fractional sum and carry by considering input carry. Multiplexers select the final carry and sum of CSKA. Therefore, by using two independent RCAs will increase the area and also leads to an increase in delay.

The problem said above can be addressed by using n-bit BEC converters. In CSKA, replacing RCA with BEC will provide lesser area usage and reduced delay, improving the addition process's speed. One advantage is fewer gates will be used than the FA structure, so the number of gates is

decreased. Figure 2 shows the proposed design of the 32-bit CSKA structure. This logic can be used to implement any adders in the modified design. Figure 3 represents the logic of 3-bit RCA with BEC.

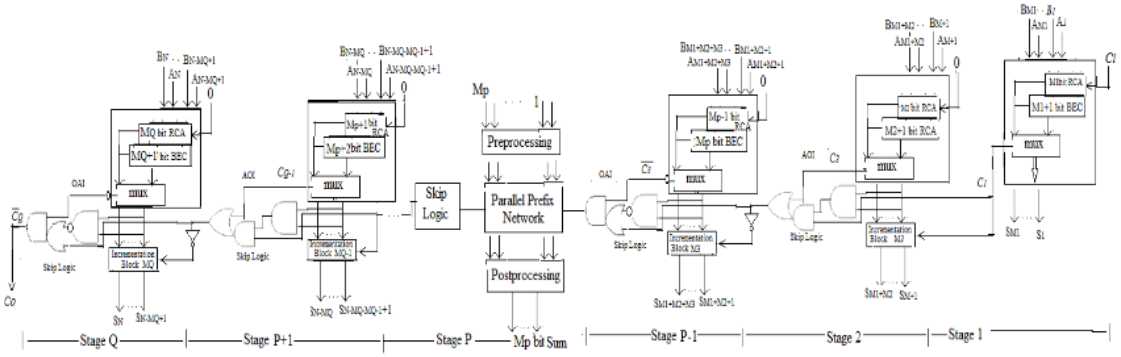

Figure 2. Proposed adder circuit

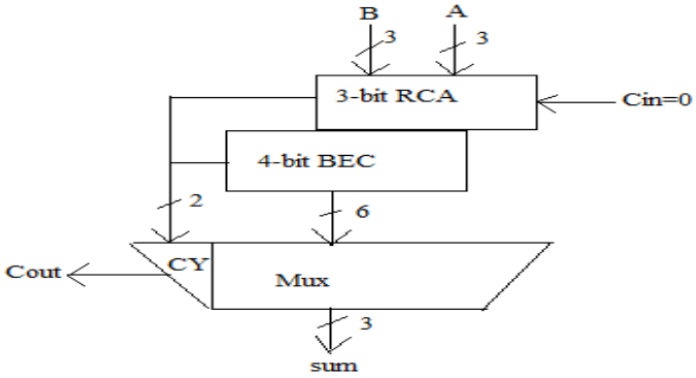

Figure 3. 3-bit RCA With BEC

In regular CSKA structure, for 3-bit RCA, two independent RCA blocks for Cin=1 and Cin=0 are used. The proposed area-efficient CSKA uses the RCA block with BEC, as shown in figure 3. Here RCA logic is replaced with BEC logic.

3.1 BEC concept

Figure 4. illustrates the basic function of the CSKA and its implementation using a multiplexer and 4-bit BEC. Two inputs are applied to multiplexer B0, B1, B2, and B3 are one set of inputs, and the output of BEC is the other set of inputs. The output of the multiplexer is selected by using Cin. Based on Cin's value, the multiplexer will select 4 bits, either B0 to B3 or the output of BEC. The main advantage of using Binary to Excess three Code converter is to reduce the number of transistors by area of the chip while designing a large number of CSKA adders.

The carry skip adder's various structures are implemented using TANNER EDA software. The proposed implementations are shown in Figure 5.

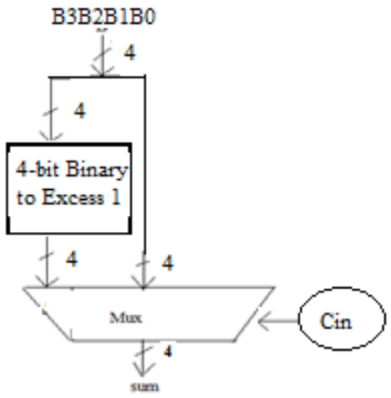

Figure 4.BEC structure for 4 bit.

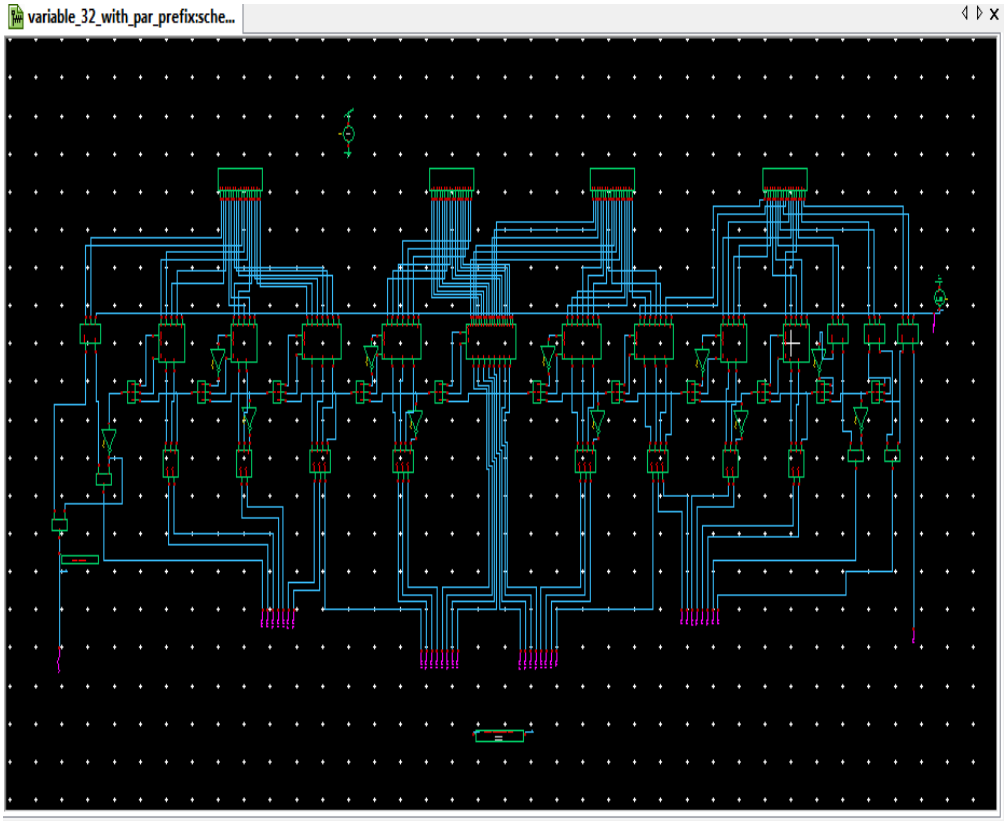

Figure 5. Structure of Proposed Adder using tanner tool.

4. Results and Discussion

Table 1 provides a proposed adder to the input patterns applied details. The sum and carry of the CSKA are generated by applying the inputs. TANNER EDA Tool is used for implementing the proposed adder, and power and delay were calculated. The number of transistors used determines the area occupied in this design. The comparison of Concatenation & Incrimination CSKA and hybrid variable latency CSKA with area efficient CSKA in terms of power, delay and area for the input pattern is given in Table 2.

Table 1. Proposed adder input patterns

LSB to MSB Bits	7	6	5	4	3	2	1	0
A	10110	10110	10110	10110	10110	10110	10110	10110
B	10110	10110	10110	10110	10110	10110	10110	10110
LSB to MSB Bits	15	14	13	12	11	10	9	8
A	10110	10110	10110	10110	10110	10110	10110	10110
B	11111	11111	11111	11111	11111	11111	11111	11111
LSB to MSB Bits	23	22	21	20	19	18	17	16
A	10110	10110	10110	10010	10010	10010	10010	10010
B	00000	00000	00000	00000	00000	00000	00000	00000
LSB to MSB Bits	31	30	29	28	27	26	25	24
A	00000	00000	00000	00000	00000	10110	10110	10110
B	11001	11001	11001	11001	11001	11001	11001	11001

Table 2. Comparison among different structures for 32-bit

	Structure of adders		
Parameter	**CSKA**	**CSKACI**	**Proposed Adder**
Power(mW)	53.3	50.4	30.9
Delay(ns)	43.6	43.7	43.9
Area(transistor count)	3270	2938	2386

Table 2 compares the performance of CSKA, CSKACI, and the proposed adder. The proposed adder has a reduction in power consumption and area compared with the existing CSKA structures but with a slight increase in delay.

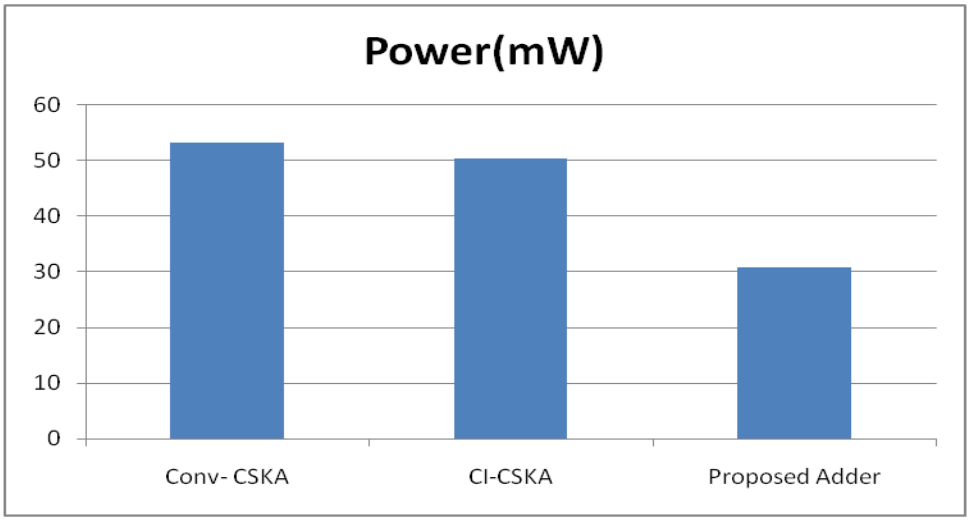

Figure 6. Power consumption comparison of existing and proposed adder

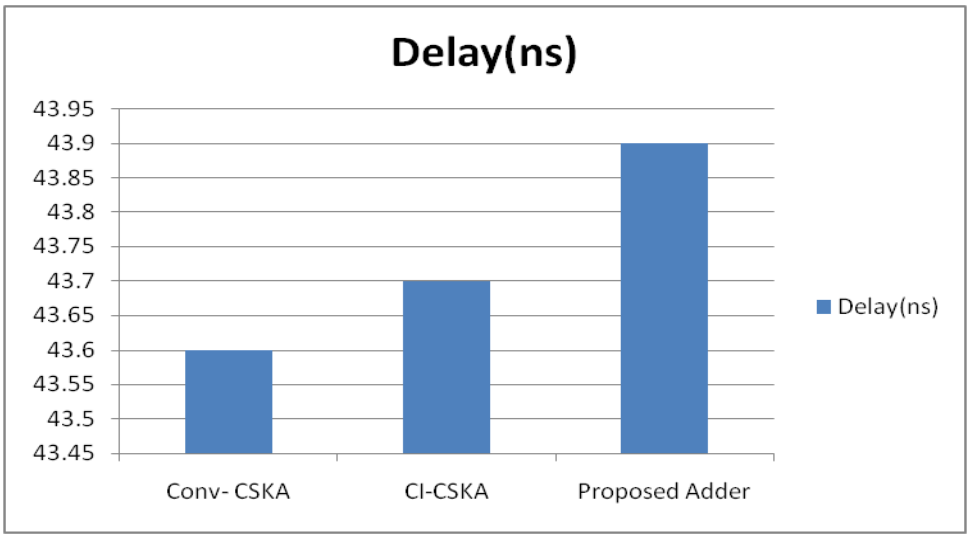

Figure 7. Delay comparison of conventional CSKA and proposed adder

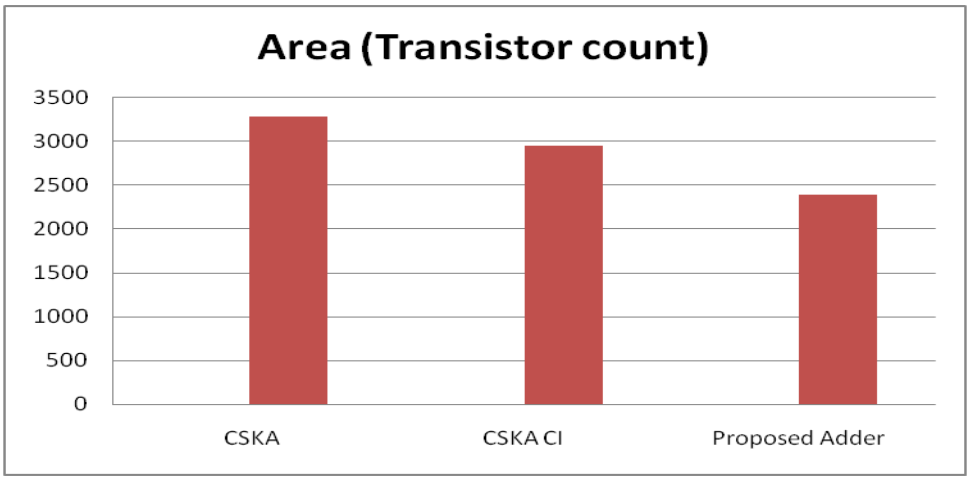

Figure 8. Comparison of Area in transistor count

Figure 6 and Figure 8 show a comparison of power consumption and area of the existing method and proposed method in which the proposed adder power consumption and area are reasonably lower than the existing methods. Figure 7 shows the comparison of the delay of the existing method and the proposed method in which the proposed adder delay is slightly higher than the existing method.

5. Implementation of FIR filter using proposed adder

The proposed adder is used in the adder unit of FIR to design the 5-tap FIR filter. Figure 9 shows the schematic implementation of the 5-tap FIR filter.

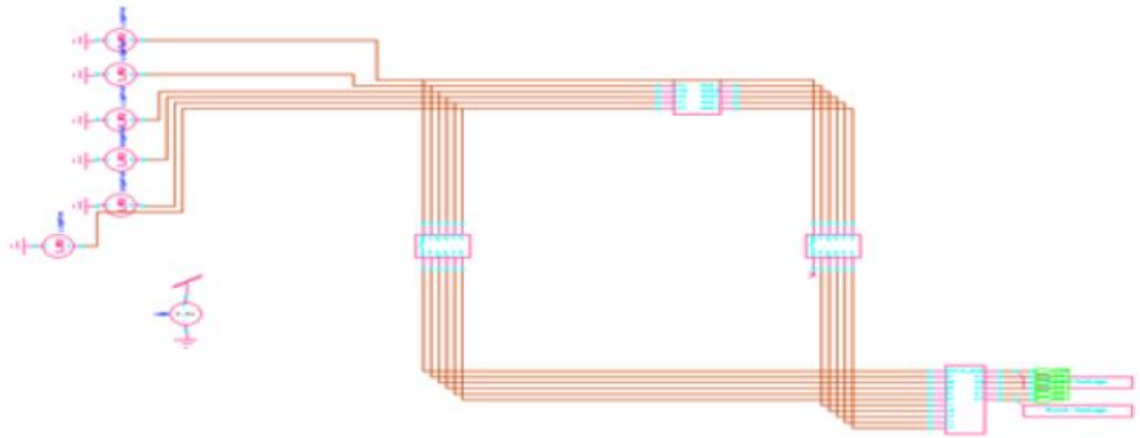

Figure 9. Schematic of 5 tap FIR filter using proposed adder

Table 3. Comparison between FIR Filters implementation

Different structure/ Parameter	FIR Filter Using Existing CSKA	Proposed adder
Power(mw)	0.194	0.183
Area(Transistor count)	852	840

6. Conclusion

An area-efficient CSKA was proposed by modifying hybrid variable latency CSKA. It exploits the customized parallel adder model at the middle stage, which provides an opportunity to reduce the area and power consumed by using n-bit binary to excess-1 code converters (BEC). Comparing the proposed method with the existing method, the proposed method has a slight increase in delay with a significant reduction in power and area. The proposed adder size of 32-bit is implemented using the tanner tool, and a comparison of results shows considerable power reduction of 42% and 38.3%, area reduction of 27% and 18.3% for conventional CSKA and CI CSKA adder with a little over ahead in delay. The over ahead is delayed due to additional logic circuits. The proposed adder shows a power reduction of 7.4% percentage and the area in the number of transistors is 1.4% while using the proposed adder to implement a 5-tap FIR filter.

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Authors' contributions

VG,CE and SD designed the the adder structure. VG implemented the structure in EDA tool. VG carried out simulation work, implemeted the FIR structure using adders, in collaboration with CE and SD, VG,CE and SD wrote up the article.

All the authors read and approved the final manuscript.

Competing interests

The authors declare that they have no competing interests.

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