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Research Paper

Fault Analysis and Compensation in a Five Level Multilevel DC-AC Converter

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Abstract: Existing Neutral clamped active (NCA) inverters have the property of high frequency common mode voltage, which can reduce the severity with less voltage gain. A newly designed five level (5L) NCA inverter can capable have achieved voltage step-up with a one stage inversion process. The proposed circuit common ground enhances DC link voltage usage while also mitigating common mode voltage with high frequency. The proposed topology is more compact and has less voltage stress than the conventional two stage topology. The proposed circuit contains merely seven power switches and two capacitors, whereas the conventional topology has ten switches and three capacitors, resulting in a more efficient layout. The proposed topology is developed in the simulink platform, and the simulation results are validated in a proto-type model with a power rating of 2000 W to validate its feasibility and performance with fault clearance capabilities.

Keywords: Neutral clamped active (NCA) inverter, 5-Level, common mode voltage, high frequency mitigation, Total Harmonic Distortion

1. Introduction

Power electronic circuits are primarily designed to convert energy from one form to another at a specific voltage level, allowing import/export to the power grid [1-3]. In this power conversion scenario, researchers design or identify various types of power converters which are highly suitable for the specific applications. Solar energy power conversion-based applications require a transformer-less DC-AC converter to avoid circuit bulkiness, reduce electromagnetic interferences (EMIs), and increase gain [4-8]. Isolation between the DC source side and the AC load side is required in DC-AC conversion circuits to avoid leak current emission and more common mode voltage gain issues [9-12]. The issue of high frequency common mode voltage gain in non-isolated transformer topologies is receiving a lot of attention. The literature survey presents specific modulation techniques with clamping circuits to control inverter topology. In the market, neutral clamped active inverters are highly preferred [13]. The alternating current output is connected in the DC link midpoint known as neutral, and a capacitor is clamped on it to prevent leakage current [14-17]. The disadvantage of the NCA Inverter bridge is its low voltage gain; a portion of the dc link voltage will appear across the AC terminal. As shown in Fig. 1, a conventional five-level converter has a two-stage structure with boost conversion operation, but the drawback is that double the AC voltage is required to achieve dc link voltage. Researchers have recently attempted to combine an NCA inverter with a switched capacitor to improve voltage gain [18-20]. To increase the voltage, the gain of the circuit switched capacitor connected in series with the DC link capacitor is discharged at the same time. For supplying load while charging from the supply, the same capacitor is connected in parallel with DC link capacitor. These topologies have two stages, current spikes, and more components.

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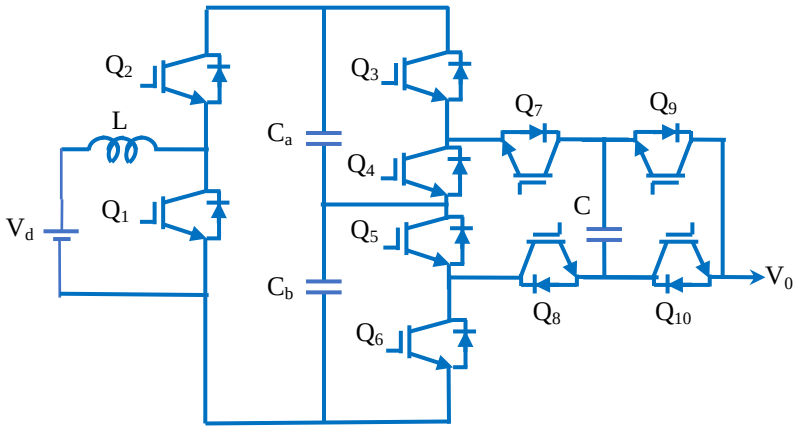


Figure 1. Conventional 5-level converter

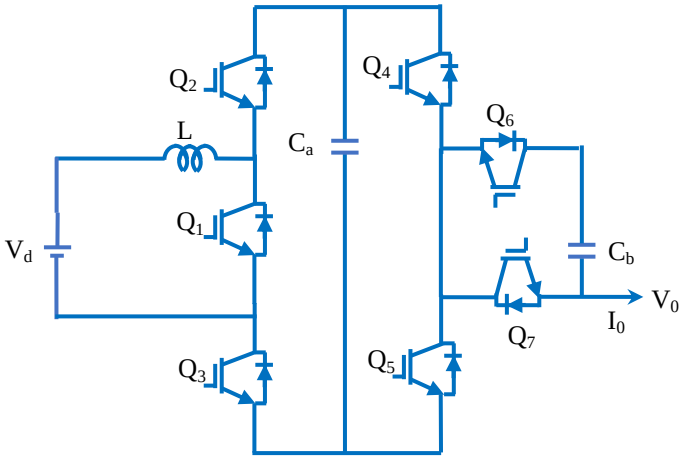


Figure 2. Proposed 5-Level converter

Figure 2 illustrates a new one stage level NCA inverter with voltage step-up capability that provides a solution while also overcoming the drawbacks of conventional two stage topology. The proposed converter has the advantage of reducing the number of switches from ten to seven, requiring only two capacitors, and increasing the dc link voltage usage. Low cost, increased efficiency, and reduced voltage stress are additional benefits. The use of a common ground to reduce or control leakage current and voltage step-up with a single stage is a significant benefit. This paper is organized with V sections; mathematical analysis with modes of operation is reported in section II, A comparisons made between existing and proposed topology is reported in section III. Implementation of the proposed system in both simulation and hardware level is reported in section IV and finally concluded in section V.

2. Modes of Operation

Proposed 5L-NAC with common ground step-up inverter topology is implemented for voltage step-up 5L ac voltage production from one stage operation is as shown in Fig. 2.

From the comparison between conventional and proposed topologies numbers of components are reduced to enhance the conversion efficiency. To increase the utilization of dc link voltage and control common voltage with high frequency a common ground is used in between ac and dc sides. Because of this arrangement dc link voltage and ac voltage are equal; this voltage is double the

times than conventional inverter. Modes of operation are explained with eight circuits which is as shown in Fig. 3. Proposed concept has a control scheme is based on pulse width modulation with a level-shifted operation (PWM-LS). PWM-LS consist of two switching parts such as signal generator and state generator.

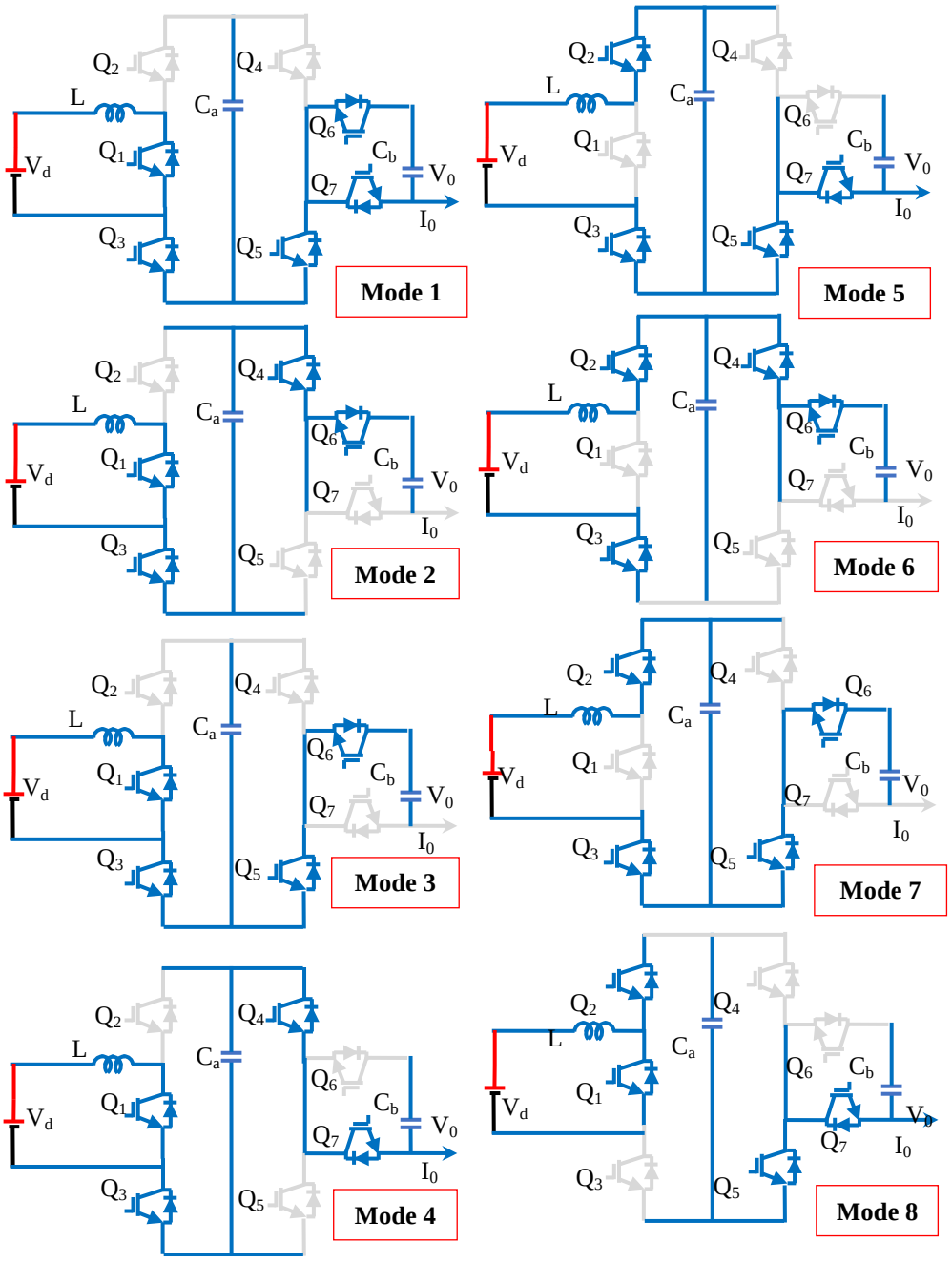


Figure 3. Modes of operation

DC link voltage with AC voltage made decoupling control is realized for comparing constant reference with top triangular carrier for producing duty cycle which increases voltage level. Step-up component L is charging by constant (δ) duty cycle, and the step-up voltage across C_a is expressed as

$$V_D = \frac{V_d}{1-\delta} \tag{1}$$

Capacitor Cb voltage is controlled automatically at 50% of the voltage. 5L of voltages are generated between $+V_{dpeak}$ to $-V_{dpeak}$. Peak AC voltage is given as

$$V_{0,1} = \frac{V_d}{1-\delta} \tag{2}$$

Where modulation index = M, considering duty cycle δ as minimum, A_v is voltage gain is given as

$$A_V = \frac{V_{0,1}}{V_d} = \frac{M}{(1-M)2} \tag{3}$$

Proposed circuit operation controlled by PWM-LS scheme. T_1 and T_{mean} are calculated from current waveform

$$T_1 = \frac{T_0}{2\pi} sin^{-1}\ \frac{M1}{2M} \tag{4}$$

$$T_{mean} = \frac{1}{2\pi f_0} sin^{-1}\ \frac{I^1 C_a}{I_{0,1}} \tag{5}$$

Change in voltage of capacitor, electric charge is given by

$$\Delta V C_b = \frac{I_{0,1}}{C_b \pi f_0}\left[1 + \frac{\pi}{2M} - 2\cos\left(sin^{-1}\frac{1}{2M}\right) - \frac{1}{M}\ \ sin^{-1}\frac{1}{2M}\right] \tag{6}$$

Capacitor voltage ripple of high frequency component and low frequency component is derived as

$$\Delta V C_a, f_s = \frac{\Delta I^1 C_a}{C_a, f_s} \tag{7}$$

$$I^1 C_a = \frac{I_{0,1}}{M\pi^2}[\pi(3M-1) + 2(1-2M\ \ sin^{-1}\frac{1}{2M}] \tag{8}$$

3. Topology Comparison

This comparison is useful to evaluate the advantages of proposed inverter over conventional inverter. Voltage gain and voltage in dc link are generalized in Fig. 4(i).

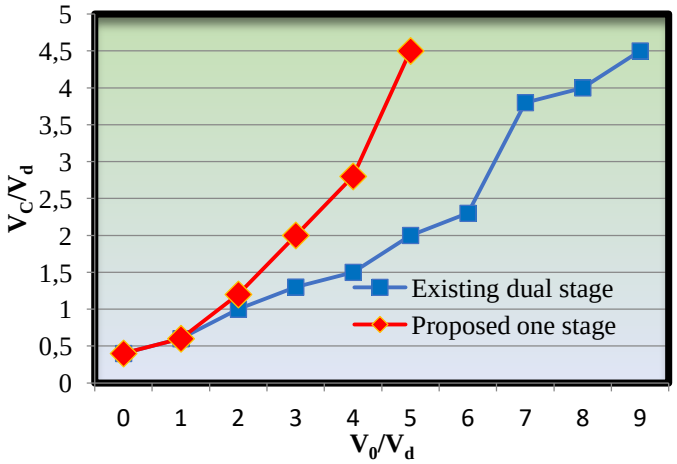


Figure 4 (i). Voltage gain comparisons

While considering AC voltages from same dc source, voltage gain produced from both topologies are same. Proposed converter having the features of more dc link voltage utilization, lower voltage stress and total standing voltage is less which is shown in Fig. 4 (ii).

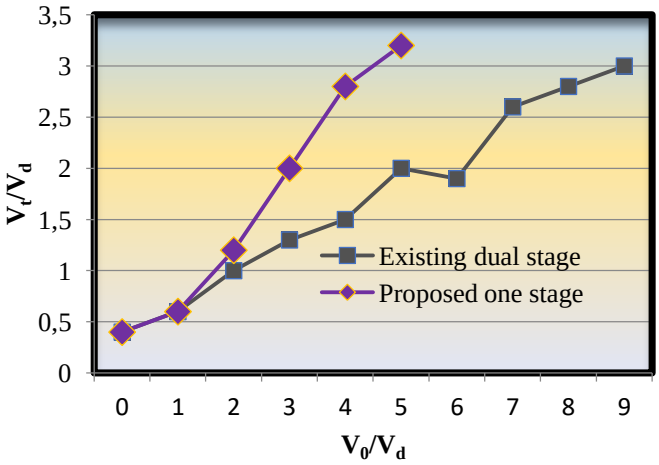
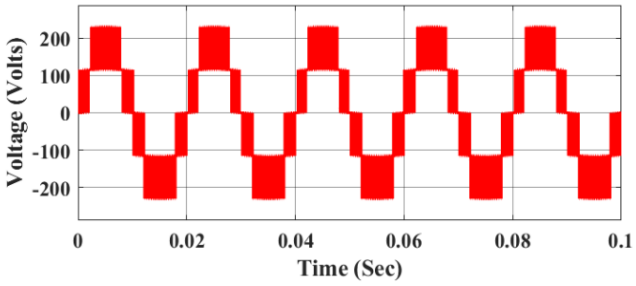
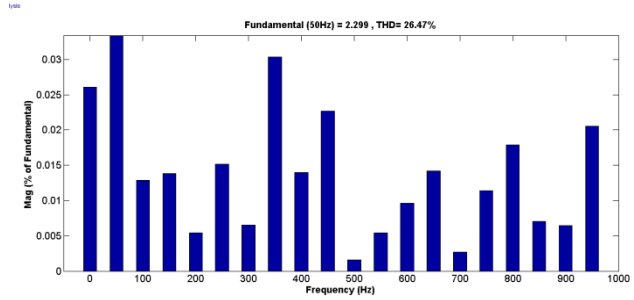


Figure 4 (ii). Voltage stress and total standing voltage comparisons

In both the conventional and proposed converters, the input 100V DC is converted to 230V AC, and the simulation waveform is recognised. Based on these comparisons, the proposed converter required less DC link voltage than the conventional topology, as well as more voltage ripple in the flying capacitor during capacitor C_b charging and discharging at fundamental frequency. Since the impact of filter component output, total harmonic distortion (THD) is slightly higher during C_b self-balancing. The proposed topology concentrates the triangular carrier frequency in order to control the harmonics, similar to the existing topology. Both conventional and proposed methods eliminate common mode voltage at high frequencies, as shown in Figs. 4(iii) (a) and (b).



(a)



(b)

Figure 4(iii). (a) Five level output (b)THD value

The existing common mode voltage is greater than 300V, and the frequency oscillates, whereas the proposed topology has fewer ripples, which control the common mode voltage. The proposed

topology is also more efficient due to the limited number of components in the circuit with one stage, as shown in Fig. 4. (iv). Table 1 compares the various components with existing topologies.

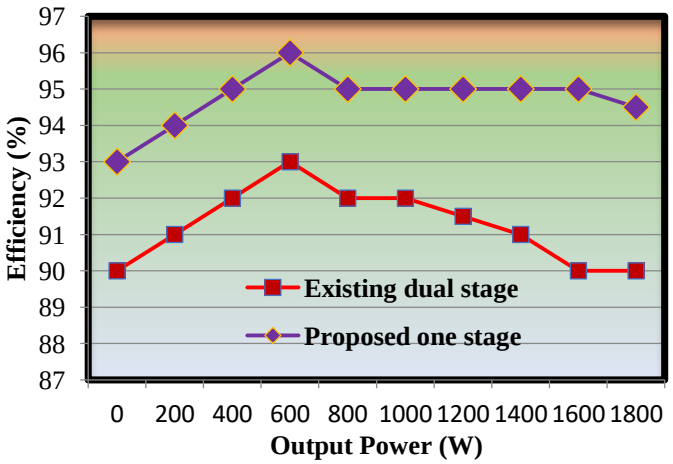


Figure 4 (iv). Efficiency Versus Output power comparisons

Table 1. Components and parameters comparison

Parameters	[16]	[17]	[18]	[19]	Proposed converter
Switches	7	8	9	7	7
Diodes	2	-	-	8	7
Capacitors	3	3	3	3	2
Inductor	1	1	1	1	1
Switching stress	High	High	Low	High	Low
Max. switch voltage	110	110	200	200	200

Power losses in the other components are estimated to be around 1kW, as well as switches have used the power. Aside from cost, the proposed topology meets some important parameters such as the number of switches, capacitor, DC link voltage usage, efficiency, and voltage stress.

4. Experimental results

Figure 5 illustrates proposed work experimental setups under normal, fault, and after fault conditions. The hardware setup comprises two circuits, one for normal operation and one for compensation operation. In the absence of a fault, the normal input and output waveforms are as shown in Fig. 6. Two critical parameters stand out: voltage levels at no loss and voltage ripples at post-fault conditions. During a fault condition, there is a loss of levels in either the positive or negative half cycle because the corresponding switches have failed, as shown in Figs. 7 and 8. Within two seconds, the same set of switches will be compensating for the faults. This fault compensation has been handled by the compensation circuit. Current loss as well as voltage, voltage of capacitor may increase or decrease depending on the faulty switches However, once the fault is remedied by the standby circuit, the capacitor voltage will return to normal due to self-balancing of voltage capability.

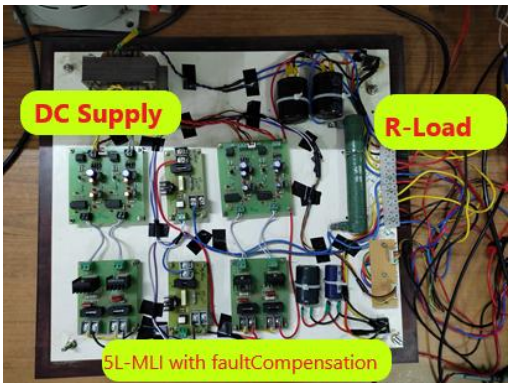


Figure 5. Experimental setup

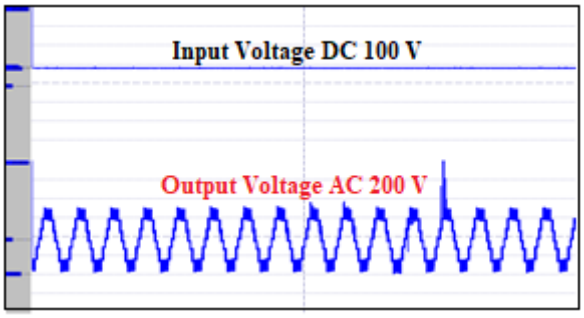


Figure 6. Normal input and output voltage

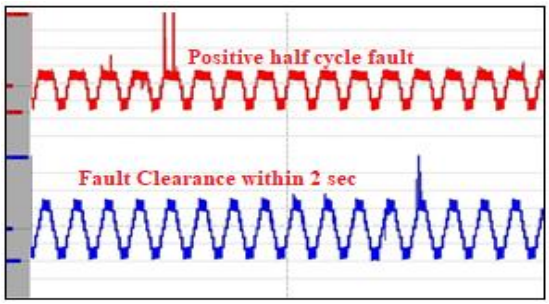


Figure 7. Positive half cycle fault and clearance

The magnitude of the sinusoidal load current is nearly 1.8A. Furthermore, the current is calculated and obtained in exercise using an impedance of 100 ohm and an input AC voltage of 180 V. The theoretical and practical voltage gains are approximately equal to 5. The obtained theoretical and practical results are nearly equal, as shown in Figs. 4 and 8. The experimental results and negative fault clearance obtained from the proto type model are shown in Fig. 8. In the prototype model, the load is R, and the load has been changed instantly without affecting the AC voltage.

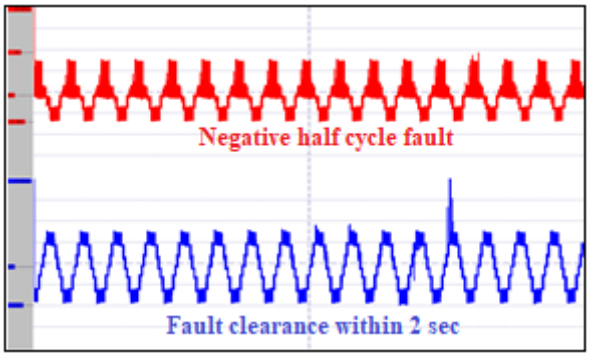


Figure 8. Negative half cycle fault and clearance

The number of devices or components used in the proposed topology versus the existing topology is used to make comparisons and discuss the findings. This comparison is based on full fault tolerance (FFT), half fault tolerance (HFT), and no fault tolerance (NFT). Table 1 illustrates comparisons between multilevel DC-AC converters. The topology from references [16, 17] have been withstand a fault from an open circuit with less output power, and the proposed circuit can withstand both short and open circuit conditions. In contrast to the existing topology, which requires two capacitors and has higher voltage ripples after faults, the proposed concepts only require one capacitor and maintain normal voltage ripples while fault tolerant. Because the number of sources required for the operation is limited, the circuit is more cost effective. The [18] topology requires more capacitors and switches, and it cannot withstand fault conditions. The circuit concept of [19] necessitates a greater number of DC sources than the proposed topology. Voltage block on many switches on the inverter legs during fault conditions may result in capacitor voltage exceeding 50% of V_d. As a result, proposed topology has found fault quickly.

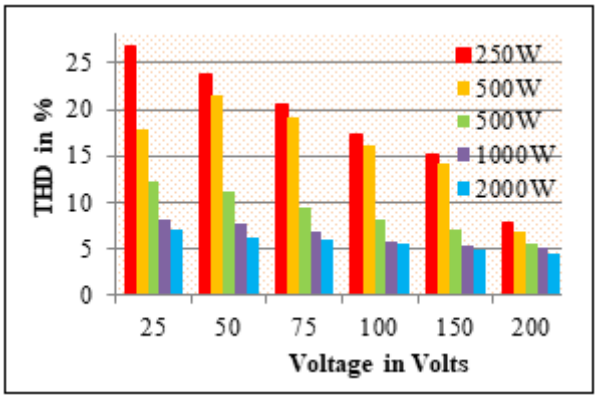


Figure 9. THD values from different power

Table 2. Comparitive analysis of various parameters

Parameters	Traditional converter	Proposed converter
DC side voltage	100 V	100 V
Frequency	50Hz	50Hz
Power output	200W	300W
Switching frequency	50KHz	50KHz
Efficiency	96.9%	97.9%
THD full load	12.6 - 18.3%	5.4 - 16.3%

THD obtained value is 4.5% in both modes of operation if output power is greater than 60%. The prototype converter's THD value of 2.3% has been achieved with specifications of 20V and 250W. Table 2 shows a comparison of the traditional and proposed converters [12]. The proposed converter with prototype model outperforms the traditional converter in terms of efficiency and THD. In Fig. 9, THD values for various power levels are expressed. It is clear that the proposed converter can achieve a significantly higher efficiency than the conventional converters. The proposed converter and the conventional converter both have calculated detailed power loss failures of their active switches.

5. Conclusion

In comparison to the existing topology, the proposed topology has been developed with fewer capacitors and a single DC source for fault-tolerant operation. For fault conditions with half fault tolerance and full fault tolerance, two ideas are proposed. During normal operation, the proposed topology produces stiff voltage by implementing the proposed control strategy for output voltage

increases as shown in simulation and hardware analysis. To compensate for the disadvantages of the proposed half fault tolerant topology level losses, capacitor ripple increases after the fault, allowing the full solution to find the same type of output as normal conditions. The hardware analysis on both short and open circuit faults from the components is provided to validate the concepts proposed.

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Authors' contributions

The authors confirm contribution to the paper as follows: study conception and design: PE, SK, data collection: PE, SK; analysis and interpretation of results: PE, SK; draft manuscript preparation: PE. All authors reviewed the results and approved the final version of the manuscript.

Competing interests

The authors declare that they have no competing interests.

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