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Quantum Transport Properties of InAs NWFET with Surface Traps

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Highlights:

- Field effect mobility value of 250 cm^2/V.s
- On/Off current ratio of 2
- Effect of surface traps on structure is crucial to optimize device transport properties

Keywords:

- Nanowire FET
- Quantum transport
- Surface traps
- Quantum conductance
- Ballistic transport
- Device modeling

ABSTRACT:

The quantum transport properties of InAs nanowire field effect transistor (NWFET) have been calculated and analyzed depending on the surface trap concentrations. Surface traps can be either impurity atoms, dangling bonds or structural deformations. Here, we have left some In and As atoms unsaturated to obtain surface traps. Our calculations show that the on-state voltage increases as the surface trap concentration increases. Within an equivalent circuit model, we have found that the effective field mobility is as low as 250 cm^2/V.s following with small transconductance value of 2.4 nS for our simulated device. This shows that surface traps significantly effect the benchmarking properties of InAs NWFET.

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INTRODUCTION

The modern integrated circuit technology has been evolved in terms of performance, capacity and speed as transistors are downscaled. Since downscaling has its own physical limits governed by mostly quantum mechanics, structures like nanowires and nanotubes are introduced as novel solutions for future high-performance transistors. In particular, nanowires with channel lengths shorter than the mean free path of the carriers can have ballistic transport. In turn, carriers can transmit along the channel without any scattering, resulting in minimal voltage drop. Since ballistic transport can also enable to utilize all available electronic channels in the electronic bands, it provides the ultimate conductance for a transistor. Recently, ballistic transport of electrons in top gated InAs nanowire (NW) transistors with dimensions of 30–75 nm diameter and 20–30 mm long has been shown with mean free path of carriers as much as 150 nm at room temperature (Chuang et al., 2013). However, the growth process of nanostructures involves irreversible mechanisms governed by thermodynamics. Therefore, surface traps can be formed at the stage of growth. These surface traps can be either impurity atoms, dangling bonds or grain boundaries, all of which play a crucial role due to effecting nanotransistor transport characteristics (Hasegawa, 2000; Bryllert et al., 2005; Lynall et al., 2018). Moreover, these surface traps might cause nanotransistor to work in specific region of current-voltage curve. Especially dangling bonds at the exterior surface of NWs change the electronic properties dramatically due to charge transfer within the structure. To prevent these changes, the NWs are immersed into chemical solutions in order to saturate these dangling bonds. In addition, the transport and electronic properties of nanowires strongly depends on its radius, cut plane and constitutions (Huang et al., 2002; Cui et al., 2003; Zhu, 2017; Lee et al., 2018). Especially, III-V semiconductor NWs have been shown to have superior FET characteristics in various gate geometries (Huang et al., 2002; Dayeh et al., 2007; del Alamo, 2011). In particular, InAs NWFETs can have ballistic or nearly ballistic transport with promising transport properties. Although the field effect mobility in InAs NWs is much lower than the bulk mobility (33000 $cm^2V^{-1}s^{-1}$) due to surface scattering within traps (Dayeh et al., 2007). But it is still higher than the value of accumulated free-electron gas (2000-3000 $cm^2V^{-1}s^{-1}$) on the InAs surface. Moreover, surface-states due to dangling bonds or other surface effects can induce new electronic bands that alter the electronic characteristics of the device. Even more, these surface states can exhibit 2-dimensional (2D) electron gas character or 1D character, because of localization of the charges at specific locations on the surface (Hasegawa, 2000).

Also, InAs NWs allow straightforward formation of low-resistance ohmic contacts. Thus, implementing InAs NWs in FETs is a promising way for nanoelectronic applications such as spin-orbit qubits (Nadj-Perge et al., 2010) and bio-chemical sensors (Tseng et al., 2017).

Furthermore, InAs NW provides an excellent system for studying electronic transport influenced by surface states.

Experimental evidence demonstrates that the presence of surface trap states at the interface of top-gated InAs NWMOSFETs has a significant impact on the transconductance properties, including carrier mobility and gate transconductance. This effect is primarily attributed to the slow charging and discharging of surface states. Surface state charging is a common phenomenon as the charges of surface states are balanced by opposite charges in the available electronic states. Consequently, the behavior of NWFETs is modified as a result of the repositioning and redistribution of these charges.

The effect of surface trap concentration in InAs [110] growth direction along the InAs (110) plane, NW FET on transport properties has not been fully studied for that given geometry and dimensions yet by means of quantum mechanical methods.

In this study, we first consider the electronic and structural properties of InAs nanowire cut from (110) plane of InAs bulk. The cross section of an InAs NWFET cut from the (110) plane exhibits a hexagonal geometry. At first, In and As atoms located at the surface of the nanowire have been saturated with hydrogen atoms to ensure sp^3 hybridization of these atoms. The structural and electronic properties of this pristine and fully saturated InAs nanowire have been calculated via ab initio methods. After elucidating the electronic and structural properties of pristine InAs NW with growth direction [110], we have explored the quantum electronic transport properties of InAs NWFET built by doped InAs electrodes and InAs channel with surface traps.

To introduce surface states along the channel of the InAs NWFET, some hydrogen atoms are removed and dangling bonds are left unsaturated up to a certain concentration.

Doping of InAs NW electrodes has been carried out by adding charges to the electrodes explicitly. The 5.4 nm long drain and source regions have charges corresponding to 10^{20} /cm^3, which is reasonable for real applications. Typically, the doping level mentioned falls within the experimental range commonly employed for doping in diverse semiconductor technology applications (Schubert, 1993, p. 40, 173, 176, 204).

After constructing the InAs NWFET made of only InAs NW, we have structurally optimized the whole structure while allowing the FET cell size to change and relax in transport z-direction.

Quantum transport properties of InAs NWFET have been calculated based on this fully relaxed FET structure at atomic scale both with and without surface states. Therefore, we have analyzed and compared the quantum transport properties of the InAs NWFET depending on the existence of surface states with various concentrations by means of ab initio calculations.

We also present a circuit model corresponding to the simulated device to extract device transport characteristics. Full atomic scale structure of InAs NW and InAs NWFET with its circuit model has been shown in Figure 1.

We have unveiled that the trap concentration has a clear effect on transport properties. Threshold voltage (V_{TH}) gets higher for higher concentrations of surface traps. Because, surface traps have electronic states close to fermi level (E_{f}) in the band structure of the InAs NW. Field-effect electron mobility (μ_{FE}) values have been found to be significantly lower than the NWFETs' reported in Table 2.

MATERIALS AND METHODS

Our InAs nanowire has been cut from an InAs bulk of (110) plane. Since electronic and structural properties of nanowires strictly depend on the wire radius, we have designed InAs nanowire with 7.5 Å radius having 74 atoms in a unit cell.

Electronic and structural properties of InAs nanowire have been calculated using the unit cell given in Figure 1.

Since we have cut InAs nanowire from InAs bulk, the unsaturated bonds have been formed at the surface of InAs nanowire. Moreover, these unsaturated bonds make electronic structure of InAs nanowire metallic rather than semiconductor.

Thus, we initially saturated dangling bonds of In and As atoms with H atoms at the surface of InAs nanowire to prevent structural and electronic degradation. To find structurally optimized unit cell of InAs, we conducted a comprehensive calculation for the optimization of all atoms involved.

After ensuring the structural and electronic properties of InAs with growth direction [100] nanowire, we have constructed a FET comprising of doped InAs nanowire and a semiconductor channel with partially unsaturated bonds as shown in Figure 1. To introduce partial unsaturation within the channel, we intentionally eliminated certain H atoms, allowing specific atoms to remain unsaturated.

The presence of partially unsaturated bonds can be attributed to the dangling bonds of these particular atoms within the channel. Consequently, our channel displays a partial unsaturation, where a combination of saturated and dangling bond atoms coexist. These partially unsaturated bonds behave as trap states during carrier flow in a FET, we carried out quantum transport calculations of InAs NWFET with surface traps.

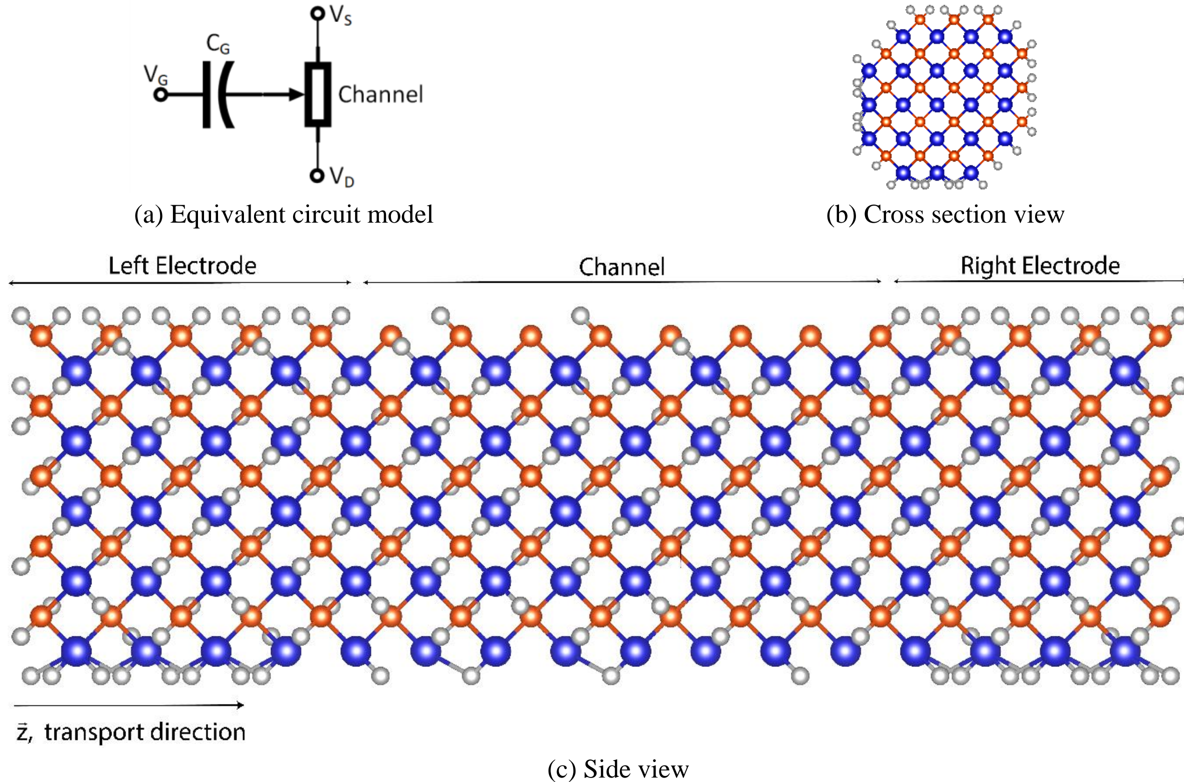


Figure 1. (a) Circuit model of simulated InAs NWFET with $\boldsymbol{V_G}$ and $\boldsymbol{C_G}$ (b) Cross section view of InAs NWFET (c) Side view of InAs NWFET. In (b) and (c), grey, blue and orange spheres represent H, In and As atoms, respectively.

Electronic structure calculation of InAs NW [110]

We first consider finding the relaxed atomic structure of the InAs NW with optimized atomic coordinates, followed by the calculation of electronic properties using numerical atomic orbitals as basis sets and Troullier Martin norm-conserving pseudopotentials. (Troullier & Martins, 1990) as implemented in SIESTA package (José M Soler et al., 2002). The exchange-correlation approximation is represented using generalized gradient approximation (GGA) (Perdew et al., 1996) within scheme of PBE (Perdew et al., 1996). After performing convergence analyses of the total energy with respect to the mesh cut-off value for the InAs nanowire unit cell, an energy cut-off of 200 Ryd for the basis set has been chosen. The relaxed atomic coordinates of the InAs with growth direction [110] nanowire have been found by using conjugate gradient method until the maximum force on atoms become less than 0.05 (eV/Å).

In addition, Brillouin Zone (BZ) calculations have been utilized to find electronic structure of InAs nanowire in the accuracy limit of GGA approximation. K-point sampling was chosen to be $1 \times 1 \times 25$ which is high in transport direction of the lattice vector $\vec{c}$ whereas low in transverse directions.

Quantum transport calculations for various trap densities of InAs NWFET

Since we have fully optimized the atomic coordinates of InAs NWFET, we have studied quantum transport properties depending on the trap concentration using non-equilibrium Green's function (NEGF) techniques, within the Keldysh formalism, based on density functional theory (DFT) as implemented in the TranSIESTA. All calculations have been performed using double zeta polarization

orbitals (DZP) as basis sets. The current through the contact region was calculated using Landauer-Buttiker formula (Datta, 1997). The gate voltage is swept from −0.5 V to 1.5 V at 0.1 V intervals, for three different surface trap densities 0, $1{\cdot}10^{12}$ /cm^3 and $5{\cdot}10^{12}$ /cm^3. The drain voltage is set at 0.5 V with respect to the source, $V_{DS} = 0.5$ V. The structural and geometrical parameters of InAs NWFET throughout this study have been given in Table 1.

RESULTS AND DISCUSSION

Electrons have spatial constraints in radial directions but they have freedom to propagate as 1D Bloch states along the longitudinal direction in NWs (Datta, 1997).

When combined with an electrode without any lattice mismatch as in our study, a junction is formed between InAs nanowire and electrodes. Since doping levels are the same for source and drain electrodes of InAs NW, the Fermi levels are assumed to be the same in energy-space. Depending on the applied bias voltage, Fermi energy distribution will change because of different charge distribution in electrodes. The current starts flowing once the top of the valance band of the left (source) electrode matches in energy with the bottom of the conduction band of the drain. However, a specific state, which propagates along the channel, can decay when an energy matching state is absent.

After elucidating the electronic properties of individual InAs NWs, we have studied the transport properties of InAs NWFET.

Structural and Electronic Properties of InAs NW [110]

The central region contains 5 primitive unit cells, with a total length of 54.56 Å. The length of the central region is sufficient to avoid an abrupt change in electronic structure while forming FET structure.

In and As atoms have 4 neighbors in InAs bulk, cutting InAs bulk as a wire results in dangling bonds at the surface and edges. After successfully achieving the complete optimization of the InAs nanowire structure, we proceeded to analyze the optimum bond lengths between the various atoms. Notably, the bond length between H and In atoms was determined to be 1.84 Å, while the bond length between A and H atoms was 1.51 Å. Additionally, for In and As atoms located near the surface of the nanowire, the bond length was found to be 2.61 Å. This bond length does not change for the inner atoms. Upon conducting our optimization process, we observed that the bond lengths between H atoms and their corresponding NW atoms exhibited minimal changes. As a result, after obtaining the fully optimized structure of the nanowire, we proceeded with transport calculations while maintaining the H atoms in a fixed position, or “frozen.” The central region (channel or scattering region) contains a few dangling bonds due to some removed H atoms. Since these dangling bonds constitute delocalized electrons, the partially unsaturated InAs NW become metallic as seen in Figure 2 and Figure 3, partial density of states of InAs NW, electronic band structure of InAs NW, respectively. Especially In and As atoms have contributions to density of states around E_{f}, revealing its metallic character. The As atoms have larger contributions around E_{f} due to having more valance electrons compared to In atoms. However, upon passivation of dangling bonds with H atoms, the metallic nanowire becomes semiconductor as shown in electronic band structure of InAs NW in Figure 4. These metallic electronic states originating from mostly unsaturated As atoms leads to accumulation of opposite charges along the As atoms on the surface. Thus, the surface of InAs NW becomes 1D metal.

We have found that electronic band gap of saturated InAs NW with radius 0.75 nm is $E_g = 1.64$ eV. It should be noted that the band gap is underestimated by the GGA calculations used in our study. Also, saturated InAs NW is direct band gap semiconductor as in the case of bulk InAs. Due to quantum confinement, InAs NW has larger electronic band gap compared to bulk InAs (Yeu et al., 2019).

Bond lengths are quite similar to the InAs bulk for passivated InAs NW, preserving its structural symmetry.

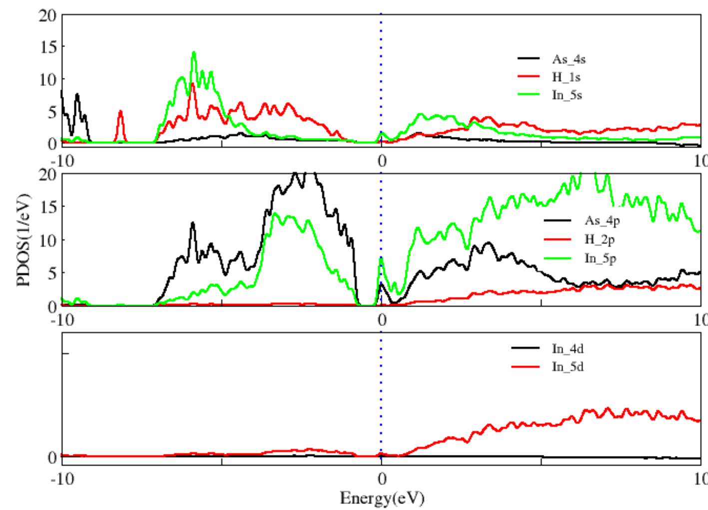


Figure 2 Partial Density of States (PDOS) of partially unsaturated InAs nanowire [110]

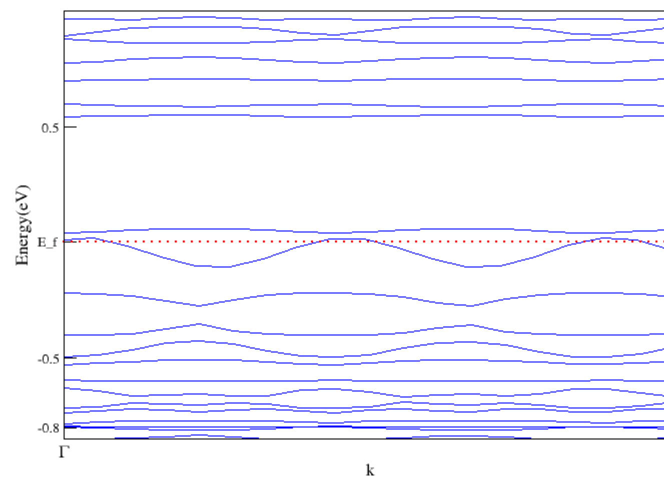


Figure 3 Electronic band structure of partially unsaturated InAs nanowire [110]

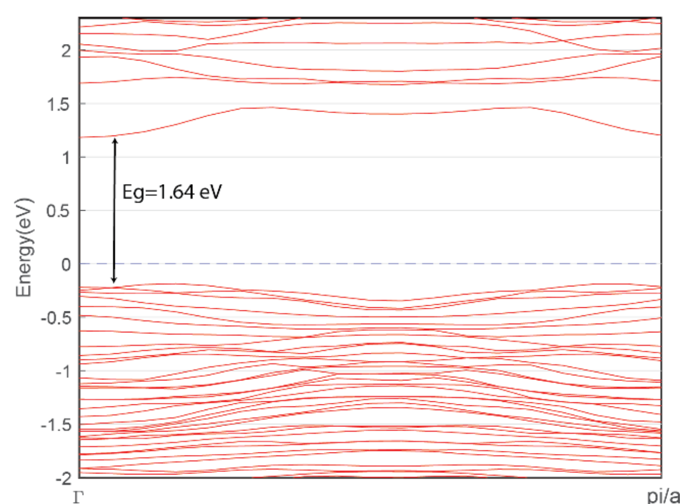


Figure 4. Electronic band structure of saturated InAs nanowire with growth direction [110]

Quantum Transport Properties of InAs NWFET for Various Trap Densities

We have applied gate voltage under 1 nm below the simulation box. The vacuum thickness is 1 nm in our simulation study. This vacuum thickness corresponds to oxide layer of SiO_2 with dielectric

constant of $(3.9 \cdot \varepsilon_0)$. Ballistic transport calculations have been done using Landauer-Buttiker formalism as given in Equation 1-2.

$$G = \left(\frac{q^2}{h}\right)\tilde{T} \quad (1)$$

$$I = \left(\frac{q}{h}\right)\tilde{T}[\mu_1 - \mu_2] \quad (2)$$

Here, G is quantum conductance and T is transmission probability matrix for each possible state contributing the current. μ_1 and μ_2 are chemical potentials of electrodes. This chemical potential difference can be modified by applying V_{DS}.

The applied bias changes chemical potential in the electrode and the gate voltage modifies the barrier height between the electrode and the channel. Having unsaturated atoms at the surface of InAs NW, a Schottky barrier is formed between the channel and the electrode. The height of Schottky barrier is also modified by the gate voltage.

As the concentration of surface traps increases, the Schottky barrier height increases, too. In turn, the V_{TH} also increases as shown in Figure 5. The current (I_{DS}) – voltage (V_G) curves in semi-log scale for different values of trap densities are given in Figure 5a. InAs NWFET works in almost ohmic region for all trap densities.

In addition, the gate voltage affects electronic bands in the channel so that bands bend accordingly as gate voltage is applied. The number of the electronic bands crossing the Fermi level will eventually contribute to the current. However, the existence of the same energy states between the electrode and the channel determines the overall current characteristics of InAs NWFET.

We have also calculated the transconductance (g_m) of InAs NWFET for bias voltage of 0.5V. The calculated values are given with structural parameters of InAs NWFET in Table 1. Clearly, saturated InAs NWFETs have larger transconductance values compared to unsaturated ones.

Table 1. Structural parameters used both for saturated and unsaturated InAs NWFET

L_G [nm]	L_S [nm]	L_D [nm]	a [nm]	t_{ox} [nm]	C_G [nF]	g_m[nS] (unsaturated)/saturated
5.4	5.4	5.4	0.75	1	0.07	2.4/7.4

$\boldsymbol{L_G}$, $\boldsymbol{L_S}$, $\boldsymbol{L_D}$, $\boldsymbol{a}$, $\boldsymbol{t_{ox}}$, $\boldsymbol{C_G}$, $\boldsymbol{g_m}$ values are gate length, source length, drain length, nanowire radius, oxide thickness, gate capacitance, and transconductance, respectively.

We have finally calculated field effect mobility, μ_{FE}, using Equation 3 both for saturated and partially unsaturated InAs NWFETs. Field effect mobility shows the efficiency of the device and it is an important figure of merit for benchmarking transistor performance and operation. The gate capacitance (C_G) plays a crucial role in determining field effect mobility. In fact, C_G should be expressed at least in terms of interface capacitance and oxide layer capacitance. However, in our simulation model the oxide layer is modeled implicitly by adding a vacuum layer between the FET and the gate. Additionally, our simulation method neglects the interface capacitance. Here, we have assumed oxide layer to be SiO_2 with dielectric constant of $(3.9 \cdot \varepsilon_0)$. Thus, our values for field effect mobility are the lowest possible values within accuracy of C_G.

$$\mu_{FE} = g_m\, L_G^2 / C_G\, V_{DS} \quad (3)$$

Our findings are compared with the literature in Table 2. As clearly seen, unsaturated NWFETs have low I_{on}/I_{off} ratios. Despite its extremely low field effect mobility, I_{on}/I_{off} ratio of ZnO NWFET (Bryllert et al., 2005) go beyond the unsaturated Si NWFET (Clément et al., 2010). In our study, we

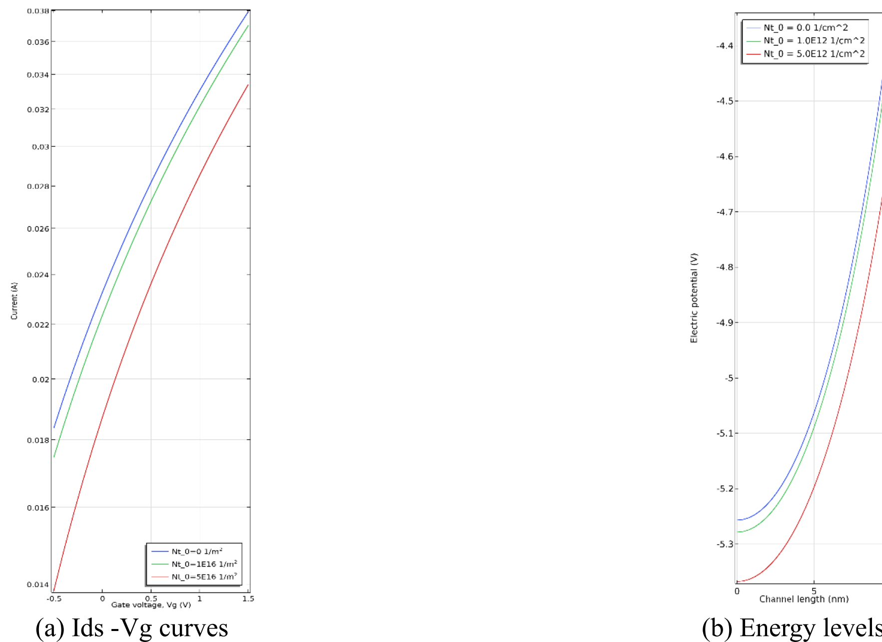
have found that transconductance value is low for InAs NWFET with surface states. It should be noted that a decrease in the transconductance implies a lower carrier mobility. Because g_m depends on V_{DS}. in linear region of on-state. If V_{DS} is constant, g_m value is directly related with carrier mobility.

Table 2. The transport characteristics of different unsaturated NWFETs

NWFET	μ_{EF} [cm^{2}V^{-1}s^{-1}]	carrier	I_{on}/I_{off}	Reference
Si	560	hole	10^4	(Cui et al., 2003)
InAs	6200 – 1900	electron	2 – 100	(Dayeh et al., 2007)
InAs (unsaturated)	250	electron	2	This work
GaN	650	electron	-	(Huang et al., 2002)
ZnO	13±5	electron	10^5-10^7	(Bryllert et al., 2005)

Electrostatic screening effect of the surface traps is seen in Figure 5b. Surface traps serve as accumulation centers for compensation charges originating from the inner region of the nanowire. This charging process diminishes the electronic impact of the gate voltage. Although this charging effect occurs only along the channel, the positions of electronic bands within the channel changes significantly. So, the gate voltage has been screened by the accumulated charges within channel. The more surface state concentration, the more electrostatic screening effect occurs.

To envisage the electron and current density along the channel, we have calculated real space resolved local density of electrons (LDOS) as given in Figure 6. The LDOS in Figure 6 is given for on state of InAs NWFET with trap concentration of $5 \cdot 10^{12}$ and gate voltage 1.5 V. The electron concentration and current density along the channel is obvious. And electric field gradient from top of the device to interior part changes due to charge compensation during the on state. Contour maps of the carrier concentration also exhibits that depletion region cannot go beyond long enough under the gate. The presence of accumulated charges due to surface states prevents full channel depletion. Thus I_{on}/I_{off} ratio becomes very low compared to fully saturated InAs NWFET (Chuang et al., 2013).



(a) Ids -Vg curves (b) Energy levels

Figure 5. (a) $I_{DS} - V_G$ curves for unsaturated InAs NWFET for various trap concentrations. (b) Electric potential change for InAs NWFET along the channel for different trap concentrations

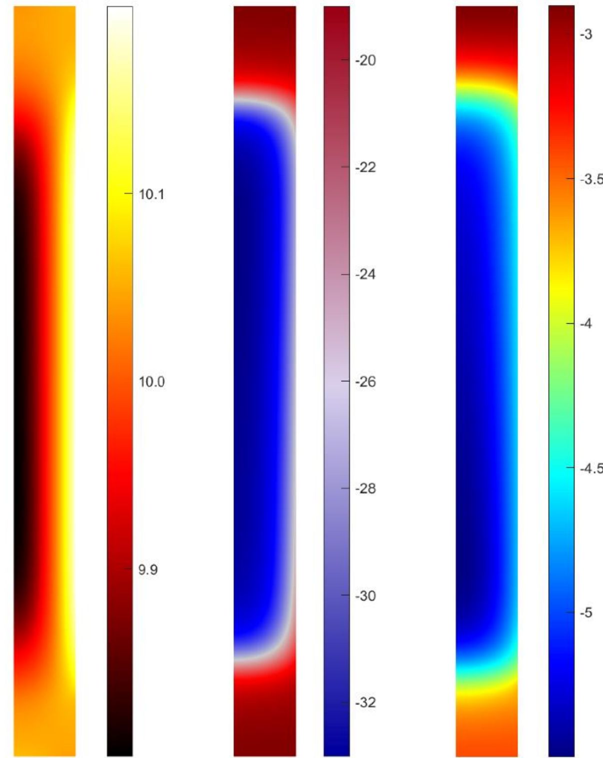


Figure 6. From left to right: the current density, electron distribution, and the electric field contour plots from LDOS calculations, when InAs NWFET is on-state with gate potential 1.5 V and trap density is $\mathbf{5 \cdot 10^{-12}\ cm^{-2}}$

CONCLUSION

Surface traps can change the electronic behavior of NWs. Partially unsaturated InAs NW have been found to be metal in contrast with saturated InAs NW with the same dimensions.

Our findings indicate that surface traps have the ability to shield the electrostatic influence of the gate voltage in partially unsaturated InAs NWFETs. This results in a significantly low I_{on}/I_{off} ratio, reaching as low as 2, which is remarkably inadequate for potential nano-electronic applications.

Since I_{on}/I_{off} ratio is remarkably low to be sufficient in real FET application, surface passivation should be introduced. We have found that μ_{EF} is also lower than saturated InAs NWFET with same structural parameters.

Surface passivation is essential in the design of InAs NWFETs due to the considerable degradation of their transport properties caused by surface traps. Additionally, surface traps offer an opportunity to study low-dimensional confined systems. More elaborate studies are still needed with more extensive circuit models and numerical methods.

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Conflict of Interest

The article authors declare that there is no conflict of interest between them.

Author's Contributions

The authors declare that they have contributed equally to the article.

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