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On the Efficient Implementation of Pulse-Width Modulated Digital Analog Converters

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Abstract

Pulse-Width Modulated Digital-Analog Converter (PWM DAC) is the most popular digital-analog conversion structure in embedded system design. However, there is no explicit formulation existing in the literature for the efficient utilization of PWM DAC implementation regarding to resolution and switching noise considerations. In this paper, optimum PWM frequency formulization is given to limit switching noise less than the least significant bit in the implemented DAC structure. So that, PWM resolution is maximized regarding to the analog signal bandwidth, where analog bandwidth and switching noise are the tradeoff in the PWM DAC. In addition, to extend the limits of the PWM modulator, a hybrid R-2R and PWM structure is proposed for the resolution improvement, resulting as higher dynamic range for the total system.

1. INTRODUCTION

Pulse-width modulated digital-analog converters (PWM DACs) are being implemented for decades [1]. The implementation is popular for its low cost and easy configuration [2-6]. The resolution of the PWM DAC is limited by counter range of the PWM generator and switching noise after the filter. As a result, the resolution of the PWM DACs is not adequate for many of the embedded system requirements whenever high resolution is needed. In [5] an alternative implementation for the PWM DAC, pulse-count modulation (PCM) is defined. The PCM method increases performance; however, the implementation is not possible using internal PWM modules of the microcontrollers. Delta-sigma PWM DACs provide high resolution [7-9]; however, the implementation of delta-sigma conversion is not possible by using basic PWM modules of general-purpose microcontrollers, rather, it requires digital and analog full custom design blocks which is not suitable for low-cost general-purpose design.

General DAC applications using PWM modulators are LCD contrast and backlight brightness control, power supply voltage adjustment, battery charger voltage and current adjustment, trimmer pot elimination, general reference voltage generation, simple music players for embedded applications etc. If high resolution is needed, generally external DACs are interfaced to the microcontroller systems. PWM DACs are also implemented in VLSI design [10-12]. PWM signals are also used for class-D audio amplifiers, motor control, DC-DC converters etc. [13-14]. In this paper, general purpose PWM DACs are analyzed in terms of switching noise and maximum achievable resolution depending on switching noise amplitude. As a result, a clear formulation is given to realize an effective PWM DAC.

PWM switching frequency and PWM resolution are the critical parameters for the calculation of the effective number of bits for PWM DACs. Increasing the PWM resolution does not directly increase the effective resolution. The reason is that, whenever the resolution is increased, PWM switching frequency is decreased, since PWM resolution is a fraction of the system frequency. If PWM frequency is decreased, then PWM noise after the filter stage increases which deteriorates the resolution. It is interesting that, there is no clear formulation for the precise resolution calculation for accurately utilizing PWM DACs. In this

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paper, formulation for effective utilization of PWM DACs is provided. In this work, the calculations in [5] are extended to derive a formula for the maximum resolution of PWM DACs regarding to the design specifications. In addition, a second order RC filter calculations are given for straightforward implementation. As a result, switching noise at the output is kept lower than least significant bit LSB of the equivalent DAC resolution.

After precise calculations for the equivalent number of bits, the calculated resolution of the PWM DAC is increased using an R-2R ladder network for the higher significant bits. Using the proposed hybrid approach, the total DAC resolution is shared between R-2R ladder network and PWM DAC. Hence, it is much easier to reach desired DAC specifications. The flow of the paper is as follows: Section II explains general PWM DAC design steps. After that, a formulization for the maximum achievable PWM resolution is given to achieve best performance depending on analog signal band and maximum system frequency. Section III provides a novel methodology to increase the PWM DAC resolution by R-2R DAC network. Section IV provides the results related to SPICE simulations and circuit realization. Section V summarizes the paper throughout the paper from calculations to implementation.

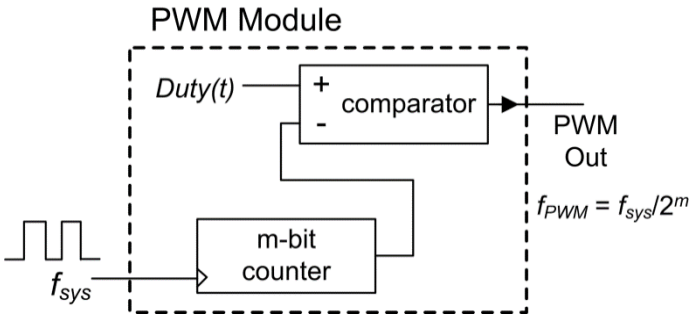


Figure 1. *Pulse Width Modulator Structure*

2. PWM DAC AND DESIGN OPTIMIZATION

General PWM module structure is shown in Fig 1. Here, f_{sys} is the main frequency of the system and *Duty*(*t*) is the duty cycle of the PWM module. PWM modulation frequency must be filtered out to have the desired analog value at the output [2-5,15,16]. Whenever PWM signal is considered as a quasi-stationary signal, DC component of the PWM signal provides desired analog output that corresponds to the duty cycle of the normalized PWM signal, and, AC component appears as noise and must be filtered out. By employing a simple RC low-pass filter at the output of the PWM modulator, a DAC is implemented, as shown in Fig 2(a). A second order RC filter stage provides better implementation of the PWM DAC [5, 6]. Although it is possible to use higher order filters they are not preferred due to increased design cost. Generally, second order filter is sufficient to obtain the desired output [6].

The duty cycle of a pulse width modulator contains the desired analog signal data. The output of the DAC can swing between GND and V_{MAX}. The maximum output voltage at the output node and least significant digit amplitude is given as:

$$V_{MAX} = V_{DD}(1-\frac{1}{2^m}), \tag{1.a}$$

$$V_{LSB} = V_{DD}\frac{1}{2^m} \tag{1.b},$$

where m is the resolution of the m-bit DAC. The normalized value of the analog signal s(t) can be represented as duty cycle of the PWM:

$$s(t) = Duty(t) \tag{2}$$

Here, Duty(t) is the duty cycle of the signal, and that corresponds to the analog output s(t) varying between 0 and 1. As s(t) is the normalized output, real amplitude of the signal is $V_{DD}.s(t)$.

The PWM output is composed of two signals: the desired analog output and modulator frequency. Since the analog signal band-width is much smaller than the modulator frequency, the analog signal component of the PWM DAC, i.e. *Duty*(*t*) signal is quasi-stationary. Hence, the quasi-stationary part of the signal contains the analog output data. Therefore, the modulator frequency must be filtered out. Fig. 2(b) shows the PWM signal in frequency and time domains. The modulator signal is filtered out using a first order RC filter to have the desired analog output in Fig 2(a). As an example, if the desired analog signal is 0.3V, then the duty cycle of the modulator has to be 30%, if 0.5V analog signal is required, then the duty cycle has to be 50%. The values are normalized to the supply voltage of 1V. The transfer function of the circuit of Fig. 2(a) is:

$$\frac{V_{Out}(j\omega)}{V_{PWM}(j\omega)} = \frac{1}{1+ j\omega RC} \tag{3}$$

The cutoff frequency for the desired analog signal can be calculted as:

$$f_{cutoff} = \frac{1}{\tau} = \frac{1}{RC}(rad/s) \tag{4}$$

In Fig. 3, analog outputs are generated using various modulation frequencies. The analog signal is generated by sweeping the duty cycle from %0, %10, ... %90 at each milliseconds. Here, supply voltage is selected to be 3.3V. In each of the step outputs, the analog signal band-width is selected to be 20 kHz, and, using (4), *R* and *C* values are selected to be 0.8 nF and 10 kΩ. As can be seen from Fig. 3, removal of modulator noise from the analog signal is very critical to reach a desired output resolution level, if modulation frequency is increased, then output noise level is less at the output. On the other hand, if PWM modulator frequency is increased, then PWM resolution decreases since:

$$f_{PWM} = \frac{f_{sys}}{2^m} \tag{5}$$

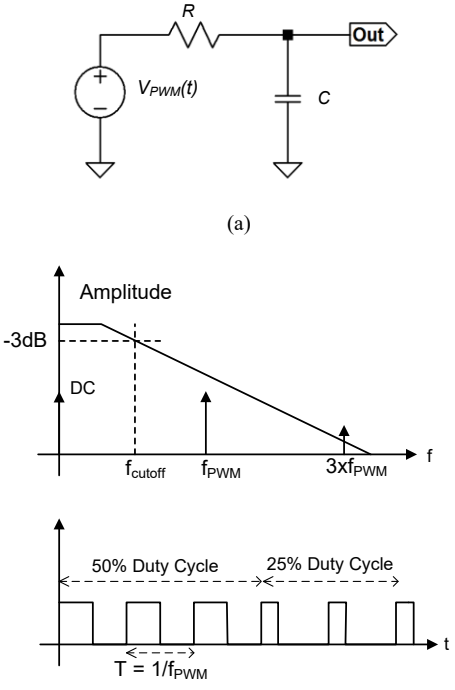


Figure 2*. (a) PWM digital-to-analog converter; (b) frequency and time representation*

The resolution of the PWM DAC depends on the pulse-width modulator resolution, desired output frequency band (fcutoff), and the filter performance for the pulse-width modulator frequency suppression.

The remaining pulse-width modulator frequency component appears as noise at the output and limits the resolution of the DAC.

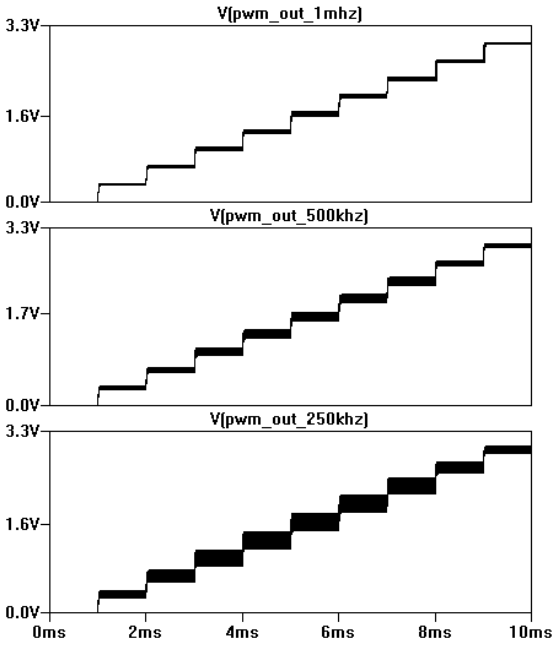


Figure 3. *Analog output generated using various PWM frequencies*

Even if m-bit counter is utilized for the PWM module as shown in Fig. 1, it does not guarantee m-bit resolution. The reason is that, if PWM DAC output noise is higher than the V_{LSB} as given in (1.b), then the effective resolution will be less than m-bits.

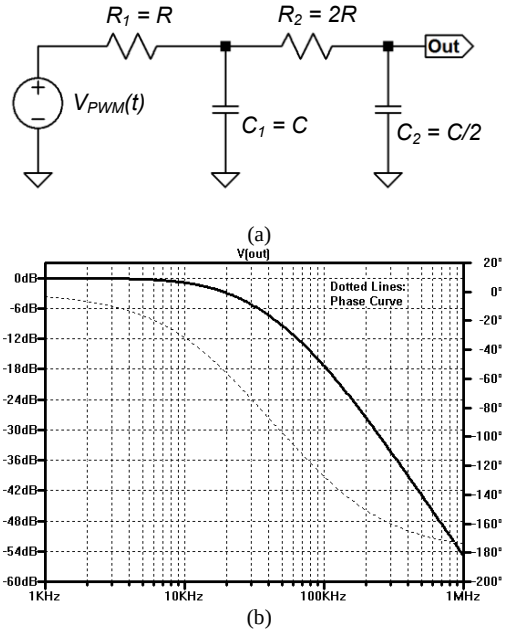


Figure 4. *(a) Second order RC filter; (b) frequency response*

For most of the applications, a first order RC filter stage is not sufficient for the removal of the PWM noise. In general, second order filter is employed to reach higher resolution levels. Here, in order to reach for the desired resolution requirements the calculation of component parameters for a second order RC filter is given. Moreover, the calculations in [5] are extended for the usage of second order and fourth order Butterworth filter applications.

A possible implementation of a second order RC filter is shown in Fig. 4(a). Here, in order to reduce the loading effect, the resistor in the second stage is selected as 2R. Regarding to this, the second stage capacitor value is selected to be C/2. The ration of the resistors and capacitors can have any value, however, R – $2R$ and C – $C/2$ are the values that are the easiest selectable values especially for the discrete component implementation. The filter transfer function of the circuit in Fig. 4(a) is:

$$\frac{V_{out}(s)}{V_{PWM}(s)} = \frac{1}{(RC)^2 s^2 + \frac{5}{2} RCs + 1} \tag{6}$$

The frequency response of the second order RC circuit in Fig. 4(a) for component values of R = 10k and C = 375pF is shown in Fig.4(b). Here, -3dB cutoff frequency is 20 kHz. Using the configuration in Fig. 4.(a) cutoff frequency can be extracted using SPICE simulations as:

$$f_{cutoff} \approx \frac{0.075}{RC} \quad \text{(Hz)} \tag{7}$$

The simulation setup is done as follows: The circuit shown in Fig. 4(a) which has R and 2R as the resistor values and C and C/2 as capacitance values is simulated in AC domain. -3 dB point of the circuit is recorded from the simulation output. Then, it is assumed that -3dB point, i.e., $f_{cutoff} = k/RC$. As f_{cutoff}, R and C all is known values, k is extracted to be 0.075, which provides the formula given in (7). The empirical formulization is verified on various R and C values and the formulization always gives correct f_{cutoff} which has been verified SPICE simulations.

The second order RC filter shown in Fig. 4(a) has R and 2R resistor values and C and C/2 capacitance values, which provides easy implementation. In addition, the cut-off frequency in (7) provides a fast calculation method without complex filter calculations. If the PWM modulation frequency is much greater than the analog signal band, which is always true for the system proposed, by using (6), attenuation rate of the PWM modulation frequency noise normalized to 1V input can be estimated using second order terms of the transfer function as:

$$\left|V_{out}(j\omega)\right| = \frac{1}{(2\pi \cdot f_{PWM} RC)^2} \tag{8}$$

As shown in Fig. 3, the noise at the output is directly dependent on the PWM frequency applied. However, maximum resolution achievable by the PWM modulator decreases as PWM frequency is increased. For a pulse-width modulator, let us define system frequency as f_{sys}. Relation between the system frequency (f_{sys}) and PWM frequency (f_{PWM}) has already been given in (5). LSB amplitude normalized to 1V is:

$$V_{LSB} = \frac{1}{2^m} = \frac{f_{PWM}}{f_{sys}} \tag{9}$$

If the amount of PWM noise at the LSB level is defined as Ripple, using (8) and (9) the minimum PWM frequency for a system can be approximated as:

$$\frac{1}{(2\pi \cdot f_{PWM} RC)^2} < \frac{f_{PWM}}{f_{sys}} (Ripple)$$

Replacing RC as $0.075/f_{cutoff}$ using (7),

$$(2\pi \cdot \frac{0.075}{f_{cutoff}} f_{PWM})^2 > \frac{f_{sys}}{f_{PWM}.(Ripple)}$$

after grouping terms,

$$f_{PWM} > \sqrt[3]{\frac{f_{sys}(f_{cutoff})^2}{0.222 \cdot (Ripple)}} \tag{10}$$

The "Ripple" in each of the calculations represent worst case ripple, and should be selected between 0 and 0.5 depending on the application requirements. Maximum achievable number of bits for the resolution can be calculated accordingly:

Table 1. *Optimum PWM frequency calculations*

	Filter Type			
	1st order RC	**2nd order RC**	**2nd order Butterworth**	**4th order Butterworth**
$f_{PWM} \geq$	$\sqrt[2]{\frac{f_{sys} f_{cutoff}}{0.64 \cdot (Ripple)}}$	$\sqrt[3]{\frac{f_{sys} (f_{cutoff})^2}{0.222 \cdot (Ripple)}}$	$\sqrt[3]{\frac{f_{sys} (f_{cutoff})^2}{0.81 \cdot (Ripple)}}$	$\sqrt[5]{\frac{f_{sys} (f_{cutoff})^4}{0.781 \cdot (Ripple)}}$
$m = \left\lfloor \log_2 \frac{f_{sys}}{f_{PWM}} \right\rfloor$ (m :effective number of equivalent bits)				
$f_{PWM\_Opt} = \frac{f_{sys}}{2^m}$ (f_{PWM_Opt} : optimum PWM frequency)				

$$m = \left\lfloor \log_2 \frac{f_{clk}}{f_{PWM}} \right\rfloor \tag{11}$$

The optimum PWM frequency to have the maximum resolution can be calculated using (5) as:

$$f_{PWM\_Opt} = \frac{f_{sys}}{2^m}. \tag{12}$$

Resolution using various filter structures at the output can be calculated similarly.

Table 1. *Optimum PWM frequency calculations*

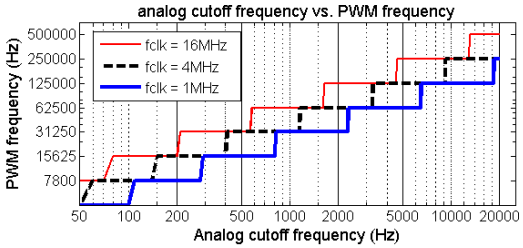
	Filter Type			
	1st order RC	**2nd order RC**	**2nd order Butterworth**	**4th order Butterworth**
$f_{PWM} \geq$	$\sqrt[2]{\frac{f_{sys} f_{cutoff}}{0.64 \cdot (Ripple)}}$	$\sqrt[3]{\frac{f_{sys} (f_{cutoff})^2}{0.222 \cdot (Ripple)}}$	$\sqrt[3]{\frac{f_{sys} (f_{cutoff})^2}{0.81 \cdot (Ripple)}}$	$\sqrt[5]{\frac{f_{sys} (f_{cutoff})^4}{0.781 \cdot (Ripple)}}$
$m = \left\lfloor \log_2 \frac{f_{sys}}{f_{PWM}} \right\rfloor$ (m :effective number of equivalent bits)				
$f_{PWM\_Opt} = \frac{f_{sys}}{2^m}$ (f_{PWM_Opt} : optimum PWM frequency)				

Calculations for optimum efficiency of PWM DACs using various output filter structures are given in Table I. The optimum PWM frequency and equivalent number of bits regarding to the analog cutoff frequency

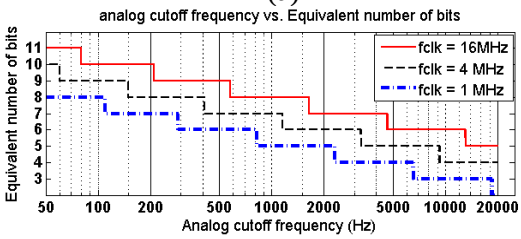
can be seen in Fig. 5. In the figure, 1 MHz, 4 MHz and 16 MHz are selected as system frequency. Formulization given in Table I is implemented regarding to the analog signal band requirement and system frequency. As a result, Fig. 5 is provided to show the limitations of PWM DACs due to various system frequency and analog signal band specifications.

The formulization given in Table I can be explained by an example. Here, the second order RC filter in Fig. 4(a) is used for the design example. Let us assume that system clock, i.e. f_{sys} is 16 MHz (it depends on the system frequency of the controller), and the DAC output frequency (f_{cutoff}) is 20 kHz. And the Ripple for least-significant bit is 50 per cent, i.e. 0.5 (which is generally the case). Then, using (10), f_{PWM} is calculated as 386kHz. Using (11), possible PWM resolution is $\lfloor \log2(16\text{MHz}/\,386\text{kHz}) \rfloor$ = 5-bits. Then, using (5), optimum PWM frequency f_{PWM_Opt} is calculated as 500 kHz. For the selection of R and C values, (6) can be used. If R is selected to be 10 kΩ, C is approximately 375 pF. To state explicitly, 5-bits of resolution is the best achievable resolution according to the given design specifications where 500 kHz PWM frequency provides the optimum resolution.

A second example may be generation of a much lower analog signal such as f_{cutoff} = 50 Hz,



(a)



(b)

Figure 5. *(a) Optimum PWM frequency vs. DAC output cutoff frequency (for the second order RC filter); (b) Equivalent number of bits when the optimum PWM frequency applied.*

similar to the requirement in [20], as 50Hz is reference frequency of AC mains supply and can be used as reference voltage for the generation of uninterruptible power supply (UPS) outputs etc. If system clock is 16 MHz, same as previous example, using (10), f_{PWM} = 7kHz. Maximum possible resolution is $\lfloor \log2(16\text{MHz}/\,7\text{kHz}) \rfloor$ = 11-bits. Then, f_{PWM_Opt} is calculated as 7812 Hz. In this configuration, using (6), if C is selected as 1μF then R can be selected as 10kΩ. As the examples reveal, PWM DAC resolution is dependent on analog signal band of the PWM DACs.

3. INCREASING RESOLUTION USING R2R NETWORK

To increase resolution of the PWM DAC an R-2R ladder network can be added. R-2R ladder DACs are another well-known DAC topology requiring multiple inputs for DAC implementation [15-19]. To implement a hybrid DAC structure, the PWM input is applied to the grounded node of the terminal resistance of the R-2R network. Resulting circuit structure is given in Fig. 6. Here, less significant bits are applied as PWM inputs and significant bits are applied as R-2R network. The total resolution can be calculated as:

$$Resolution_{DAC} = m + k, \tag{13}$$

where m represents PWM DAC resolution and k represents R-2R DAC network resolution. In Fig.6, the R-2R resolution is 4-bits, and the PWM resolution is dependent on the resolution of the modulator that can be

calculated using Table I depending on the design requirements. If the previous section's example is selected, PWM resolution was calculated as 5-bit resolution, as a result the circuit in Fig.6 would have 5+4 = 9-bits of resolution.

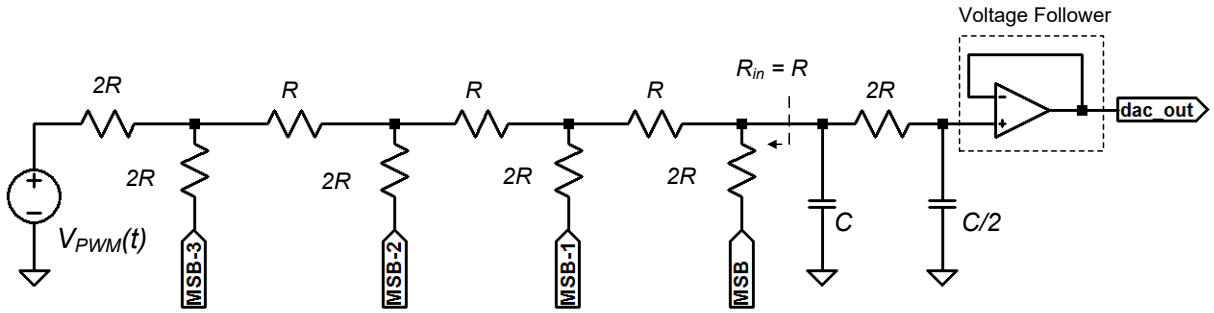


Figure 6. *Hybrid DAC with second order RC filter*

The circuit presented in Fig. 6 functions as a hybrid DAC. Moving the RC filter stage at the end of the DAC structure removes the undesired output noise, i.e. glitches, generated from digital inputs of R-2R network. Glitch is the main problem of many DAC systems especially whenever bit transition is high such as 011111 to 100000. The glitch problem is defined in many of the resources [21-22]. Moreover, positioning the filter at the output also removes noise sources related to the other digital signalling paths. The resistor components for the R-2R ladder network in the proposed circuit are selected to be same values of R and C in the filter stage for easy implementation of the structure.

A passive second order RC filter stage is generally sufficient for the noise removal of the PWM signal. The Op-Amp at the output functions as a buffer (voltage follower) and required for the impedance isolation of the filter and R-2R DAC stage. In Fig. 6, the voltage follower stage is optional, if the target has high impedance, then the voltage follower stage can be removed. The circuit performance is also verified using SPICE together with physical measurements. SPICE verification is done as follows: PWM signal is applied as square wave with 50 % duty cycle at the V_{PWM} input of Fig. 6. Transient amplitude swing at the DAC output is always recorded to be less than least significant bit amplitude given in (1.b). As a result, the resolution requirement is verified.

In the proposed circuit shown in Fig. 6, matching ratios of the R-2R ladder network is critical [17-19]. The possible achievable resolution for the resistor tolerances are calculated using Monte-Carlo simulations of the R-2R ladder network. Resolution table for the resistor tolerances of the R-2R ladder network is given in Table II. As an example, if PWM resolution is 5 bits and 3-bit R-2R ladder network is employed it results as 8-bit total resolution. If the circuit is built using 1% tolerance resistors, only 3-bits of R-2R ladder network is implemented and there exists missing codes only at 2^3-1 = 7 points. Missing codes can be defined as non-monotonic steps at the DAC output larger than one LSB. Missing codes, i.e. non-linearity of the R-2R steps can be calculated as:

$$M_{MAX} = Resolution_{DAC} - Res\_Max_{R2R} \quad \text{bits} \tag{14}$$

where $Resolution_{DAC}$ is the resolution of hybrid DAC structure, as calculated in (13); Res_Max_{R2R} is the maximum achievable resolution of R-2R ladder according to the resistor tolerances that can be looked-up from Table II.

If Res_Max_{R2R} value is greater than targeted resolution, i.e. $Resolution_{DAC}$, then there is no missing code existing in the structure. As an example, if 8-bits of resolution is targeted using n = 5-bits of PWM and m = 3-bits of R-2R network with 1% tolerance resistors, $Resolution_{DAC}$ = 8, Res_Max_{R2R} = 6 (looked-up from Table 2), then missing codes M_{MAX} = 2 bits as maximum. Since R-2R network is selected to be 3-bits, there will be maximum 2-bits of nonlinearity at $2m - 1 = 7$ distinct points. Although R-2R network can add missing codes to the DAC, the dynamic range of the system is increased which is more important in many of the applications. As a result, $Resolution_{DAC}$ can be selected as higher than the Table 2 shows limitations of R-2R ladder limitations, $Resolution_{DAC}$ can be selected higher than $Resolution_{R2R}$ whenever dynamic range is more important than precision.

Table 2. *Resistor tolerances vs. total resolution*

Resistor tolerance (R-2R ladder)	Maximum deviation (normalized to 1V)	Maximum resolution of R-2R network (Res_Max_{R2R})
1%	7mV	6-bits
0.5 %	3.9mV	7-bits
0.1 %	0.85 mV	9-bits
0.05 %	0.37mV	10-bits

4.RESULTS AND DISCUSSIONS

The proposed structure shown in Fig. 6 is simulated using SPICE and also realized using a prototype board interfaced to an Altera™ Cyclone-III FPGA development board. SPICE simulations are done by applying square wave inputs with various duty cycles for the circuit shown in Fig. 6. Also R-2R bits are tested by applying V_{DD} and GND voltages to the R-2R hybrid path. SPICE simulations agree with resolution calculations, i.e., switching noise is recorded as less than one LSB is recorded.

For the hardware implementation, the resolution of the R-2R ladder and PWM DACs are both selected to be 4-bits resulting as 8-bits of total DAC resolution. Hardware implementation of PWM modulator is realized using Altera™ DE0 FPGA development board. Both PWM modulator outputs and R-2R network outputs are interfaced to the circuit shown in Fig. 6 which is realized on a prototyping board. A triangular wave is generated using FPGA board by digital up and down counter to realize the triangular wave shape. The hybrid PWM and R-2R DAC output is measured using a digital oscilloscope and the output snapshot is recorded and shown in Fig. 7. According to the simulation results and hardware implementation, there is no visible glitch in the signal transitions. The results agree with the calculations.

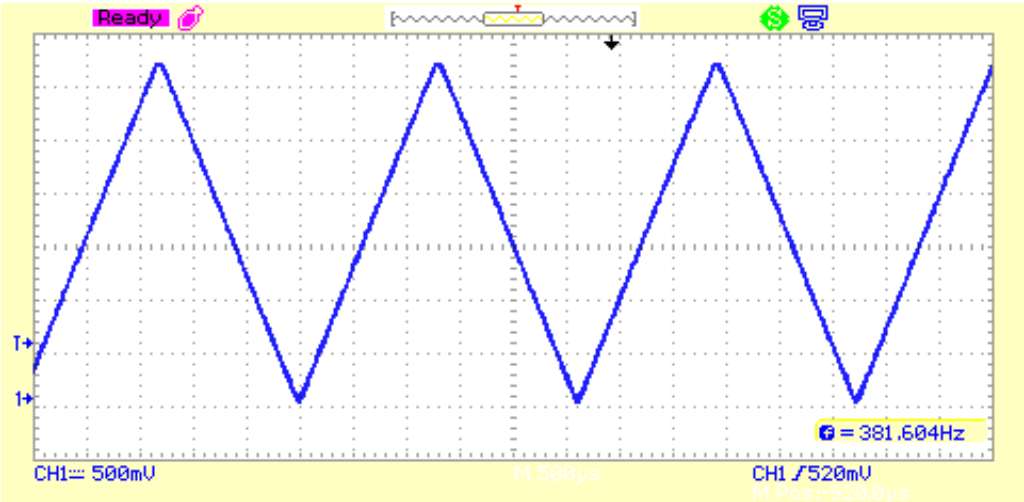


Figure 7. *Digital oscilloscope snapshot of the PWM DAC with triangular wave generation*

5.CONCLUSION

In this paper, formulation for the equivalent number of bits for maximum achievable resolution of PWM DACs is provided which is not clearly stated in previous literature. Moreover, R-2R and PWM DAC structures are employed together to have a hybrid digital-analog converter in order to increase maximum achievable DAC resolution. The proposed architecture is built using only R and 2R resistor values together with two capacitors having the values of C and C/2 for practical implementation. Moreover, a simple equation is given for the calculation of component values of the second order RC filter. Optimum resolution formulation for the second and fourth order Butterworth filters is also given for alternative implementations of PWM DACs. The proposed hybrid circuit gives freedom to designers to reach the desired DAC resolution easily. The bottleneck of the system is relative matching of the resistor values, and pulse-width modulator resolution. However, together with the proposed structure, higher design freedom is provided to reach the desired DAC performance.

CONFLICT OF INTEREST

No conflict of interest was declared by the authors

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