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Research Article

Analysis of the Performance of a 5-Level Modular Multilevel Inverter for a Solar Grid-Connected System

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Abstract : The main purpose of a multilevel inverter is to combine numerous levels of DC voltage to create a nearly sinusoidal voltage. The synthesized output waveform has more stages as the number of levels rises, creating a staircase ripple which resembles the preferred waveform. As the number of voltage levels rises, the output wave's harmonic distortion diminishes and eventually approaches zero. In particular, the performance analysis of a five-level inverter with variable loads is highlighted in this paper. This topology has fewer devices than traditional multilevel inverters for the same five output levels, which makes it more affordable due to lesser driver circuits. The proposed modular five level topology is simulated using both high frequencies switching pulse width modulation and basic frequency switching modulation techniques. The output voltage, current waveform, and total harmonic distortion are examined and compared using simulink to confirm the viability of the modular multilevel inverter topology.

Keywords : five-level, matlab-simulink, multilevel inverter, photovoltaic, total harmonic distortion.

1 Introduction

A group of power electronic converters known as multi-level inverters can create a staircase waveform from multiple DC sources. Modular Multilevel Inverters have emerged as reliable DC/AC converters for high-power applications in recent decades [1, 2, 3, 4]. When combined to two-level inverters, multi-level inverters have a numerous benefit, including dramatically lower total harmonic distortion (THD) throughout the last modulating signal and outstanding reliability, lower blockage voltage with the help of switching devices [5, 6, 7, 8]. The existence of voltage level in a multilevel inverter are sometimes related to the number of output voltage levels. In an effort to produce an output voltage of high quality, more apparatus is being used, though [9, 10, 11, 12].

The much more common multilevel inverter configurations are diode clamped (DC), flying capacitor (FC), and cascaded H-bridge multilevel inverters (CHB), as shown in Table 1. This last topology is preferable to the others because it requires minimal power switches, is more efficient, and has a simpler schematic circuit [13, 14, 15, 16, 17, 18]. Figure 1 depicts a typical single phase, five level cascaded H-bridge multilevel inverter circuit with two H-bridge modules. A P-level inverter needs R number of power switches, which is expressed in (1),

$$R = 2(P - 1) \tag{1}$$

Four power switching devices make up each H-bridge module, each of which has its own DC input voltage. The cascaded multilevel inverter has five output voltage levels which can be produced from each module: $+2V_{DC}$, $+V_{DC}$, $0V_{DC}$, $-V_{DC}$, and $-2V_{DC}$ respectively.

Table 1: Comparative components of various multilevel inverter

Parameters	DC	FC	CHB	Proposed MLI
DC Supply	1	1	2	2
Switches	8	8	8	5
Diodes	12	-	-	1
DC bus Capacitors	4	4	-	-
Balancing Capacitors	0	6	-	-

Power converter deployment is increasingly trending toward using fewer and smaller major elements as the need for energy multilevel inverters with reduced size/performance ratios grows. By reducing the number of main semiconductor switches in

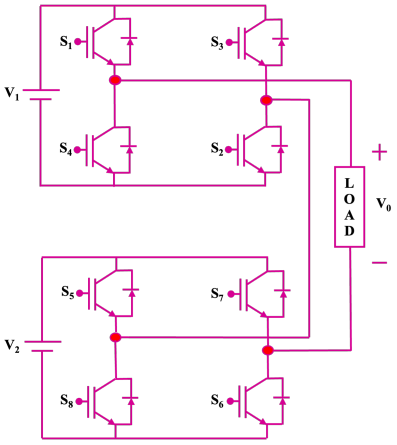

Figure 1: Conventional five level CHB

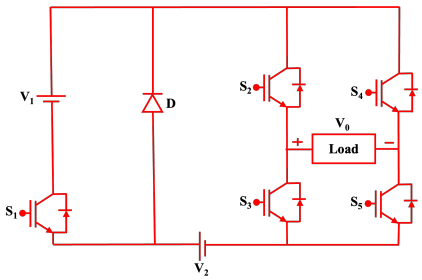

Figure 2: Proposed five level multilevel inverter

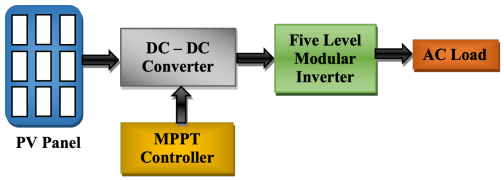

Figure 3: Representation of five level inverter with solar grid-connected system

a cascaded H-bridge multilevel inverter integration diminishes switching and conduction losses while increasing converters efficiency. As a result, a modular multilevel inverter with only five power switches and one freewheeling diode has been recommended, as illustrated in figure 2.

A new five level multilevel inverter topology is shown in figure 2 which addresses the shortcomings of the traditional cascaded H-bridge five level topology while also offering an improvement. The advantage of the proposed converter is it uses more DC link voltage while reducing the number of switches from eight to five, necessitating only one power diode. Supplementary advantages include low cost, improved efficiency, and decreased voltage stress. Voltage stress refers to the maximum voltage experienced by the components of a multilevel inverter, which can lead to insulation breakdown and reduce their lifespan. It can be reduced by using higher numbers of voltage levels, which distribute the stress more evenly, and by using pulse-width modulation techniques to minimize voltage fluctuations. Figure 3 illustrates the representation of five level inverter with solar grid-connected system. This paper is organized with 5 sections; modes of operation is reported in section 2, sinusoidal pulse width modulation (PWM) and power loss analysis is reported in section 3. Implementation of the proposed system in simulation and is reported in section 4 and finally concluded in section 5.

2 Modes of Operation

In a multilevel inverter, power semiconductors are utilized to generate a staircase waveform from multiple DC levels. Conventional multilevel inverter (MLI) has been designed with 8 insulated gate bipolar transistor (IGBT) switches on the five level output voltages. In this paper, additional commentary of the newly proposed topology with a reduced switch count of 5 IGBT switches is described. The proposed modular multilevel inverter's various modes of operation are shown in Figure 4 (a–e). The output voltage of $+2V_{DC}$ has been evaluated while switches S_2 and S_5 are turned on; during this time, voltages V_1 and V_2 are connected to a load. Similar remaining voltages of $+V_{DC}$, $0V_{DC}$, $-V_{DC}$, and $-2V_{DC}$ have been assessed during various power switching operations.

3 Sinusoidal PWM and Power Loss Analysis

In the investigation of power electronic devices, switching methods or pulse width modulation signal processing methods are frequently used. For a variety of applications, different pulse-width modulation approaches have been developed. The sinusoidal pulse width modulation (SPWM) technique is utilized to sift an output pulse-wave form with varying width into a sine wave output waveform. By using a high shift frequency, as well as by changing the frequency and magnitude of a reference or altering voltage, a superior filtered curved output wave shape may be rendered non-heritable. The most popular PWM technique, recognized as sinusoidal PWM, compares a triangular wave to a sinusoidal reference known as the modulating signal, as shown in figure 5. A MLI's magnitude and frequency modulation are controlled by the expressions (2) and (3),

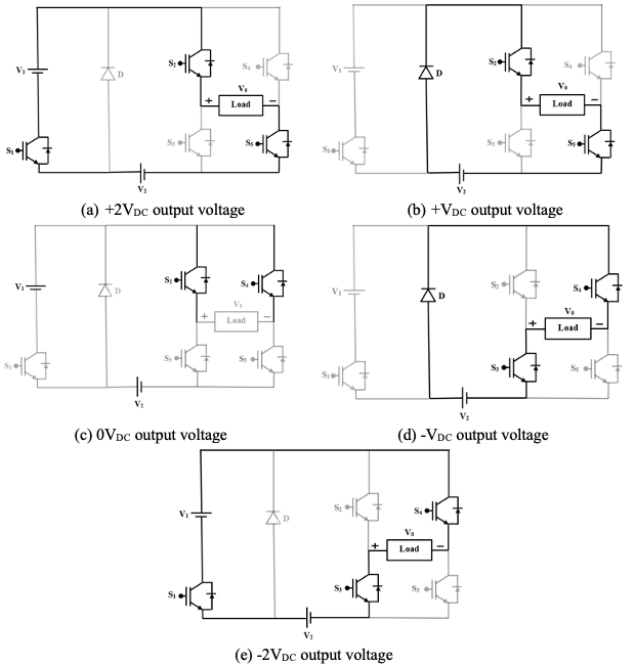

Figure 4: Proposed five level MLI – Modes of operation

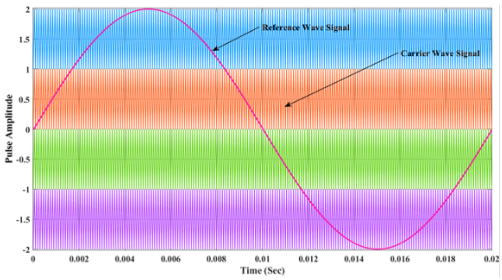

Figure 5: Sinusoidal pulse width modulation

$$M_A = \frac{V_m}{V_c(m-1)} \tag{2}$$

$$M_f = \frac{f_c}{f_m} \tag{3}$$

The following expression (4) is used to calculate the THD value of the voltage of the proposed MLI. Similar to that, the current THD value is also calculated.

$$THD = \sqrt{\frac{V_2^2 + V_3^2 + V_4^2 + \ldots + V_N^2}{V_1}} \tag{4}$$

The losses in the proposed and existing systems are majorly mainly focused on the three key power losses, particularly switching ($P_{Switching}$) and conduction losses ($P_{Conduction}$). The total power loss of the MLI is instead expressed as (5) (P_{Loss}),

$$P_{Loss} = P_{Switching} + P_{Conduction} \tag{5}$$

Conduction loss of power semiconductor devices is calculated by following equation (5),

$$P_{\text{Conduction}} = \int_0^{T_0/2} \left\{ [V_{CE0} + ri_p \sin(\omega t)] * i_p \sin(\omega t) \left[\frac{1}{2} (1 + A_m \sin(\omega t + \varphi)] \, dt \right\} \right. \tag{6}$$

after simplification of above equation,

$$P_{\text{Conduction}} = \frac{1}{2}\left\{\left(V_{CEO} * \frac{i_p}{\pi} + r * \frac{i_p^2}{4}\right) + \left(A_m * \cos\varphi * V_{CEO} * \frac{i_p}{8}\right) + \left(\frac{1}{3\pi} * r i_p^2\right)\right\} \tag{7}$$

Where V_{CEO} is the zero-current collector to emitter voltage, r is the collector to emitter on-state resistance, A_m is the modulation index and i_p is the peak current of IGBT device. Switching loss is expressed as the integration of all the turn-on and turn-off switching energies at the switching instants. In the equation, variable switching time is considered and integrated in equation (7),

$$P_{\text{Switching}} = f_{sw}\frac{1}{T_0}\int_0^{T_0/2}\left(E_{on} + E_{\text{off}}\right)(t, i_p)\,dt \tag{8}$$

Where T_0 is the switching time period, fsw is the switching frequency, E_{on} is the on-state voltage drop and E_{off} is the off-state voltage drop. The efficiency of MLI is calculation by the following equation (8),

$$\text{Efficiency} = \frac{P_{\text{Output}}}{P_{\text{Ouput}} + W_{\text{Loss}}} * 100 \tag{9}$$

4 Results and Discussion

The proposed MLI is implemented using the Matlab/simulink software tool. The simulation parameters for a five-level multilevel inverter are summarized in Table 2.

Table 2: Conventional five level CHB

Parameters	Conventional CHB Inverter	Proposed Five level Inverter
No. Input DC supply (Symmetrical)	2	2
DC Voltage (Magnitude)	110 V	110 V
RMS output Voltage	220 V	220 V
No. of IGBTs	8	5
No. Gating Circuits	8	5
Carrier frequency (kHz)	20	20
%THD (Current)	5.45 (RL load)	2.30 (RL load)
PSwitching loss	00.32 W	00.24 W
PConduction loss	48.25 W	45.31 W
PTotal loss	48.81 W	45.55 W
Efficiency	91.63%	95.52%

Figure 6 illustrates the conventional MLI output and current pattern during RL load and the proposed MLI's three phase output voltage and pattern are shown in figure 7. Dynamic load changes are shown in figure 8 after 0.1 seconds of load current pattern with staircase current pattern. Figure 9 illustrates the dynamic changes in load current for a three-phase system from resistive to resistive and from inductive to resistive. Figure 10 depicts dynamic load changes of resistive and inductive load current. THD analysis of voltage and current during RL load is presented in figure 11. Figure 12 depicts the investigation of THD current using various modulation indices. Figure 13 illustrates an efficiency analysis with variable output power.

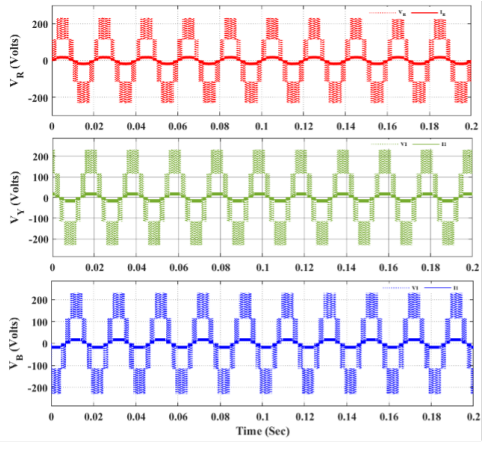

Figure 6: Voltage and current pattern of conventional MLI with R load

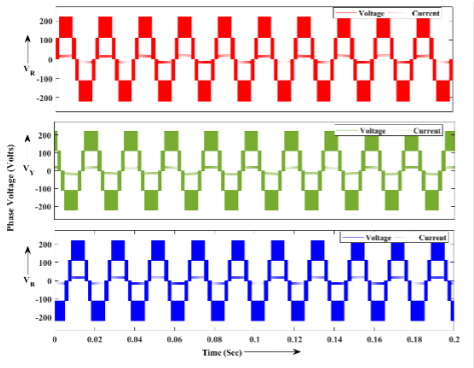

Figure 7: Voltage and current pattern of proposed MLI with R load

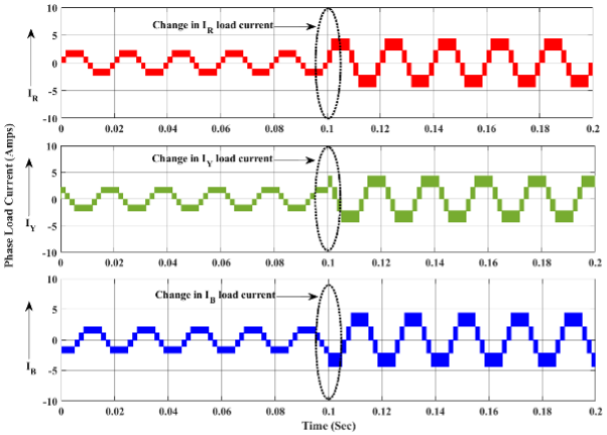

Figure 8: Proposed MLI dynamic load current variation during R load

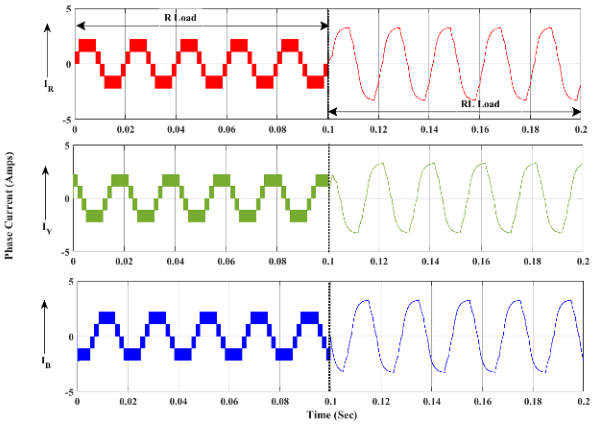

Figure 9: Proposed MLI dynamic load current variation from R to RL load

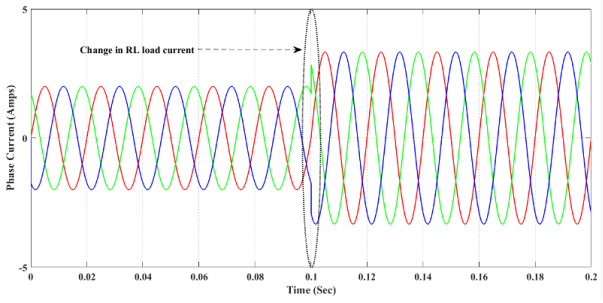

Figure 10: Proposed MLI dynamic load current variation during RL load

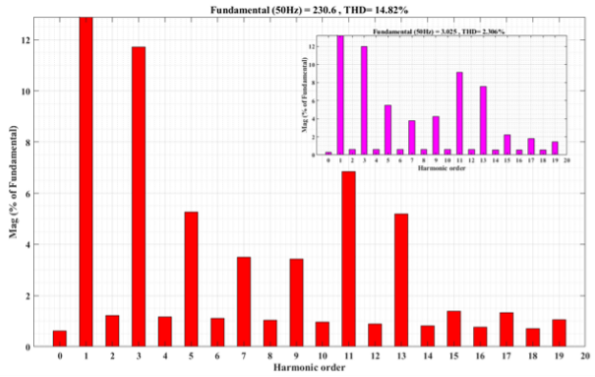

Figure 11: Proposed MLI - THD analysis of voltage and current during RL load

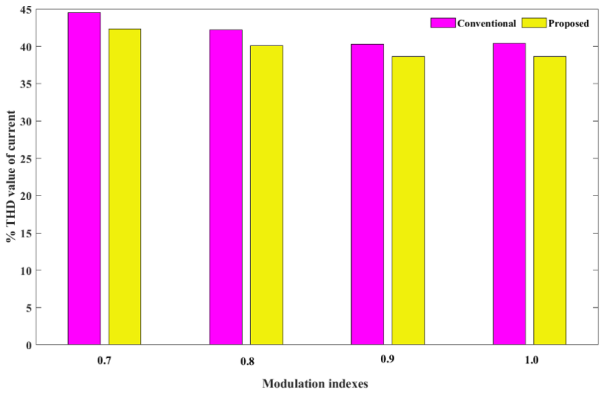

Figure 12: THD current analysis with different modulation indexes

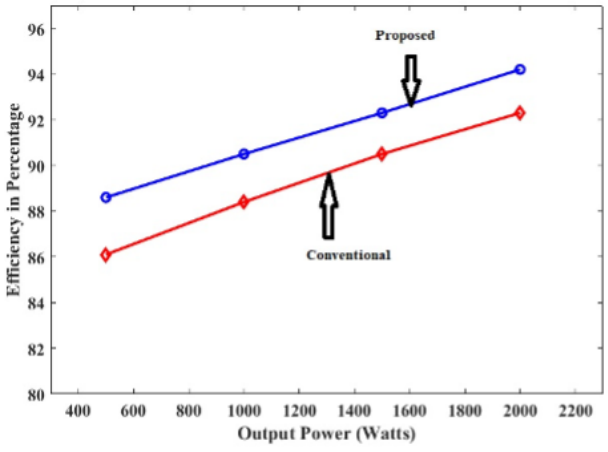

Figure 13: Efficiency analysis with variable output power

5 Conclusion

A five-level converter which is reconfigurable and utilizes fewer power switches is examined, and it is unearthed that it appeases MLI specifications. When the power switches have been given the correct pulse width modulation signal in a logical manner, the five-level inverter that was employed generated five levels of root mean square (RMS) output staircase voltage. THD values between 2.30% distances with various loads were obtained using the MATLAB/SIMULINK tool and examined. When taking into account input, output, and power losses, the proposed converter has an efficiency of 95.32%. Comparisons demonstrate

that the recommended single-phase five-level inverter outperforms conventional converters by a significant margin.

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Authors' Contributions
The authors confirm contribution to the paper as follows: study conception and design: PE, SK, data collection: PE, SK; analysis and interpretation of results: PE, SK; draft manuscript preparation: PE. All authors reviewed the results and approved the final version of the manuscript.

Competing Interests
The authors declare that they have no competing interests.

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