BMBAD BJESR Mühendislik Bilimleri ve Araştırmaları Dergisi
Journal of Engineering Sciences and Researches

FDCCII Based New Memcapacitor Emulator Circuit with Electronically Tunable

Elektronik Olarak Ayarlanabilen FDCCII Tabanlı Yeni Memkapasitör Emülatör Devresi

[1]Muhammet Oğuz KORKMAZ , [2]Abdullah YEŞİL

[1, 2]Department of Electrical and Electronics Engineering, Bandirma Onyedi Eylul University, Balıkesir, 10200 Turkey

[1]mkorkmaz@bandirma.edu.tr, [2]ayesil@bandirma.edu.tr

Araştırma Makalesi/Research Article

ARTICLE INFO

Article history

Received : 3 March 2023
Accepted : 5 April 2023

Keywords:

Memcapacitor, Emulator, FDCCII, Electronic Tunable, Grounded

ABSTRACT

Since memcapacitor and meminductor elements have not been produced yet, emulator circuits are used to examine their application areas. In this paper, a new fully differential second-generation current conveyor (FDCCII) based grounded memcapacitor emulator circuit is presented. The proposed circuit consists of one FDCCII, one multiplier, three capacitors and two MOSFETs. These two MOSFETs are utilized as electronic resistors in the circuit. The variable part of memconductance can be adjusted electronically and the proposed memcapacitor possesses an incremental-decremental adjustable structure. Moreover, it contains fewer active elements than many memcapacitor emulator studies in the literature. The proposed circuit was designed in LTspice, and frequency response, temperature, and Monte Carlo analyses were performed. In addition, the electronic resistor has been simulated at various values, demonstrating that the circuit is electronically adjustable. The simulation results are consistent with the mathematical results presented in the article.

MAKALE BİLGİSİ

Makale Tarihleri

Gönderim : 3 Mart 2023
Kabul : 5 Nisan 2023

Anahtar Kelimeler:

Memkapasitör, Emülatör, FDCCII, Elektronik Ayarlanabilir, Topraklı

ÖZET

Memkapasitör ve memindüktör elemanları henüz üretilmediğinden uygulama alanlarını incelemek için emülatör devreleri kullanılmaktadır. Bu makalede, yeni bir tam farksal ikinci kuşak akım taşıyıcı (FDCCII) tabanlı topraklanmış memkapasitör emülatör devresi sunulmaktadır. Önerilen devre, bir FDCCII, bir çarpan, üç kapasitör ve iki MOSFET'ten oluşmaktadır. Bu iki MOSFET, devrede elektronik direnç olarak kullanılmaktadır. Memkapasitansın değişken kısmı elektronik olarak ayarlanabilir ve önerilen devre artan-azalan olarak ayarlanabilir yapıdadır. Ayrıca literatürdeki birçok memkapasitör emülatör çalışmasından daha az aktif eleman içermektedir. Önerilen devre LTspice programında tasarlanmış ve frekans tepkisi, sıcaklık ve Monte Carlo analizleri yapılmıştır. Ayrıca elektronik direnç, çeşitli değerlerde simüle edilerek devrenin elektronik olarak ayarlanabilir olduğu gösterilmiştir. Simülasyon sonuçları, makalede sunulan matematiksel sonuçlarla tutarlıdır.

ORCID: [1]0000-0002-4589-4824
[2]0000-0002-0607-8226

1. INTRODUCTION

Emulator circuits have been used in the implementation of memory elements ever since the first study [1] presented the theoretical and scientific basis for the memristor element. After the production of the first memristor element [2] using TiO_2 in 2008, more studies have begun on the development of emulator circuits for memory elements. Although it is not possible to produce memcapacitor and meminductor elements at the moment, grounded and floating emulator circuits are developed and the application areas of the elements are investigated. Although there are many memcapacitor emulator circuits designed using the memristor element in the literature [3]–[13]. One of the main disadvantages of these emulators is that they have to use the memristor, which can be difficult to find on the market, or that they require a large number of active elements to design the memristor emulator. In the floating memcapacitor emulator circuit designed by Sah et al. [14], two operational amplifiers (OPAMP), one multiplier circuit and four passive elements are used. In the study by Zhao et al. [15] , both grounded and floating memcapacitor emulator circuits are proposed. While three second generation current conveyor (CCII) elements, one multiplier and five passive elements were used in the circuit designed in grounded structure, five CCII elements one multiplier and seven passive elements were used in the circuit designed in floating structure. In a study by Sharma et al. [16], a memcapacitor emulator circuit was designed using two CCII, one multiplier and passive elements. The designed emulator circuit can be used as floating and grounded by using it in different configurations. The floating emulator circuit designed by Yu et al. [17], can be used to obtain memristor, memcapacitor and meminductor elements by using different configurations. The memcapacitor emulator can be obtained by using four AD844s, one OPAMP, and nine passive elements. Although floating structures have more usage areas than grounded structures, the number of active elements used is higher in studies designed as floating structures [14-17] compared to grounded ones.

In the grounded structure memcapacitor emulator circuit designed by Fouda and Radwan [18], four OPAMPs, one multiplier, seven passive elements and one current controlled current source are used and the simulation results of the circuit are given. Three OPAMPs, two multiplier circuits and nine passive elements are used in the grounded memcapacitor emulator circuit designed by Fitch et al. [19]. The circuit has been tested both as a simulation and experimentally. In a study conducted by Yuan and Li [20], a circuit was designed using three OPAMPs, one multiplier, and nine passive elements. This circuit was then tested in simulation and experimentally, and it was utilized in a chaotic oscillator circuit. In a study conducted by Yeşil and Babacan [21], two different memcapacitor emulator circuits were designed. The first circuit was designed using two CCIIs, a multiplier, and four passive elements, while the second circuit was designed using a CCII element, an operational transconductance amplifier (OTA), a multiplier, and three capacitors. Simulation results for both circuits are given, but only two CCII-based emulator circuits are experimentally studied.Two memcapacitor emulator circuits in grounded structure were proposed by Raj et al. [22] and tested in Chua's oscillator circuit. The first circuit contains three OTA elements, while the second circuit consists of two MO-OTA elements. Three passive elements are utilized in both circuits. Yuan et al. [23] proposed a new grounded memcapacitor emulator circuit. The circuit has been investigated both simulation and experimentally by using the chaotic oscillator circuit. The memcapacitor emulator is made of five OPAMPs, a multiplier and fourteen passive elements. A memcapacitor emulator circuit designed by Konal and Kacar [24] utilizes two OTAs, a multiplier circuit and four passive elements. Although the circuit is electronically adjustable, it is limited to operating at frequencies between 1 Hz and 10 Hz. The active element numbers of the emulator circuits of the studies in this grounded structure [18-24] are high.

In this study, a grounded new memcapacitor emulator circuit is proposed. It consists of one fully differential second-generation current conveyor (FDCCII), one multiplier, three capacitors and two PMOS transistors which act like electronically adjustable resistor. Therefore, the variable part of memconductance can be controlled by biasing voltage. LTspice program was used to simulate the proposed circuit throughout the design process. Frequency response, temperature, and Monte Carlo analyses were carried out to validate the circuit's functionality. In addition, the adjustable resistor was tested at different values to demonstrate that the circuit can be adjusted electronically. The simulation results agree with the mathematical results presented in the article.

2. PROPOSED MEMCAPACITOR EMULATOR CIRCUIT

The memcapacitor element is defined by the nonlinear relationship between sigma (σ) and flux (φ) as seen in Equation (1). The sigma (σ) used in the memcapacitor equation is the integral of the charge. The memcapacitor equation can be expressed in terms of charge and voltage, if the sigma and the flux in the equation are taken as the derivative of time [25]. If both the numerator and the denominator of the expression in Equation (1) are derived with respect to time, the memcapacitor equation can be defined in terms of charge and voltage as in Equation (2). By rearranged Equation (2), the equation of the charge-controlled invert memcapacitor is obtained as in Equation (3) [26].

$$C_M = \frac{d\sigma}{d\varphi} \tag{1}$$

$$C_M = \frac{\frac{d\sigma}{dt}}{\frac{d\varphi}{dt}} = \frac{q(t)}{V(t)} \tag{2}$$

$$V_C(t) = C_M^{-1}\left[\int q(\tau)d\tau\right]q(t) \tag{3}$$

The schematic representation of FDCCII element used in the proposed memcapacitor emulator is shown in Figure 1.

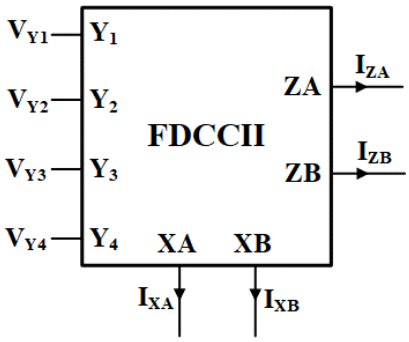

Figure 1. Schematic representation of the FDCCII element.

The current-voltage relationships between the terminals of the element are shown in Equation (4). No current flows through the *Y* input terminals of the element.

$$\begin{bmatrix} V_{XA} \\ V_{XB} \\ I_{ZA} \\ I_{ZB} \end{bmatrix} = \begin{bmatrix} 1 & -1 & 1 & 0 & 0 & 0 \\ -1 & 1 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} V_{Y1} \\ V_{Y2} \\ V_{Y3} \\ V_{Y4} \\ I_{XA} \\ I_{XB} \end{bmatrix} \tag{4}$$

As illustrated in Figure 2, the proposed circuit employs one FDCCII element, one multiplier, three capacitors, and two PMOS transistors. These transistors are worked as an electronically adjustable resistor. The input voltage is applied to the *XA* terminal of the FDCCII element. The input current flowing through capacitor C_1 on terminal *XA* is given by Equation (5). The $I_{XA}(t)$ current flows in the opposite direction to the $I_{IN}(t)$ current, while it flows in the same direction as the $I_{ZA}(t)$ current, as seen in Equation (6).

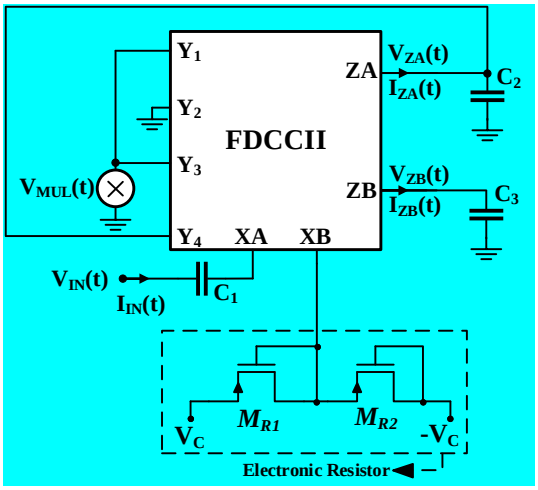

Figure 2. The proposed FDCCII based memcapacitor emulator circuit.

$$I_{IN}(t) = C_1 \frac{d(V_{IN}(t) - V_{XA}(t))}{dt} \tag{5}$$

$$I_{ZA}(t) = I_{XA}(t) = -I_{IN}(t) \tag{6}$$

The current $I_{ZA}(t)$ flowing through the capacitor C_2 creates the voltage $V_{ZA}(t)$. Since the current $I_{ZA}(t)$ is equal to the inverse of the current $I_{IN}(t)$, the integral of the current $I_{ZA}(t)$ gives the expression charge (q). If the Y_4 terminal is connected to the Z_A terminal in the circuit, the Equation (7) is obtained.

$$V_{Y4}(t) = V_{ZA}(t) = \frac{1}{C_2}\int I_{ZA}(t)dt = -\frac{1}{C_2}\int I_{IN}(t)dt = -\frac{q(t)}{C_2} \tag{7}$$

When the multiplier is positive, the product of $V_{ZA}(t)$ and $V_{ZB}(t)$ voltages is applied to the Y_1 and Y_3 terminals of the FDCCII. The $I_{ZB}(t)$ current is equal to the $I_{XB}(t)$ as seen in Equation (9).

$$V_{MUL}(t) = V_{ZA}(t)V_{ZB}(t) \tag{8}$$

$$I_{ZB}(t) = I_{XB}(t) = \frac{V_{XB}(t)}{R_{eq}} = \frac{-V_{Y1}(t)+V_{Y2}(t)+V_{Y4}(t)}{R_{eq}} = \frac{-V_{ZA}(t)V_{ZB}(t)+V_{ZA}(t)}{R_{eq}} \tag{9}$$

When the voltage $V_{ZA}(t)$ is substituted in the equation, the current $I_{ZB}(t)$ can be obtained as in Equation (10). The current $I_{ZB}(t)$ flowing through the capacitor C_3 creates the voltage $V_{ZB}(t)$ as in Equation (11).

$$I_{ZB}(t) = \frac{q(t)V_{ZB}(t)-q(t)}{R_{eq}C_2} \tag{10}$$

$$V_{ZB}(t) = \frac{1}{C_3}\int I_{ZB}(t)dt = -\frac{1}{R_{eq}C_2C_3}\int \left(q(t)V_{ZB}(t)-q(t)\right)dt \tag{11}$$

If $\lambda = \left(R_{eq}C_2C_3\right)^{-1}$ is defined in Equation (11) and by taking the derivative of both sides, Equation (12) is obtained.

$$V_{ZB}^{'}(t) + \lambda q(t)V_{ZB}(t) = \lambda q(t) \tag{12}$$

The solution of the first order inhomogeneous differential equation in Equation (12) is given in the appendix and the voltage $V_{ZB}(t)$ is found as in Equation (13).

$$V_{ZB}(t) = 1 - e^{-\frac{1}{R_{eq}C_2C_3}\int q(t)dt} \tag{13}$$

The voltage on the multiplier is given as in Equation (14).

$$V_{MUL}(t) = V_{ZA}(t)V_{ZB}(t) = \left(-\frac{q(t)}{C_2}\right)\left(1 - e^{-\frac{1}{R_{eq}C_2C_3}\int q(t)dt}\right) \tag{14}$$

Using Equation (4) and (14), the $V_{XA}(t)$ is obtained as Equation (15).

$$V_{XA}(t) = Y_1 - Y_2 + Y_3 = V_{MUL}(t) - 0 + V_{MUL}(t) \Rightarrow V_{XA}(t) = \left(-\frac{2q(t)}{C_2}\right)\left(1 - e^{-\frac{1}{R_{eq}C_2C_3}\int q(t)dt}\right) \tag{15}$$

When the $V_{XA}(t)$ is substituted in Equation (5), Equation (16) is obtained.

$$I_{IN}(t) = C_1\frac{d\left(V_{IN}(t) + \left(\frac{2q(t)}{C_2}\right)\left(1 - e^{-\frac{1}{R_{eq}C_2C_3}\int q(t)dt}\right)\right)}{dt} \tag{16}$$

By integrating both sides of Equation (16), the charge is obtained as shown in Equation (17).

$$\int I_{IN}(t)dt = C_1\int \frac{d\left(V_{IN}(t) + \left(\frac{2q(t)}{C_2}\right)\left(1 - e^{-\frac{1}{R_{eq}C_2C_3}\int q(t)dt}\right)\right)}{dt}dt$$
$$\Rightarrow q(t) = C_1V_{IN}(t) + \left(\frac{2C_1q(t)}{C_2}\right)\left(1 - e^{-\frac{1}{R_{eq}C_2C_3}\int q(t)dt}\right) \tag{17}$$

Inverse memcapacitance of the decremental charge controlled memcapacitor structure is obtained as shown in Equation (18).

$$C_M^{-1}\left[\int q(\tau)d\tau\right] = \frac{V_{IN}(t)}{q(t)} \Rightarrow C_M^{-1}\left[\int q(\tau)d\tau\right] = \frac{V_{in}(t)}{q(t)} = \underbrace{\frac{1}{C_1} - \frac{2}{C_2}}_{\text{Fix Part}} + \underbrace{\frac{2}{C_2}e^{-\frac{1}{R_{eq}C_2C_3}\int q(t)dt}}_{\text{Variable Part}} \tag{18}$$

When the multiplier is set to negative, inverse memcapacitance of the incremental charge controlled memcapacitor structure is obtained, as can be seen in Equation (19).

$$C_M^{-1}\left[\int q(\tau)d\tau\right]=\frac{V_{IN}(t)}{q(t)}\Rightarrow C_M^{-1}\left[\int q(\tau)d\tau\right]=\frac{V_{in}(t)}{q(t)}=\underbrace{\frac{1}{C_1}+\frac{2}{C_2}}_{\text{Fix Part}}-\underbrace{\frac{2}{C_2}e^{-\frac{1}{R_{eq}C_2C_3}\int q(t)dt}}_{\text{Variable Part}} \tag{19}$$

As shown in Equation (18) and (19), the variable part of the proposed emulator circuit can be modified with the R_{eq} resistor which can be adjusted by biasing voltage (V_C) and the fixed part can be modified with the C_1 capacitor.

3. SIMULATION RESULTS OF THE PROPOSED CIRCUIT

The FDCCII element used in the proposed circuit was designed using CMOS elements in LTspice. The internal structure of the FDCCII element is based on reference [27]. In the proposed circuit shown in Figure 2, the resistance value (R_{eq}) is 1.1 kΩ, since the voltage of the electronic resistor element (V_C) is set to 700 mV. The capacitors C_1, C_2 and C_3 are 20 pF, 100 pF and 50 pF, respectively. In all simulation studies, the input voltage amplitude is 300 mV and the frequency is 200 kHz. The input voltage and charge graphs for the decreasing and increasing structure of the emulator circuit are shown in Figure 3 (a) and Figure 3(b), respectively.

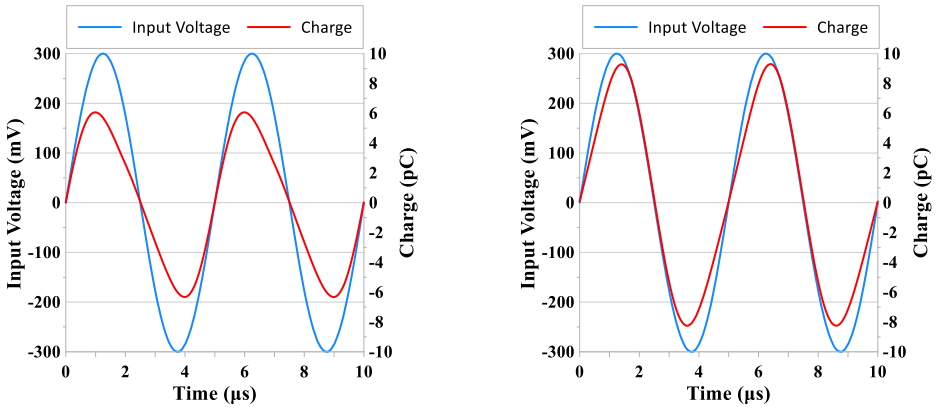

Figure 3. Input voltage and charge graph of (a) decremental structure (b) incremental structure.

The hysteresis loops in Figure 4 were obtained with an input signal frequency of 200 kHz, 300 kHz, and 1 MHz. It can be observed from Figure 4 that as the input frequency of the memcapacitor element is increased, the hysteresis loops become more linear. In Figure 5, the electronic adjustability of the hysteresis loop is examined according to the control voltage. When the control voltage of the electronic resistor is set to 500 mV, 700 mV, or 900 mV, the resistance values of electronic resistor are calculated as 3.6 kΩ, 1.1 kΩ, or 0.7 kΩ, respectively. According to Equation (18) and (19), it should be noted that the variable part increases as the resistance value decreases, in other words control voltage increases. It can be clearly seen from Figure 5 that the hysteresis loop of the circuit becomes linear as control voltage decreases.

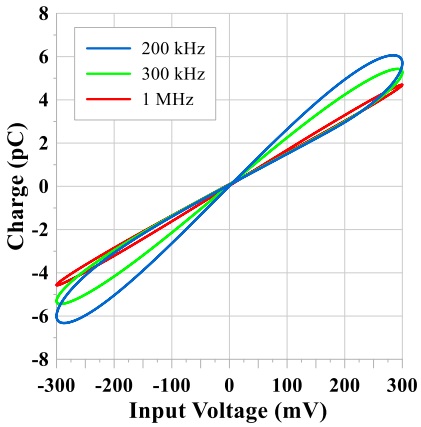

Figure 4. Hysteresis loops obtained at 200 kHz, 300 kHz and 1 MHz input frequencies.

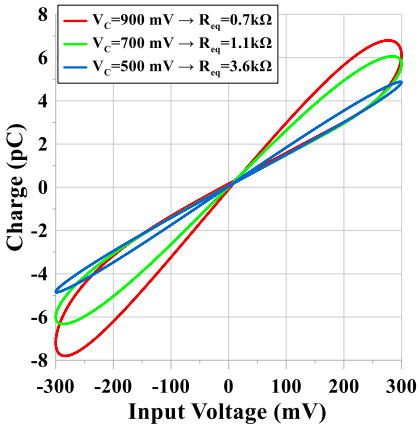

Figure 5. Hysteresis loops obtained at different resistance values.

So as to survey connectivity of memcapacitor emulator, different connections such as single and parallel of memcapacitor are depicted in Figure 6. When the hysteresis loops given in Figure 6 are examined, it is clearly observed that the slopes of hysteresis loops are altered depending on different connections. For instance, its slope increases in parallel connection, in other word memcapacitance enhances.

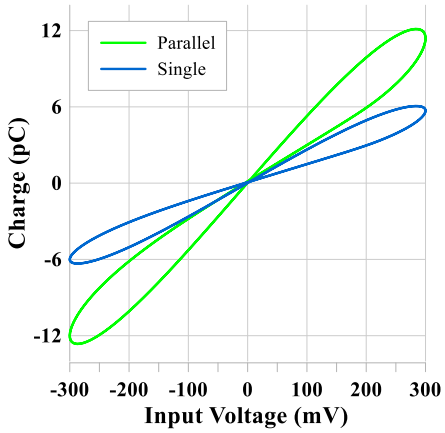

Figure 6. The hysteresis loops resulting from the single and parallel connection of the proposed memcapacitor emulator circuit.

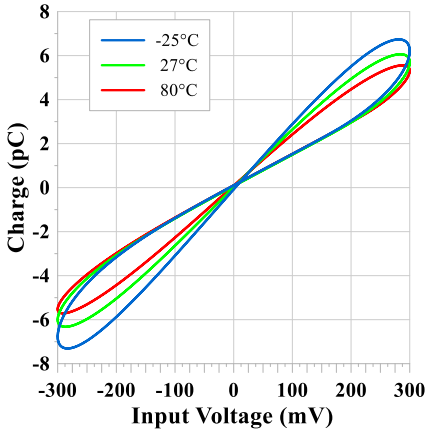

Figure 7. Hysteresis loops obtained at -25°C, 27°C and 80°C.

The temperature analysis of the proposed circuit was made at temperatures of -25°C, 27°C and 80°C. When examining Figure 7, it is seen that as the temperature increases, the hysteresis loop becomes linear but maintains its characteristic features. While performing Monte Carlo Analysis of the proposed emulator circuit, the *W* and *L* values of M_{R1}, M_{R2} MOSFETs used in the electronic resistor circuit and the tolerance values of capacitance values of C_1, C_2, C_3 capacitors were determined as 5%. Examining the hysteresis loops obtained after 50 iterations as shown in Figure 8 revealed that the circuit didn't change significantly at the 5% tolerance value.

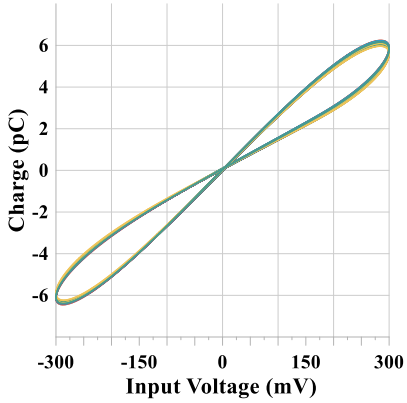

Figure 8. Monte Carlo analysis result obtained as a result of 50 iterations with 5% tolerance.

4. CONCLUSION

In this study, a charge-controlled memcapacitor emulator circuit based on FDCCII is presented. The proposed emulator circuit is simulated in the LTspice program. When the relationship between the input voltage and the charge is examined, it is seen that the closed hysteresis loop is close to the origin and has a symmetrical structure. In the hysteresis loops obtained at different input frequencies, it was observed that the hysteresis loops became linear as the frequency increased. The input voltage and frequency of the emulator circuit are kept constant and connected in a single and parallel configuration in the simulation. When the hysteresis loops obtained were examined, it was observed that the width of the hysteresis loop increased approximately twice as expected when the memcapacitor emulator circuits were connected in parallel. The circuit was tested at temperatures of -25°C, 27°C, and 80°C in order to analyze the effect of temperature on the circuit. When the obtained data were examined, it was seen that the circuit became linear as the temperature increased, but kept its general characteristic structure. After running 50 iterations of a Monte Carlo analysis on the circuit with a tolerance value of 5%, it was observed that while the circuit element values changed the amplitude of the hysteresis loop slightly, the loop's characteristics remained the same.

Appendix

The f(x) and g(x) are defined as in Equation (16).

$$V_{ZB}'(t) + \underbrace{\lambda q(t) V_{ZB}(t)}_{f(x)} = \underbrace{\lambda q(t)}_{g(x)} \tag{16}$$

The general solution of the inhomogeneous differential equation obtained in equation (16) is as in equation (17).

$$V_{ZB}(t) = e^{-\int f(x)dx}\left[\int e^{\int f(x)dx} g(x)dx + C\right] \tag{17}$$

When the expressions *f(x)* and *g(x)* defined in equation (16) are replaced in equation (17) and the equation is arranged, the expression $V_{ZB}(t)$ is obtained as in equation (18).

$$V_{ZB}(t) = \frac{\lambda}{\lambda} + Ce^{-\lambda\int q(t)dt} \tag{18}$$

To find the constant value of *C*, if the initial values are assumed to be zero and equation (18) is substituted in equation (11), the expression *C* is obtained as in equation (19).

$$C = -\frac{\lambda}{\lambda}e^{\lambda\int q(0)dt} \Rightarrow C = -1 \tag{19}$$

If the constant *C* and the expression λ are substituted in equation (18), the expression $V_{ZB}(t)$ becomes as in equation (20).

$$V_{ZB}(t) = 1 - e^{-\frac{1}{R_{eq}C_2C_3}\int q(t)dt} \tag{20}$$

Acknowledgment

This work was supported by the Scientific and Technological Research Council of Turkey (TUBITAK) under Project 119E458.

Author Contributions

The authors contributed equally to the study.

Conflict of Interest

The authors of the article declare that there is no conflict of interest between them.

REFERENCES

[1] L.O. Chua "Memristor—The Missing Circuit Element", IEEE Transactions on Circuit Theory, vol. 18, no. 5, pp. 507–519, 1971.

[2] D.B. Strukov, G.S. Snider, D.R. Stewart, and R.S. Williams "The missing memristor found", Nature, vol. 453, no. 7191, pp. 80–83, 2008.

[3] D.S. Yu, Y. Liang, H.H.C. Iu, and Y.-H. Hu "Mutator for transferring a memristor emulator into meminductive and memcapacitive circuits", Chinese Physics B, vol. 23, no. 7, p. 070702, 2014.

[4] D.S. Yu, Y. Liang, H. Chen, and H.H.C. Iu "Design of a practical memcapacitor emulator without grounded restriction", IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 60, no. 4, pp. 207–211, 2013.

[5] X.Y. Wang, A.L. Fitch, H.H.C. Iu, and W.G. Qi "Design of a memcapacitor emulator based on a memristor", Phys Lett A, vol. 376, no. 4, pp. 394–399, Jan. 2012.

[6] Y.V. Pershin and M. Di Ventra "Memristive circuits simulate memcapacitors and meminductors", Electron Lett, vol. 46, no. 7, p. 517, 2010.

[7] D. Biolek and V. Biolkova "Mutator for transforming memristor into memcapacitor", Electron Lett, vol. 46, no. 21, p. 1428, 2010.

[8] D. Yu, Y. Liang, H.H.C. Iu, and L.O. Chua "A universal mutator for transformations among memristor, memcapacitor, and meminductor", IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 61, no. 10, pp. 758–762, Oct. 2014.

[9] F.J. Romero, D.P. Morales, A. Godoy, F G. Ruiz, I. M. Tienda, A. Ohata, N. Rodriguez "Memcapacitor emulator based on the Miller effect", International Journal of Circuit Theory and Applications, vol. 47, no. 4, pp. 572–579, Apr. 2019.

[10] Z.G. Çam Taşkıran, M. Sağbaş, U.E. Ayten, and H. Sedef "A new universal mutator circuit for memcapacitor and meminductor elements", AEU - International Journal of Electronics and Communications, vol. 119, 2020.

[11] A. Singh and S.K. Rai "VDCC-Based Memcapacitor/Meminductor Emulator and Its Application in Adaptive Learning Circuit", Iranian Journal of Science and Technology - Transactions of Electrical Engineering, vol. 45, no. 4, pp. 1151–1163, Dec. 2021.

[12] F. Wang and F. Wang "Floating Memcapacitor Based on Knowm Memristor and Its Dynamic Behaviors", IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 69, no. 12, pp. 5134–5138, 2022.

[13] A. Sinha, B. Aggarwal, S.K. Rai, and S. Gautam "Current Conveyor Transconductance Amplifier (CCTA) based Grounded Memcapacitor Emulator", International Journal of Electrical and Electronics Research, vol. 10, no. 3, pp. 442–446, 2022.

[14] M.P. Sah, C. Yang, R.K. Budhathoki, H. Kim, and H. J. Yoo "Implementation of a memcapacitor emulator

with off-the-shelf devices", Elektronika ir Elektrotechnika, vol. 19, no. 8, pp. 54–58, 2013.

[15] Q. Zhao, C. Wang, and X. Zhang "A universal emulator for memristor, memcapacitor, and meminductor and its chaotic circuit", Chaos, vol. 29, no. 1, p. 013141, 2019.

[16] P.K. Sharma, R.K. Ranjan, F. Khateb, and M. Kumngern "Charged controlled MEM-element emulator and its application in a chaotic system", IEEE Access, vol. 8, pp. 171397–171407, 2020.

[17] D. Yu, X. Zhao, T. Sun, H.H.C. Iu, and T. Fernando "A simple floating mutator for emulating memristor, memcapacitor, and meminductor", IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 67, no. 7, pp. 1334–1338, 2020.

[18] M.E. Fouda and A.G. Radwan "Charge controlled memristor-less memcapacitor emulator", Electron Lett, vol. 48, no. 23, p. 1454, 2012.

[19] A.L. Fitch, H.H.C. Iu, and D.S.Yu "Chaos in a memcapacitor based circuit", Proceedings - IEEE International Symposium on Circuits and Systems, no. 3, pp. 482–485, 2014.

[20] F. Yuan and Y. Li "A chaotic circuit constructed by a memristor, a memcapacitor and a meminductor", Chaos, vol. 29, no. 10, 2019.

[21] A. Yesil and Y. Babacan "Electronically Controllable Memcapacitor Circuit with Experimental Results", IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 68, no. 4, pp. 1443–1447, 2021.

[22] N. Raj, R.K. Ranjan, and A. James "Chua's Oscillator With OTA Based Memcapacitor Emulator", IEEE Trans Nanotechnol, vol. 21, pp. 213–218, 2022.

[23] F. Yuan, Y. Li, G. Wang, G. Dou, and G. Chen "Complex Dynamics in a Memcapacitor-Based Circuit", Entropy, vol. 21, no. 2, p. 188, Feb. 2019.

[24] M. Konal and F. Kacar "Electronically Tunable Memcapacitor Emulator Based on Operational Transconductance Amplifiers", Journal of Circuits, Systems and Computers, vol. 30, no. 05, p. 2150082, Apr. 2021.

[25] D. Biolek, M. di Ventra, and Y.V. Pershin "Reliable SPICE simulations of memristors, memcapacitors and meminductors", Radioengineering, vol. 22, no. 4, pp. 945–968, 2013.

[26] M. Di Ventra, Y.V. Pershin, and L.O. Chua "Circuit Elements With Memory: Memristors, Memcapacitors, and Meminductors", Proceedings of the IEEE, vol. 97, no. 10, pp. 1717–1724, 2009.

[27] A.A. El-Adawy, A.M. Soliman, and H.O. Elwan "A novel fully differential current conveyor and applications for analog VLSI", IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, vol. 47, no. 4, pp. 306–313, 2000.