



Research Paper

A Five Level SC Inverter with Reduced Switch Count and Self Balancing Capability

**B. Hemanth KUMAR^{1,a*}, K. JANARDHAN^{2,b}, V.S. CHANDRIKA^{3,c}, G.G. Raja SEKHAR^{4,d},
Deepak Prakash KADAM^{5,e}, Dhananjay KUMAR^{6,f}**

^{1,2}School of Engineering, Department of EEE, Mohan Babu University (Erst while Sree Vidyanikethan Engineering College), Tirupati, India

³Department of EEE, KPR Institute of Engineering and Technology, Coimbatore, India

⁴Department of EEE, Koneru Lakshmaiah Education Foundation, Vaddeswaram, Guntur, Andhra Pradesh, India.

⁵Department of EEE, MET Institute of Engineering, Nashik, India

⁶Department of Industrial Research Design and Development (IRDD), Aartech Solonics Ltd., Mandideep, India

*hemub09@gmail.com

Received: 13.03.2023

Accepted: 23.09.2023

Abstract: Multilevel inverters (MLIs) have become a favoured option for medium voltage and high power DC to AC conversion applications to assure high power level cascade type inverter which accepts multiple/single DC sources and offers combined AC output for appropriate voltage and frequency. MLIs provide various benefits over two-level inverters, including lower dv/dt , the capacity to handle greater voltage levels, a quasi-sinusoidal output waveform, and lower Total Harmonic Distortion (THD), among others. The biggest problem in adopting the MLI is the increasing number of switches and its design. MLIs based on switched capacitors (SC) for boost-type DC-AC converters often demonstrate a trade-off among switch voltage rating and switch count. This work introduces a new 5-level (5L) SC inverter by adding a switched capacitor module into the usual 3L neutral point clamped inverter leg (NPC). The SC unit consists of one bidirectional switch and two capacitors capable of withstanding one-quarter of the DC voltage. When compared to typical 5L inverters, such as standard NPC and active NPC designs, the new approach in addition reduces the amount of switches but also shortens the topology. The proposed FLSCI has been examined by using several PWM techniques. The simulation and hardware results showed that the presented FLSCI is ideal for a broad variety of applications.

Keywords: Multilevel inverter, Switched capacitor, Harmonic distortion, DC-AC inverter, Voltage balancing.

1. Introduction

Increasing the switching frequency in a simple two-level inverter reduces the output voltage's harmonics, resulting in increased voltage stresses and switching losses due to a reduction in the output voltage's step count. The drawbacks of the two-level inverter pique interest in multilayer inverters (MLIs). MLI was introduced in 1991, and its progress has been rapid over time.

MLIs are widely used in several industries today, especially for medium voltage and high power applications [1]. MLIs produce a staircase waveform that closely resembles a sinusoidal signal and has less harmonic distortion by using more DC supply and switches [2]. Over conventional two-level inverters, MLIs provide a number of advantages, including a greater basic output voltage, a reduced switching loss and common mode voltage, a decrease in EMI, and a decrease in THD [3]. Because of these advantages, MLIs are applicable to a variety of applications, including HVDC, FACTS, electric vehicles, and solar power systems. The most common MLI topologies are the CHB inverter, created by Peng et al., the flying capacitor (FC) inverter, found by Meynard et al., and the NPC inverter, discovered by Nabae et al. FC utilizes capacitors in a ladder structure, while NPC uses diodes. NPC

How to cite this article

B. Hemanth Kumar, K. Janardhan et al., "A Five Level SC Inverter with reduced switch count and self-balancing capability," *El-Cezeri Journal of Science and Engineering*, Vol. 10, No. 3, 2023, pp. 517-525.

ORCID: ^a0000-0001-6282-5102; ^b0000-0001-5640-3667; ^c0000-0001-8417-4742; ^d0000-0003-3042-8035; ^e0000-0002-5325-9513; ^f0000-0002-1764-9928

and FC both need more power components to achieve greater inverter levels, and they also suffer with voltage imbalance [3]. In the CHB topology, H-bridge cells are linked in series, and the modular architecture is established by requiring each cell to have its own DC source. This CHB architecture is advantageous for both single-phase and three-phase power conversion. CHB MLIs are suited for PV applications and are one of the three core MLI topologies.

However, the total amount of output levels of these MLIs is limited by various inherent restrictions. NPC, for example, uses 12 clamping diodes in addition to eight active power switches, while FC utilizes six capacitors for each phase of 5L structure. Auxiliary circuits are also required to balance the voltages of the four DC rail capacitors utilized in the 5L NPC. The term "electronic commerce" refers to the sale of electronic goods. Numerous innovative structures of 3-ph 5L inverters are created in latest years to overcome the aforementioned restrictions. The 5-level classical active NPC inverter described in [4] in particular incorporates parts of 3L ANPC and 3L FC.

The 5L nested NPC inverter presented in [5], on the other hand, utilizes two FC and 2 bidirectional power switches. Here actuality, the standing voltage for each switch in the nested NPC is the identical as in the classic ANPC. And T-type nested NPC 5L inverter shown in [6] has fewer bi-directional switch than in NNPC, however it needs wide advanced control technology. These cutting-edge inverters have fewer components than ordinary 5L FC and NPC inverters. To make sure that voltage re-mains maintained about one-quarter with respect to DC voltage, the voltage across capacitor should be maintained, such that a difficult management method is necessary.

Furthermore, [7] present a 5L asymmetric hybrid HB inverter made of a bridge leg and a T-model leg to diminish the switching device count. In [8] develops a hybrid 5L-ANPC FB inverter for single-phase applications. Because each of the 2 inverters has 2 asymmetric legs, their 3-phase extensions need six legs. To regulate the MLIs, many modulation approaches are available in the literature [9–11].

In this work, the aim is to directly derive a new 5L inverter among the existing 3L NPC design utilizing the minimum supplementary circuit. By instantly inserting a SC unit into a 3L NPC phase-leg, a novel 5L inverter is built based on this notion. As a consequence, mature 3L NPC modules might be used to build the novel 5L inverter. Furthermore, this innovative inverter features an inherent balanced capacitor, an easy circuit design and control method, a low common-mode voltage (CMV) and switching frequency.

This paper is organized with V sections; Section-I deals with the introduction and literature part of exiting work. The proposed FLSCI is explained in detail in section II. The simulation results of FLSCI and discussion are reported in section III. The experimental analysis and comparative analysis of proposed FLSCI is reported in section IV and finally concluded in section V.

2. Proposed Five-Level Switched Capacitor Inverter (FLSCI)

Figure 1 depicts the proposed FLSC inverter. Its phase leg is created immediately by putting a SC unit into the usual 3L NPC phase-leg composed of S_1 , S_3 , S_4 , S_5 D_1 and D_2 . The SC unit is made up of 4 capacitors C_1 , C_2 , C_3 and C_4 as well as one bidirectional switch S_2 , which is often made up of two anti-series linked transistors. C_1 , C_2 are DC link capacitors. The suggested FLSC inverter may be realized by merging several commercial 3L NPC module among a less voltage switched capacitor module. This is quite useful in terms of reducing design difficulties and expediting commercialization. To ease analysis, all components used in the 5L inverter are considered to be perfect, and because all capacitors are so large, their voltages may seem constant. For each phase of FLSCI, five switches S_1 to S_5 are used, as illustrated in Fig. 1. At any one moment, just one of S_1 , S_2

or S_3 is switched ON, while the other two are turned OFF. The two switches, S_4 and S_5 function in a complimentary way.

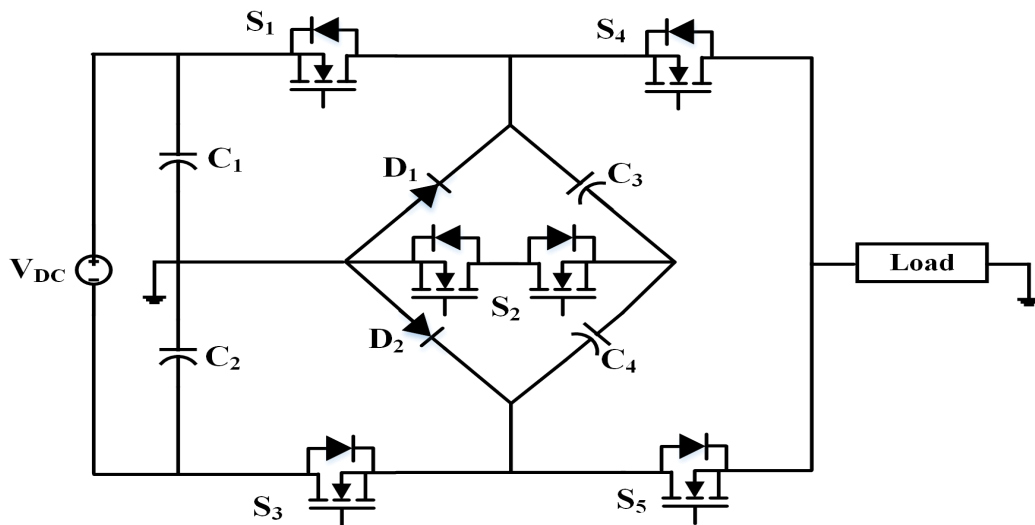


Figure 1. Proposed five level switched capacitor inverter (FLSCI)

Table 1. Switching logic of proposed FLSCI Topology

Voltage Level	S_1	S_2	S_3	S_4	S_5	C_3	C_4
$+0.5V_{DC}$	1	0	0	1	0	C	C
$+0.25V_{DC}$	0	1	0	1	0	D	N
0	0	0	1	1	0	C	C
$-0.25V_{DC}$	0	1	0	0	1	N	D
$-0.5V_{DC}$	0	0	1	0	1	C	C

Table 1 shows the switching logic of presented FLSCI. It should be noted that 0 and 1 reflect the OFF and ON states of the associated switches, correspondingly. The states of capacitors are denoted by the letters N, D and C' which stand for idle, discharging and charging respectively. Figure 2 depicts the state circuits for different voltage levels.

3. Simulation Results

In this work, to validate the proposed FLSCI topology, MATLAB simulation analysis is carried out. Different PWM techniques are used to produce pulses to the switches in FLSCI. The simulation parameters are considered as: RL load ($R=100\Omega$ & $L=110mH$), DC supply is 600V and sampling time is $1/2500sec$. The SCNLBI phase current and voltage wave forms for diverse values of modulation indices by using sinusoidal pulse width modulation (PWM) [12], offset PWM [13], total harmonic injection(THI) PWM[14] & space vector PWM[15] are shown in Fig.4 at unity modulation index, which confirm the validation of presented FLSCI topology.

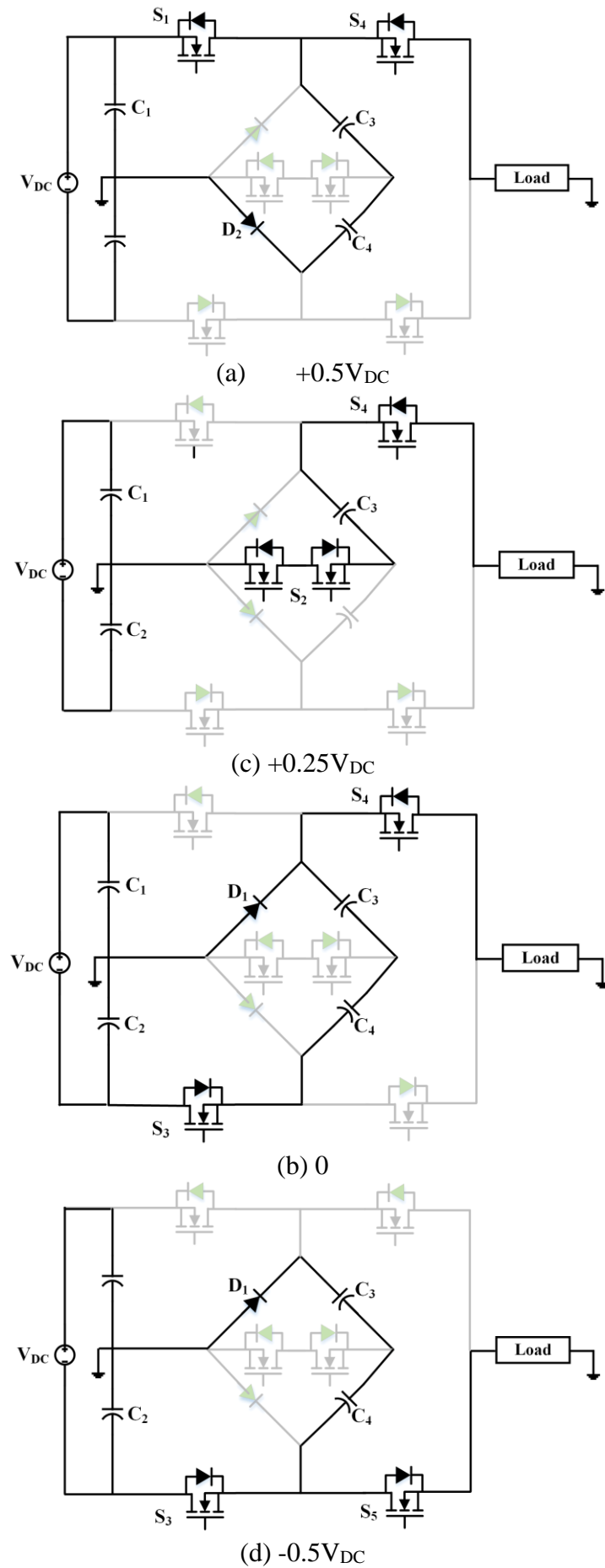
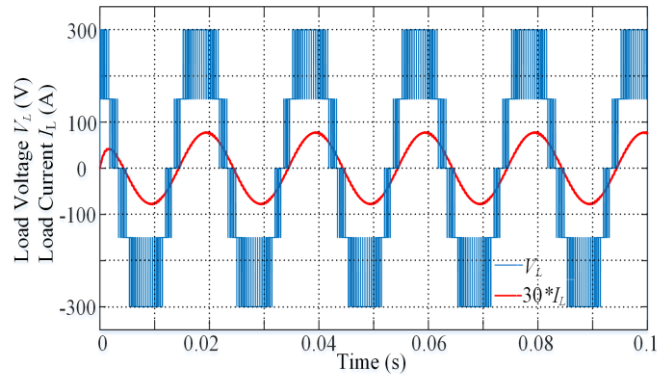
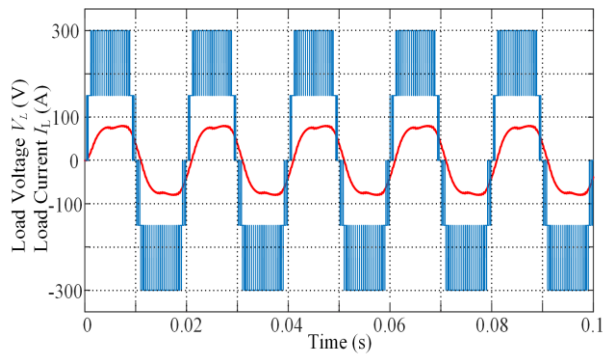


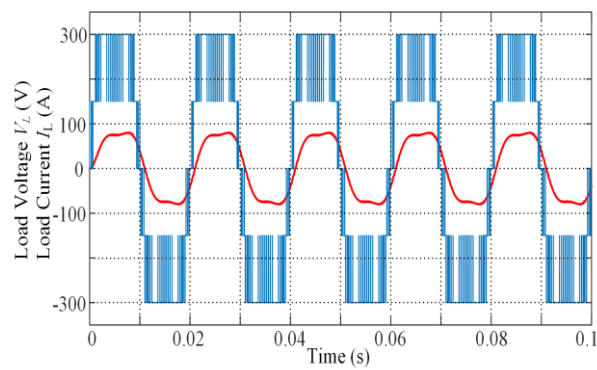
Figure 2. Conduction path of proposed FLSCI for different voltage levels



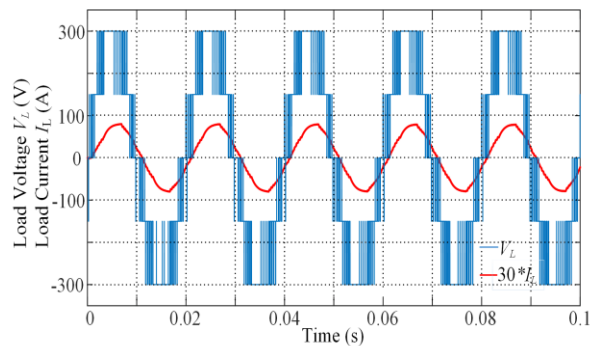
(a)



(b)



(c)



(d)

Figure 3. FLSCI inverter load current and voltage (a) SPWM (b) Offset PWM and (c) SVPWM and (d) THI-PWM techniques.

4. Hardware Results

In order to validate the proposed FLSCI topology, hardware results have been presented for different modulation techniques such as sinusoidal PWM, Offset PWM THI PWM and SVPWM techniques.

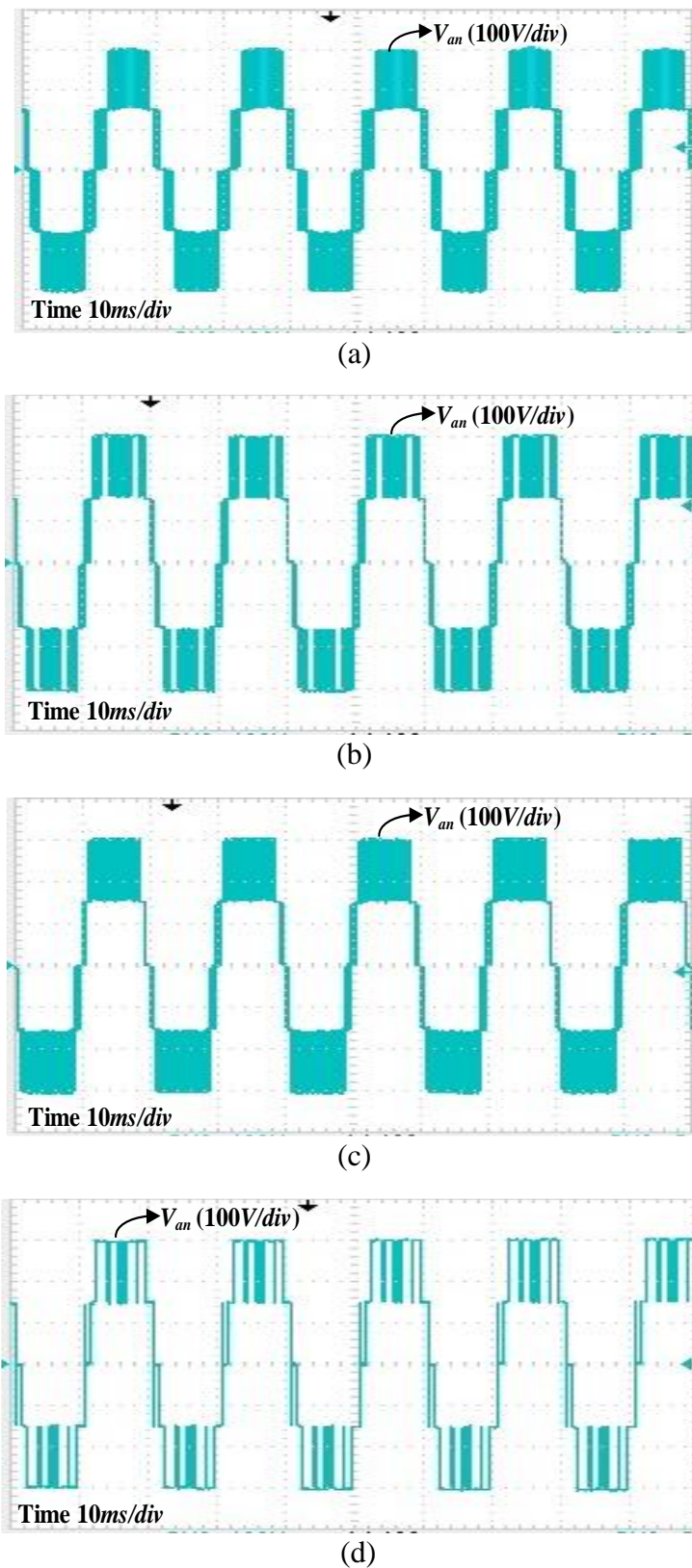


Figure 4. Proposed FLSCI hardware load voltage by using (a) SPWM technique, (b) THI-PWM technique and (c) Offset PWM technique and (d) SVPWM Technique.

The parameters considered for hardware results are same as simulation parameters. The FLSC inverter phase voltage by using SPWM, THI-PWM, Offset PWM and SVPWM techniques are shown in Fig .4 at unity modulation index. These results validate the effectiveness of proposed FLSCI topology. The comparison of proposed FLSCI topology in terms of switch count, capacitors count, diode count, voltage stress, voltage gain and self balancing capability with the existing 5L MLIs and three conventional MLIs is shown in Table 2. As the proposed 5L MLI topology requires lower components such that number of gate driver circuit's requirement also less, which makes overall cost and complexity to design the proposed 5L MLI is less compared to existing such 5L MLIs.

Table 2. Comparison of various FL MLIs

Topology	No. of Switches	No. of Capacitors	No. of Diodes	Output voltage gain	Maximum blocking voltage	Self balancing capability
CHB MLI	8	0	0	1	1	--
FC MLI	8	10	0	1	1	No
DC MLI	8	4	6	1	1	No
[16]	7	1	4	2	4	Yes
[17]	8	1	0	2	4	Yes
[18]	6	2	0	1	2	No
[19]	8	2	0	1	2	No
[20]	12	5	0	1	1	No
[21]	6	1	2	1	3	No
[22]	8	1	0	1	3	No
[23]	6	1	0	1	3	No
[24]	8	1	0	1	3	No
Proposed FLSCI	6	2	2	1	2	Yes

5. Conclusion

A new 5L inverter is constructed in this work by incorporating a low-voltage switched capacitor unit consisting of a two-way switch and a couple of capacitors forms a typical 3L NPC phase-leg. In contrast to a traditional 5L neutral point clamped topology, that equalizes DC link voltage across capacitors with additional balancing circuits or advanced logical algorithms, the unique design diminishes the components count while maintaining reactive power capabilities. The comparison analysis reveals the effectiveness of the presented FLSCI topology in terms of lower components like power switches, diodes and capacitors, inherent balance, voltage boosting and blocking capability. Different PWM techniques such as SPWM, THIPWM, Offset PWM and SVPWM have been implemented on FLSCI. MATLAB simulation and hardware results show the validation and effectiveness of presented FLSCI topology.

Acknowledgments

This work was supported by the Sree Vidyanikethan Educational Trust (SVET), Tirupati, Andhra Pradesh, India.

Authors' Contributions

The authors confirm contribution to the paper as follows: study conception and design: BHK, KJ; data collection: VSC, GGR; analysis and interpretation of results: BHK, DPK, DK; draft manuscript preparation: BHK. All authors reviewed the results and approved the final version of the manuscript.

Competing interests

The authors declare that they have no competing interests.

References

- [1]. J. Rodríguez, S. Bernet, B. Wu, J. O. Pontt, and S. Kouro, "Multilevel voltage-source-converter topologies for industrial medium-voltage drives," *IEEE Transactions on Industrial Electronics*, vol. 54, no. 6, pp. 2930-2945, 2007.
- [2]. J. Rodríguez, L. G. Franquelo, S. Kouro, J. I. Leon, R. C. Portillo, M. A. M. Prats and M. A. Perez, "Multilevel converters: An enabling technology for high-power applications," *Proceedings of the IEEE*, vol. 97, no. 11, pp. 1786-1817, 2009.
- [3]. B. Hemanth Kumar, S. Prabhu, K. Janardhan, V. Arun and S. Vivekanandan, "A Switched Capacitor Based Multilevel Boost Inverter for Photovoltaic Applications," *Journal of Circuits, Systems and Computers*, vol. 32, no. 04, 2350057, 2023.
- [4]. P. Barbosa, P. Steimer, and J. Steinke et al., "Active neutral-pointclamped multilevel converters," in *Proc. 36th IEEE Power Electron. Spec. Conf.*, 2005, pp. 2296-2301.
- [5]. J. Li, J. Jiang, and S. Qiao, "A space vector pulse width modulation for five-level nested neutral point piloted converter," *IEEE Trans. Power Electron.*, vol. 32, no. 8, pp. 5991-6004, Aug. 2017.
- [6]. A. Bahrami and M. Narimani, "A New Five-Level T-Type Nested Neutral Point Clamped (T-NNPC) Converter," *IEEE Trans. Power Electron.*, vol. 34, no. 11, pp. 10534-10545, Nov. 2019.
- [7]. Sung-Jun Park, Feel-Soon Kang, Man Hyung Lee and Cheul-U Kim, "A New Single-Phase Five-Level PWM Inverter Employing A Deadbeat Control Scheme," *IEEE Trans. Power Electron.*, vol. 18, no. 3, pp. 831-843, May 2003.
- [8]. L. Zhang, Z. Zheng, and C. Li et al., "A Si/SiC Hybrid Five-Level Active NPC Inverter With Improved Modulation Scheme," *IEEE Trans. Power Electron.*, vol. 35, no. 5, pp. 4835-4846, May 2020.
- [9]. B. Hemanth Kumar, M. M. Lokhande, "Investigation of switching sequences on a generalized SVPWM algorithm for multilevel inverters," *Journal of Circuits, Systems and Computers*, vol. 28, no. 02, 1950036, 2019.
- [10]. B. H. Kumar, M. M. Lokhande, "An enhanced space vector PWM for nine-level inverter employing single voltage source," *IEEE Transportation Electrification Conference (ITEC)*, pp. 1-6, 2017.
- [11]. B. H. Kumar, M. M. Lokhande, "Space Vector Pulse Width Modulation for Multilevel Inverter - A Survey," *4th International Conference for Convergence in Technology (I2CT)*, pp. 1-6, 2018.
- [12]. W. Song, X. Feng, and K. M. Smedley, "A carrier-based PWM strategy with the offset voltage injection for single-phase three-level neutral-point-clamped converters," *IEEE Transactions on Power Electronics*, vol. 28, no. 3, pp. 1083-1095, 2012.
- [13]. B. P. McGrath, D. G. Holmes, and T. Meynard, "Reduced PWM harmonic distortion for multilevel inverters operating over a wide modulation range," *IEEE Transactions on power electronics*, vol. 21, no. 4, pp. 941-94, 2006.
- [14]. W. Subsingha, "A comparative study of sinusoidal PWM and third harmonic injected PWM reference signal on five level diode clamp inverter," *Energy Procedia*, vol. 89, pp.137-148, 2016.
- [15]. B. H. Kumar, K. Janardha, R. S. Kumar, J. R. Rahul, A. R. Singh, R. Naidoo, and R. C. Bansal, "An Enhanced Space Vector PWM Strategies for Three Phase Asymmetric Multilevel Inverter," *International Transactions on Electrical Energy Systems*, Feb 2023. <https://doi.org/10.1155/2023/5548828>.
- [16]. M. J. Sathik, Z. Tang, Y. Yang, K. Vijayakumar and F. Blaabjerg, "A New 5-Level ANPC

- Switched Capacitor Inverter Topology for Photovoltaic Applications,” in *Proc. 45th Annu. Conf. IEEE Ind. Electron. Soc.*, Lisbon, Portugal, 2019, pp. 3487-3492.
- [17]. Y. P. Siwakoti, A. Palanisamy, A. Mahajan, S. Liese, T. Long and F. Blaabjerg, “Analysis and Design of a Novel Six-Switch Five-Level Active Boost Neutral Point Clamped Inverter,” *IEEE Trans. Ind. Electron.* vol. 67, no. 12, pp. 10485-10496, Dec. 2020.
- [18]. W. A. Pineda C. and C. Rech, “Modified Five-Level ANPC Inverter with Output Voltage Boosting Capability,” in *Proc. 45th Annu. Conf. IEEE Ind. Electron. Soc.*, Lisbon, Portugal, 2019, pp. 3355-3360.
- [19]. A. Bahrami and M. Narimani, “A New Five-Level T-Type Nested Neutral Point Clamped (T-NNPC) Converter,” *IEEE Trans. Power Electron.*, vol. 34, no. 11, pp. 10534-10545, Nov. 2019.
- [20]. J. Li, J. Jiang, and S. Qiao, “A space vector pulse width modulation for five-level nested neutral point piloted converter,” *IEEE Trans Power Electron.*, vol. 32, no. 8, pp. 5991-6004, Aug. 2017.
- [21]. E. Burguete, J. López and M. Zabaleta, “A New Five-Level Active Neutral-Point-Clamped Converter With Reduced Overvoltages,” *IEEE Trans. Ind. Electron.*, vol. 63, no. 11, pp. 7175-7183, Nov. 2016.
- [22]. H. Wang, L. Kou, Y. F. Liu, and P.C. Sen, “A New Six-Switch Five Level Active Neutral Point Clamped inverter for PV Applications,” *IEEE Trans. Power Electron.*, vol. 32, no. 9, pp. 6700-6715, Sep. 2017.
- [23]. T. B. Soeiro, R. Carballo, J. Moia, G. O. Garcia, and M. L. Heldwein “Three-phase five-level Active Neutral Point Clamped Converters for Medium Voltage Applications,” in *Proc. Brazilian Power Electron. Conf.*, Oct. 27-31, 2013, pp. 85-91.
- [24]. P. Barbosa, P. Steimer, and J. Steinke et al., “Active neutral-point-clamped multilevel converters,” in *Proc. 36th IEEE Power Electron. Spec. Conf.*, 2005, pp. 2296-2301.