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Research Article

Comparison of Performance Analysis of CMOS-based VDCC and Differantial Amplifiers FGMOS-based VDCC Circuits and Its Filter Application

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Abstract: This paper presents a comparison and performance analysis of CMOS-based VDCC (Voltage Differencing Current Conveyor) circuits and differential amplifier FGMOS-based circuits. Differential amplifiers at the input stage of the VDCC circuit are designed using FGMOS instead of CMOS. Designing the differential amplifiers in the input stages of the VDCC circuit using FGMOS instead of CMOS amplifies the input signal of the circuit, providing a significant increase in linearity and voltage following properties. At the same time by using FGMOS transistors, the input stage of the circuit, which provides arithmetic calculations, is simplified. A three-input single output (TISO) type band-pass filter application is given to show the versatility of the VDCC circuit topology. The THD value of the CMOS-based VDCC filter circuit is found to be 15.99%. The THD value of the proposed differential amplifiers FGMOS-based VDCC filter circuit is found to be 1.03%. Theoretical analysis results confirm the simulation results. The presented CMOS and FGMOS-based band-pass filters are simulated using TSMC CMOS 0.18 µm technology with V_{DD}, a power supply voltage equal to 0.9 V. The proposed circuit topology will be an essential reference in the literature for researchers to design new linearly tunable filters.

Keywords: *Voltage Differencing Current Conveyor (VDCC), Floating Gate MOS (FGMOS), Voltage-Mode Band-Pass Filter.*

CMOS Tabanlı VDCC ve Fark Kuvvetlendiricisi FGMOS Tabanlı VDCC Devrelerinin Performans Analizinin Karşılaştırılması ve Filtre Uygulaması

Öz. Bu makale, CMOS tabanlı VDCC (Voltage Differencing Current Conveyor) devreleri ile fark kuvvetlendiricisi FGMOS tabanlı VDCC devrelerinin karşılaştırmasını ve performans analizini sunar. VDCC devresinin giriş aşamasındaki fark kuvvetlendiricileri, CMOS yerine FGMOS kullanılarak tasarlanır. VDCC devresinin giriş katlarındaki fark kuvvetlendiricilerinin CMOS yerine FGMOS kullanılarak tasarlanması, devrenin giriş sinyalini yükselterek doğrusallık ve voltaj takip etme özelliklerinde önemli bir artış sağlar. Aynı zamanda FGMOS transistörler kullanılarak devrenin aritmetik hesaplamaları sağlayan giriş aşaması basitleştirilir. VDCC devre topolojisinin çok yönlülüğünü göstermek için üç girişli tek çıkışlı (TISO) tip bant geçiren filtre uygulaması verilir. CMOS tabanlı VDCC filtre devresinin THD değeri %15.99 olarak bulunur. Önerilen fark kuvvetlendiricisi FGMOS tabanlı VDCC filtre devresinin THD değeri %1.03 olarak bulunur. Teorik analiz sonuçları, simülasyon sonuçlarını doğrulamaktadır. Sunulan CMOS ve FGMOS tabanlı bant geçiren filtreler, 0.9 V'a eşit bir güç kaynağı voltajı olan V_{DD} ile TSMC CMOS 0,18 µm teknolojisi kullanılarak simüle edilir. Önerilen devre topolojisi, araştırmacıların doğrusal olarak ayarlanabilir yeni filtreler tasarlamaları için literatürde önemli bir referans olacaktır.

Anahtar Kelimeler:*Gerilim Farkı Akım Taşıyıcı (VDCC), Yüzen Geçit MOS (FGMOS) Transistor, Voltaj Modlu Band-Geçiren Filtre.*

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1. Introduction

Voltage differencing current conveyors (VDCC) are a versatile active building block used in analog signal processing circuit applications. A very substantial advantage of using VDCCs in analog circuit design is that it is able electronic tunability. FGMOS is a device where the second gate, called a floating gate, is electrically isolated and capacitively connected to the input gates[1-9]. In this work presents a comparison and performance analysis of CMOS-based VDCC (Voltage Differencing Current Conveyor) circuits and differential amplifiers FGMOS-based circuitsThe design of the differential amplifiers in the input stage of the VDCC circuit using FGMOS in the place of CMOS has substantially increased the linearity range of the circuit. THD value of the CMOS based VDCC filter circuit is found to be 15.99% and the THD value of the proposed differential amplifiers FGMOS based VDCC circuit is found to be 1.03%. Theoretical analysis results confirm the simulation results. The presented CMOS and FGMOS-based band-pass filters are simulated using TSMC CMOS 0.18 μm technology with VDD, a power supply voltage equal to 0.9 V.

The use of FGMOS transistors instead of the conventional CMOS structure for the differential amplifiers in the input stage provides significant advantages. A control voltage at one of the inputs of the multi-input FGMOS provides a wide range of tunability to the circuit. Circuit designs with FGMOS allow controllability of the threshold voltage (Vth). Due to the properties of FGMOS, the linearity range increases and simplifies the input stage that provides the arithmetic calculations of the circuit. This specialty allows operation at power supply voltage levels lower than the intended operating limit.

In addition to all these features, the FGMOS VDCC consumes fewer power than required in a circuit designed with conventional MOSFET. Literature researches show that a great number of the analog circuits using VDCC as an active element have been found, for instance, capacitance multiplier [12-13], inductance simulator [10-11], versatile passive element simulator [14- 15], triangular and square wave generator [16], sinusoidal oscillator [6, 13, 17-20], first order allpass filter [21], ladder filter [22] etc. But differential amplifiers FGMOS-based VDCC has not been found before in the literature. The versatility of the proposed differential amplifiers FGMOS-based is demonstrated on a filter circuit example. The proposed filter in the reference [23], The three-inputs single-output (TISO) consists of 2 capacitances and 1 resistor. In this study, only band pass filter application is made to show that FGMOS increases linearity in a filter application.The unique aspect of this study is that there was no differential amplifiers FGMOS-based VDCC circuit design in the previous studies. The rest of the paper is organised as follows: Section 2 describes proposed circuit. Brief introduction of FGMOS and differential amplifier FGMOS based VDCC circuit is given in section 3. Simulation results are discussed in section 4. Finally, conclusions are present in section 5.

2. Proposed Circuit

The circuit symbol of the proposed in recent years active element, VDCC, is shown in Figure 1, where P and N are input terminals and Z, X, W_P and W_N are output terminals. Except the X terminal all of the terminals exhibit high impedance.

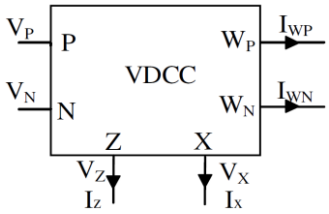

Fig. 1. *Circuit symbol of the VDCC.*

$$\begin{bmatrix} I_p \\ I_N \\ I_Z \\ V_Z \\ I_{W_p} \\ I_{W_N} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ \alpha g_m & -\alpha g_m & 0 & 0 \\ 0 & 0 & \beta & 0 \\ 0 & 0 & 0 & \gamma_{W_p} \\ 0 & 0 & 0 & -\gamma_{W_N} \end{bmatrix} \begin{bmatrix} V_p \\ V_N \\ V_X \\ I_X \end{bmatrix} \quad (1)$$

In equation 1, α, β and γ are the non-ideal voltage and current gains of the VDCC and ideally equal to one. gm is transconductance gain of the VDCC and is defined as:

$$g_m = \sqrt{I_{B1}\ \mu_n\ C_{ox}\ \frac{W}{L}} \quad (2)$$

In Equation (2), μ_n is the carrier mobility for NMOS transistors, C_{ox} is the gate oxide capacitance per-unit area, W is the effective channel width, L is the effective channel length, and I_{B1} is the bias current to control, and is used to control the gm.

The filter topology in Figure 2 is created using only the VDCC active element. It can be used as the three-input single-output (TISO) voltage mode filter in Figure 3 [23]. The circuit analysis gives the following for the output voltage, which can be expressed in Equation (3).

$$V_{OUT} = \frac{V_2\, s^2 C_1\, C_2 + V_1\, s\, C_2\, g_m + V_3\, g_m\, G}{s^2\, C_1\, C_2 + s C_2\, g_m + g_m\, G} \quad (3)$$

$$\begin{aligned} &(i)\ LP: V_1 = V_2 = 0, V_3 = V_{IN} \\ &(ii)\ BP: V_2 = V_3 = 0, V_1 = V_{IN} \\ &(iii)\ HP: V_1 = V_3 = 0, V_2 = V_{IN} \\ &(iv)\ BS: V_1 = 0, V_2 = V_3 = V_{IN} \\ &(v)\ AP: V_2 = V_3 = -V_1 = V_{IN} \end{aligned} \quad (4)$$

The circuit of quality factor (Q) and pole frequency (w_0) can be given as follows:

$$Q = \sqrt{\frac{G\, C_1}{g_m\, C_2}} \quad (5)$$

$$w_0 = \sqrt{\frac{g_m\, G}{C_1\, C_2}} \quad (6)$$

Figure 2 shows CMOS implementation of the VDCC. Figure 3 shows TISO biquad filter. The terminals of the TISO biquad

filter in Figure 3 are shown in Figure 1 and Figure 2. Three-inputs single-output (TISO) filter which can make real all five types of biquadratic functions in voltage mode that is low-pass, high-pass, band-pass, band-stop, and all-pass filter with single VDCC. In this work, only the band-pass filter application is included to show the accuracy of the proposed circuit. For the TISO filter, pole frequency can be tuned electronically with changing bias current. In addition, VDCC-based biquad filter circuit with a minimum number of grounded passive elements have been studied in the present paper. A voltage mode biquad filter which involves a single VDCC and a few passive elements has been presented. Therefore, this filter circuit is used for the application. The design of the differential amplifiers at the input stage of the VDCC active element of the TISO filter circuit using FGMOS has increased the linearity significantly, as can be seen in Figure 5. The performances of the VDCC-based TISO filter are illustrated by SPICE simulations. The theoretical analysis of the filter agreed well with the SPICE simulations. Table 1 shows the aspect ratios of the transistors for the VDCC in Figure 2.

In this study, the two differential amplifiers in the input stage of the VDCC circuit are designed using FGMOS instead of CMOS. The design of the differential amplifiers in the input stages of the VDCC circuit topology using FGMOS instead of CMOS provides a significant increase in linearity and voltage following properties by amplifying the input signal of the circuit.

In this section, floating gate MOSFET (FGMOS) and differential amplifier FGMOS-based VDCC circuits have been briefly introduced with their schematic representation. This section also explains the implementation of FGMOS and differential amplifier FGMOS-based VDCC circuit into the final design.

3. FGMOS and Differential amplifier FGMOS-based VDCC circuit

In this section, floating gate MOSFET (FGMOS) and differential amplifier FGMOS-based VDCC circuits have been briefly introduced with their schematic representation. This section also explains the implementation of FGMOS and differential amplifier FGMOS-based VDCC circuit into the final design.

3.1. Floating Gate MOSFET (FGMOS)

Floating Gate MOS transistors are widely used in analog and digital world as EPROM, EEPROM, flash memories, and neuronal computational element in neural network. Especially FGMOS used in low-voltage, low-power analog design and analog storage elements is gaining popularity day by day. A typical multi input floating gate transistor is shown in Figure 4. It is a conventional MOSFET in which the gate is capacitively coupled to the input using another poly-silicon layer. The equation that models the behaviour of floating gate voltage (VFG) of FGMOS is given by equation (7).

$$V_{FG}\text{-}\Sigma_{i=1}^{N}\frac{C_i}{C_T}V_{i+}\frac{C_{gs}}{C_T}V_{S+}\frac{C_{gd}}{C_T}V_{D+}\frac{Q_{FG}}{C_T} \quad (7)$$

Where C_T-C_{GS}+C_{GD}+$\Sigma_{i=1}^{N}C_i$ and Q_{FG} explain the amount of charges that is being trapped in FG during fabrication. FGMOS provides impressive features with low-voltage, low-power context. In application of linear and nonlinear functions provides flexibility to designers. Also, since FGMOS is multi-input, it allows adding extra inputs according to the needs of the designer. In this way, tunability feature is earned to the circuit.

4. Simulation Results

Finally, a CMOS realization of a VDCC circuit is shown in Figure 3. The supply voltages and biasing currents are given by V_{DD} = −V_{SS} = 0.9 V, I_{B1} = 50 µA, and I_{B2} = 100 µA, respectively. The aspect ratios of the transistors are given in Table 1. The MOS transistors are simulated using TSMC CMOS 0.18 µm process model parameters. In the CMOS and FGMOS based designs of the voltage mode filter shown in Figure 3, R_1 = 2 kΩ and C_1 = C_2 = 50 pF. A typical multi input floating gate transistor is shown in Figure 4.

Figure 5 shows the linearity comparison of VDCC circuit topologies. The design of the differential amplifiers in the input stages of the VDCC circuit using FGMOS instead of CMOS provided a significant increase in the linearity and voltage following properties of the circuit.

Figure 6 shows the I_X-I_Z DC characteristics of CMOS based VDCC and differential amplifiers FGMOS-based VDCC circuits. Differential amplifiers FGMOS-based VDCC circuit's I_X-I_Z DC characteristic graph produced a more symmetrical result for the -100µA to 100µA range compared to the CMOS-based VDCC circuit.

Figure 7 shows the I_{wn}/I_x and I_{wp}/I_x DC characteristics of CMOS-based VDCC and differential amplifiers FGMOS-based VDCC circuits. Differential amplifiers FGMOS-based VDCC circuit's Iwn/Ix and Iwp/Ix DC characteristic graphs produced more symmetrical results for -100µA to 100µA range compared to CMOS-based VDCC circuit.

Figure 8 shows the I_X/I_Z magnitude AC characteristics of CMOS and differential amplifier FGMOS-based VDCC circuits. The fact that the I_X/I_Z ratio is equal to 1 in the differential amplifier FGMOS-based VDCC circuit shows that the current at the X terminal is transferred to the Z terminal exactly.

Figure 9 shows the I_{WN}/I_X, I_{WP}/I_X magnitude AC characteristics of CMOS and differential amplifiers FGMOS-based VDCC circuits. The fact that the I_{WN}/I_X, I_{WP}/I_X ratios are equal to 1 in the differential amplifiers FGMOS-based VDCC circuit shows that the current at the I_{WN} and I_{WP} terminals are transferred to the X terminal exactly.

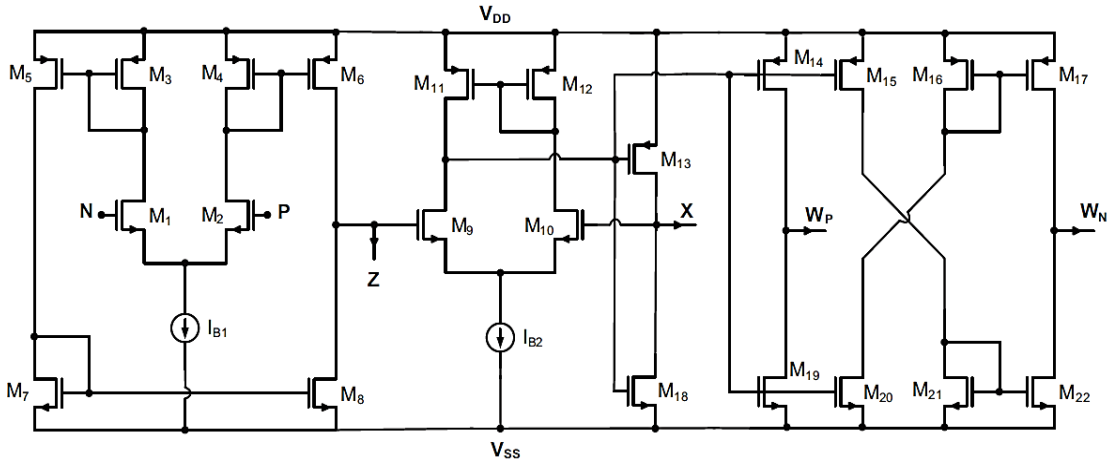

***Fig. 2**. CMOS implementation of the VDCC [23].*

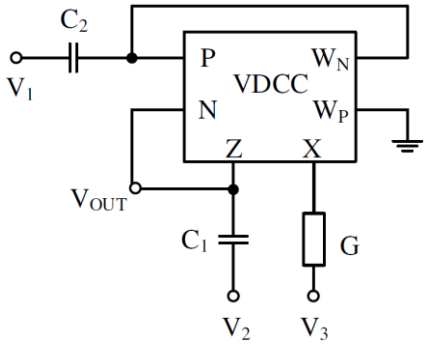

***Fig. 3**. TISO biquad filter [24].*

Table 1 Transistors aspect ratios for the VDCC of Figure. 2.

Transistors	W/L(μm)
M_1-M_4	3.6/1.8
M_5-M_6	7.2/1.8
M_7-M_8	2.4/1.8
M_9-M_{10}	3.06/0.72
M_{11}-M_{12}	9/0.72
M_{13}-M_{17}	14.4/0.72
M_{18}-M_{22}	0.72/0.72

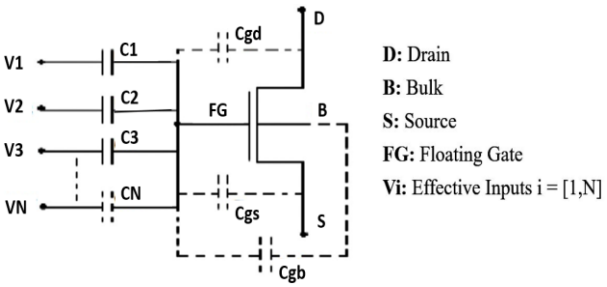

***Fig. 4**. Equivalent schematic of N-input n-channel FGMOS [24].*

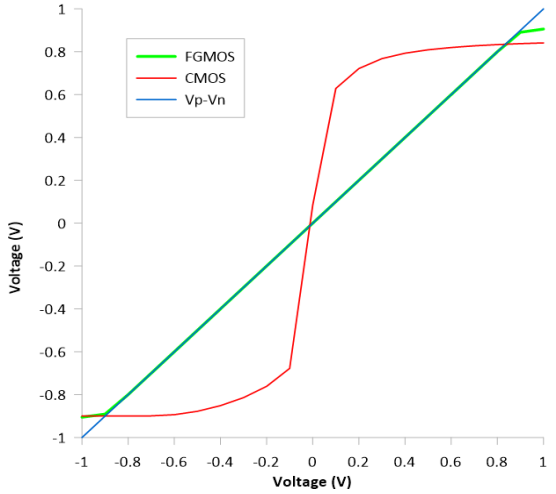

***Fig. 5**.Comparison of linearity VDCC circuit topologies.*

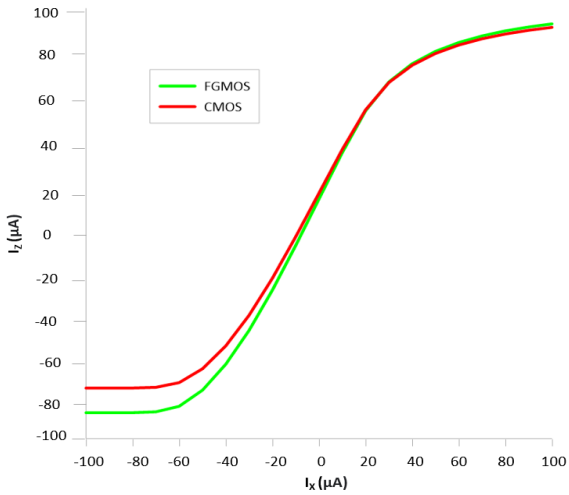

***Fig. 6**. I_X-I_Z DC characteristics of CMOS and differential amplifiers FGMOS-based VDCC circuits.*

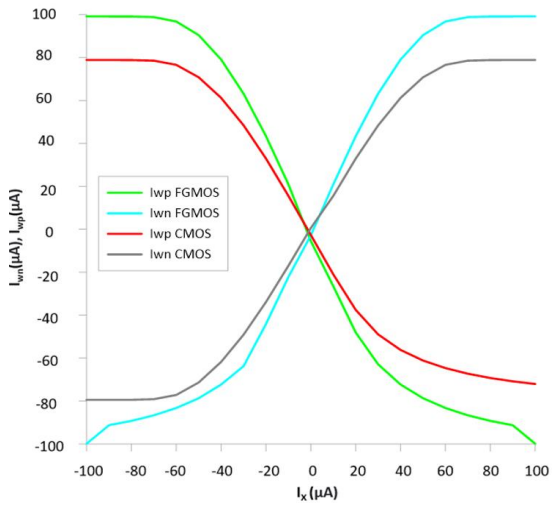

Fig. 7. *I_{wn}/I_x and I_{wp}/I_x DC characteristics of CMOS and differential amplifier FGMOS based VDCC circuits.*

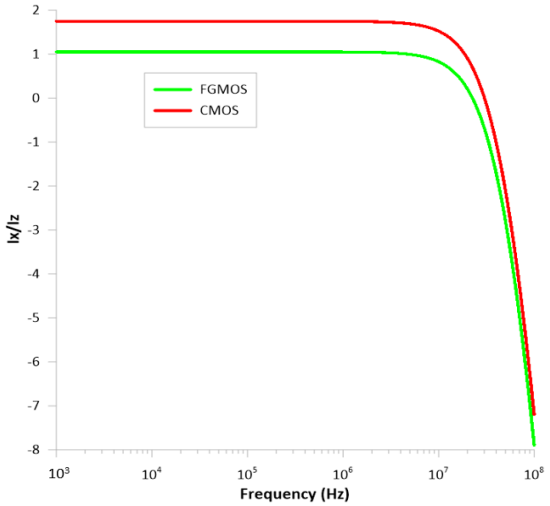

Fig. 8. *CMOS and FGMOS based VDCC AC Characteristics I_{Rx}/I_{RZ} magnitude.*

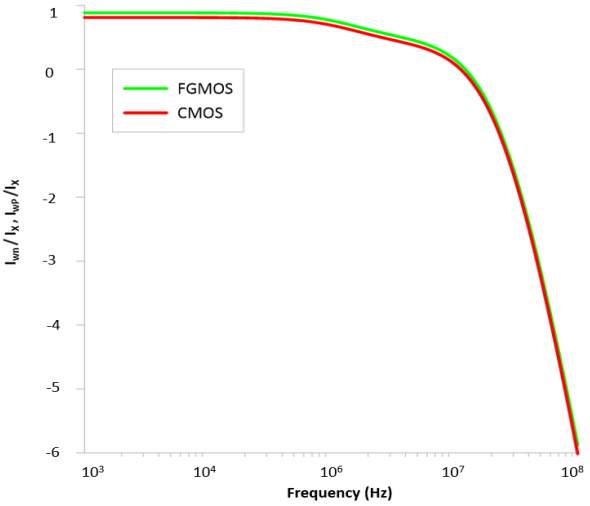

Fig. 9. *CMOS and FGMOS-based VDCC AC Characteristics I_{WN}/I_X, I_{WP}/I_X magnitude.*

Figure 10 shows magnitude of CMOS based VDCC band-pass filter and differential amplifiers FGMOS-based VDCC band-pass filter. The simulation result of the CMOS and FGMOS-based two filter circuits shown in the figure is found to be compatible with the characteristic of the band-pass filter circuit.

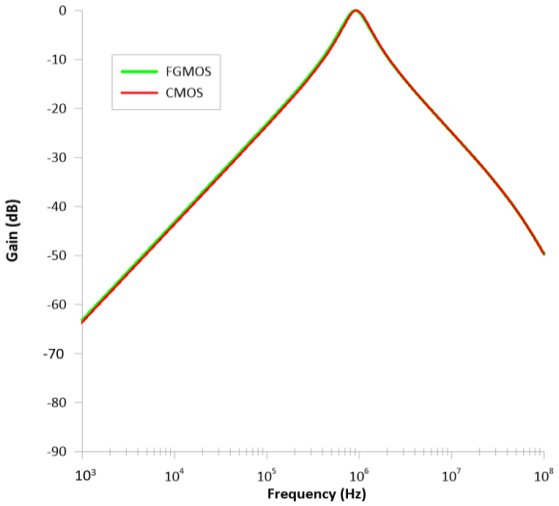

Fig. 10. *Magnitude of CMOS based VDCC band-pass filter and differential amplifiers FGMOS-based VDCC band-pass filter.*

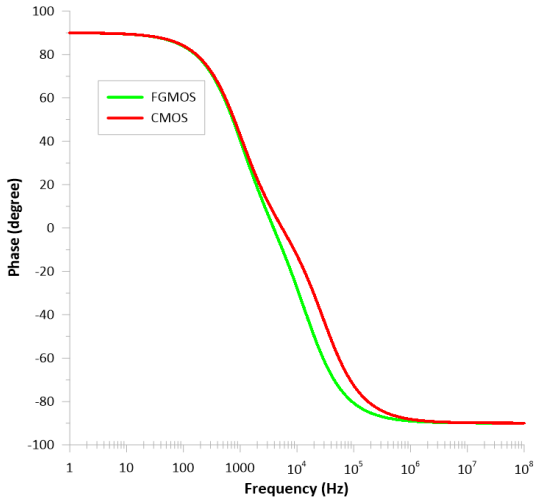

Fig. 11.*Phase of CMOS based VDCC band-pass filter and differential amplifiers FGMOS-based VDCC band-pass filter.*

Figure 11 shows phase of CMOS based VDCC band-pass filter and differential amplifiers FGMOS-based VDCC band-pass filter. The phase of CMOS-based VDCC band-pass filter and differential amplifiers FGMOS-based VDCC band-pass filter circuits is found in accordance with the band-pass filter characteristic and is between -90 degree and 90 degree.

Figure 12 shows the THD analysis of the CMOS based-VDCC and differential amplifier FGMOS-based VDCC band-pass filter. V_P is a pure sine signal applied to the input. V_Z refers to the output of the band-pass filter. The output voltage of the CMOS based-VDCC filter circuit is between +0.7 V and -0.7 V. Differential amplifier FGMOS-based VDCC band-pass filter output voltage is between +0.9 V and -0.9 V. As can be seen from the Figure 12, the output voltage V_P of the proposed circuit is found to be closer to the pure sine voltage.

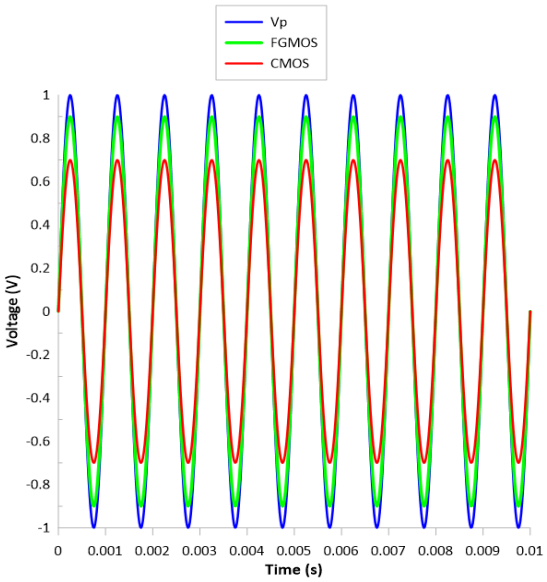

Fig. 12*.THD analysis of CMOS VDCC band-pass filter and differential amplifier FGMOS- based VDCC band-pass filter.*

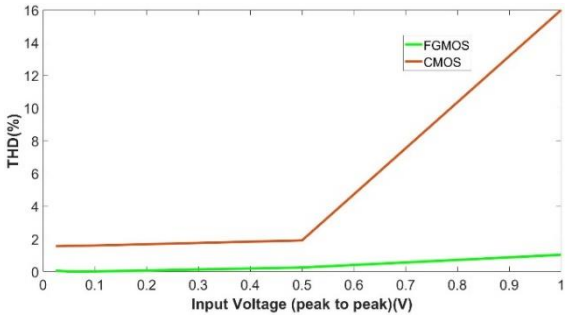

Fig. 13*. THD value of CMOS VDCC BP filter and differential amplifiers FGMOS-based VDCC band-pass filter.*

Figure 13 shows the THD analysis of the CMOS VDCC band-pass filter and differential amplifiers FGMOS-based VDCC band-pass filter. THD indicates the percentage of distortion from the fundamental waveform. THD is used to determine harmonics in voltage and current [25]. Voltage THD is expressed as the ratio of the sum of all voltage harmonic components apart from the fundamental voltage component to the fundamental voltage component [26]. According to the IEEE 519 standard, the maximum acceptable THD value for low-voltage applications is 5%, and also maximum acceptable value for individual voltage harmonics is 3% [27-30].

The THD value of the CMOS VDCC band-pass filter circuit was 15.99%, and the THD value of the differential amplifier FGMOS-based VDCC band-pass filter circuit was found to be 1.03%. The fact that the THD value in the band-pass filter application of the proposed circuit is lower indicates that the linearity is substantially increased.

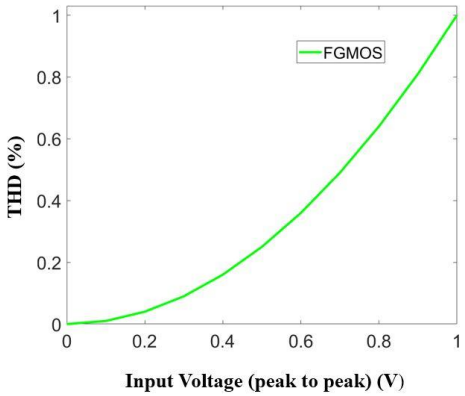

Fig. 14*.THD value of differential amplifiers FGMOS-based VDCC band-pass filter.*

Figure 14 shows the THD analysis of the differential amplifier FGMOS-based VDCC band-pass filter. THD value of the FGMOS-based VDCC band-pass filter circuit was found to be 1.03%.

5. Conclusion

This paper presents a comparison and performance analysis of CMOS-based VCDD (Voltage Differencing Current Conveyor) circuits and differential amplifiers FGMOS-based circuits. The design of the differential amplifiers in the input stage of the VDCC circuit using FGMOS instead of CMOS has significantly increased the linearity range of the VCDD active element. THD value of the CMOS based VCDD filter circuit is found to be 15.99%, and the THD value of the proposed differential amplifier FGMOS-based VDCC circuit is found to be 1.03%. The presented CMOS and FGMOS-based band-pass filters are simulated using TSMC CMOS 0.18 µm technology with a power supply voltage, V_{DD}, equal to 0.9V. As a result, the use of FGMOS transistors at the input stage of the VDCC circuit amplifies the input signal of the circuit, providing a significant increase in linearity and voltage following properties. The proposed FGMOS-based circuit topology will be an important reference in the literature for researchers to design new linearly tunable filters.

Author Contributions

Format analysis – Büşra Hasılcı (BH) - Fırat Kaçar (FK); Simulation Performance - BH, Processing - BH, FK; Literature review – BH, FK; Writing - BH; Review and editing - BH, FK.

Declaration of Competing Interest

The authors declared no conflicts of interest with respect to the research to the research, authorship, and/or publication of this article.

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