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Research Article

Analysis and Compensation of Dead Time Harmonics Based on Time Compensation Strategy in the Single-Phase Full-Bridge Inverters

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***Abstract*—A short period, called dead time, is implemented to prevent power switching devices from shoot-through in voltage-source inverters (*VSI*). While adding dead time is required in the switching signals, it also causes negative effects on inverter operation such as distortion at output voltage due to significant number of harmonic components, and reduction in voltage magnitude of fundamental components. Eventually, the negative effects caused by dead time have to be compensated with compensation schemes. Different modulation schemes, which are called unipolar and bipolar switching, can be implemented in *VSI*, which in return might change the dead time effect. Although analysis of bipolar switching on the dead time effect has been implemented, analysis of unipolar switching is not addressed by most. In this paper, the effect of dead time on unipolar sinusoidal pulse width modulation (*SPWM*) is analyzed, the principle of the proposed compensation strategy is described in detail and the time compensation method with unipolar *SPWM* scheme is implemented using microprocessor-STM32F407G. The technique is intensively simulated and the evaluated through experimental results on resistive and resistive-inductive loads by comparing uncompensated and compensated states. Simulation and experimental results are presented to demonstrate and confirm the validity of the proposed dead-time compensation method.**

***Index Terms*—Dead time compensation method, Dead time effect, Single phase full bridge inverter, Time compensation method, Unipolar switching.**

I. Introduction

INVERTERS have become an indispensable converter for many industrial application areas where they are widely used in the control of various applications such as traction systems, electric vehicles, renewable energy integration with utility grid and several industrial systems. Wide spread use of inverters have increased recently and inverter technologies are developing gradually [1]. In real applications, power semiconductor switches used in power electronics circuits are not ideal, i.e., they have finite turn-on and turn-off times during switching transitions. In order to prevent synchronous conduction of upper and lower switches of the same leg at the same time, certain time delay called dead time [2]- [4] is inserted to the driving signals of these switches on the same leg to allow enough time to turn off one switch before other switch receives turn on signal which ensures safe operation [5]. On the other hand, this blanking time causes problems in the system operation such as distortion of the output voltage and current waveform to contain a large number of harmonic components and reduction in fundamental output voltage and high switching frequency [6], [7]. As the frequency increases, this negative effect increases even more [3], [8] which is called as dead time effect. According to IEEE 519, the total harmonic distortion of the output voltage should not be more than %5. In off-grid systems, an *LC* filter is used to suppress harmonics and THD values of the output voltage and current remains below the level determined by the standards. However, it is difficult to suppress the output voltage distortion caused by dead time with these output filters because of increase in filter size and cost. Therefore, dead time compensation method become important to reduce these negative effects on voltage source inverter. Dead time compensation methods are classified as shown in Figure 1 where they can be divided into three parts such as time compensation method, average voltage compensation method and repetitive control method, respectively.

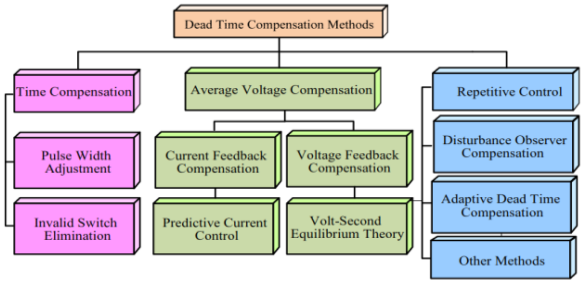

Fig. 1: Dead time compensation methods [3].

While one such category of the methods is based on the averaging voltage theory, other method is based on determination of output current polarity. The time compensation approach which is also known as pulse width adjustment method is the most extensively utilized method due to faster and more accurate results. In order to compensate for the effect of dead time, the turn-on or turn-off time of the power devices are altered by changing pulse-width as increasing or decreasing according to direction of output current and voltage in one period [3], [6]. In this method, pulse width can be increased or decreased following the detection of output current direction which is shown in Figure 2.

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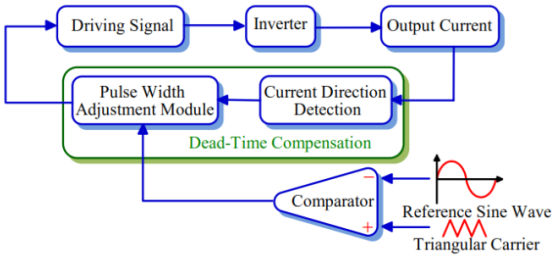


Fig. 2: The schematic diagram of pulse width adjustment method [3].

When the advantages of this method are examined, the output voltage is compensated about zero error and this method depends on direction of output current and voltage which results in simple structure. However, any uncertainty in the zero-crossings of the current adversely affects the compensation. Since the direction of the current is also decisive in the compensation, this is one of negative features of pulse width adjustment method and it strains the memory of the microcontrollers for operating in every period requiring significant amount of computational resources [3]. Several studies regarding dead time compensation method have been presented in the literature. The method proposed by authors [4] demonstrates novel distorted voltage compensation method to eliminate the effect of dead time on zero-current clamping phenomenon. The novel compensate strategy is represented for six-switch three-phase output inverter in [9] by using the direction of the current in each phase and error voltage occurred due to dead time is compensated by increasing or decreasing of the switching conduction period. The protection algorithm, which ensures two switches are not conducted at the same time, is applied on circuit by the author [10] and the dead time is defined within algorithm from the beginning. In literature [11], the fifth and seventh current harmonics are generated in the stationary reference frame because of dead time and sixth current harmonics are generated in the D-Q reference frame. The distortion of output waveforms caused by dead time is compensated by using a proportional integral (PI) current regulator in synchronous frame. In literature [12], a modified pulse width modulation method is proposed to reduce common-mode voltage in case of effect of dead time. In addition, the direct pulse compensation of the dead time is proposed by authors [13]. The aim of this study is to reduce dead time-imposed voltage distortion by superimposing a square wave on the triangle wave. The frequency of the triangle carrier and the square wave is the same and the amplitude of the square wave equals the dead time. In literature [14], the effect of dead time on a three-level neutral-point clamp (NPC) voltage source converter is examined in detail. The self-balancing space vector pulse-width modulation (SVPWM) is applied for improving the effect of dead time and it provides cost effective. In terms of continuous and discontinuous pulse-width modulation, the effect of dead time is discussed in [15] which includes minimum and maximum pulse width effects. In literature [16], novel dead-time space vector pulse-width modulation technique is presented for controlling voltage source inverter. In this study, the proposed algorithm has been altered to ensure that the duty cycle is independent of carrier frequency and sampling time. In terms of optimum dead time, the method proposed by the authors [17] predict optimum dead time based on load current and eliminate body-diode conduction. In [18], the proposed compensation method using the controller output has been presented and in [19], adaptive dead time compensator is carried out by calculating the feed-forward compensation duty cycle. In order to fully mitigate low order harmonics caused by dead time effect, multiple resonant controllers and repetitive controllers is used by authors [20] - [23]. In [24], the dead time compensation algorithm has been suggested by using filter. However, the bandwidth of the current controller can be limited due to low pass filter (*LPC*). In [25] - [27], a more complex mathematical model of *VSI* is carried out, considering the effect of parasitic capacitance on output voltage and the compensation formula is derived according to parasitic capacitance. Generally, the studies mentioned above are carried out by using bipolar *SPWM* which is easier to analyze and a direct time compensation method can be applied. However, unipolar *SPWM* has advantages compared to bipolar *PWM* technique, such as obtaining lower *THD* values, helping the selection of semiconductor switches with lower nominal value depending on the *dv/dt* value in real applications, and harmonic frequencies present at two times the switching frequency at load [28], [29]. Despite all the advantages, analysis of the effect of dead time on unipolar *SPWM* could hardly be found in literature. In this paper, analysis of the effect of dead time on unipolar *SPWM* is carried out and time compensation method is applied on unipolar *SPWM* single phase full bridge inverter. The experimental and simulation results for compensated and uncompensated states are obtained at resistive *(R)* and resistive-inductive *(RL)* loads in fixed dead time and the results are compared according to *THD* values. The analysis of the effect of dead time on unipolar *SPWM* and the usefulness of applying the compensation method to the circuit at *R* and *RL* loads are confirmed by simulation and experimental results.

II. Analysis of Dead Time Effect on Voltage Source Inverter

A. Model of Single-Phase Full Bridge Inverter

A single-phase full bridge inverter is shown in Figure 3 where V_{DC} is the DC input voltage, C_{input} is input capacitor, *S1-S4* are power switches with four freewheeling diodes connected in reverse and parallel to the power switches, L_f is filter inductor, C_f is filter capacitor and load.

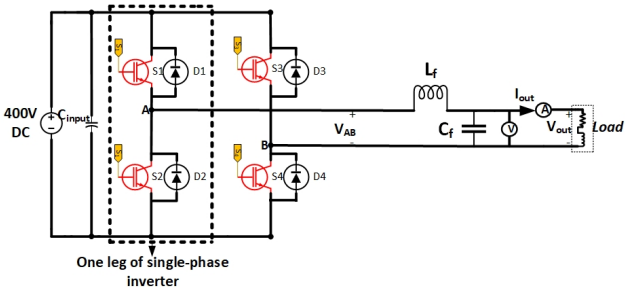


Fig. 3: The circuit model of single-phase full bridge inverter.

B. Dead time effect

When *S1* and *S2* power switches are ideal, these switches can be altered simultaneously from on to off at the same time. However, power switches used in voltage source converter (Mosfet, IGBT etc.) do not have ideal characteristic. In practice, it is seen that *S1* and *S2* power switches have turn-on and turn-off time delays. For this reason, turn-on of the power switch is delayed by a few second or vice versa in order to avoid the simultaneous conduction of the power devices in the same phase leg. This case indicates the necessity of dead time in H bridge-type *PWM* voltage source converters in order to ensure safe operation. In addition, dead time is also known as blanking time and normally a few microseconds [6]. The representation of dead time on gate signals is shown in Figure 4.

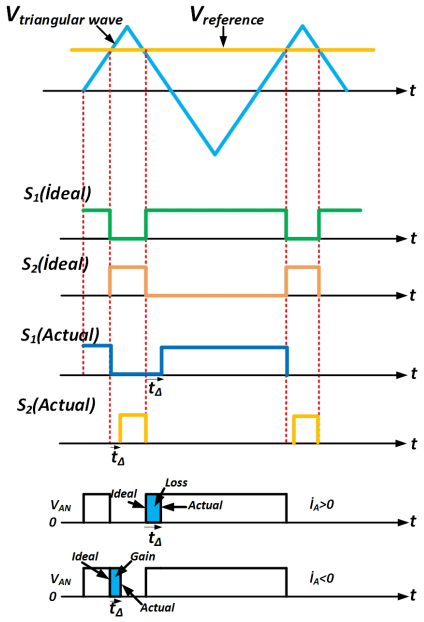


Fig. 4: The representation of dead time on gate signals.

PWM (Pulse-Width Modulation) is generated within microcontroller using a counter instead of triangular waveform which is known as carrier signal. It is more convenient to use the triangular waveform in Figure 4 to better illustrate the effect of dead time. In Figure 4, the voltage waveforms of one leg of single-phase inverter V_{AN} show in more detail for the state of *S1* and *S2* switches. During the dead time, both switching elements stop to conduct, the output current flows through the anti-parallel diodes which are determined as D_1 and D_2 due to the continuous current. As mentioned in Figure 4, anti-parallel diodes are turned on depending on the direction of the current. If output current is positive ($I_A > 0$), diode(D_2) is turned on and the output terminal will show a negative voltage. If output current is negative ($I_A < 0$), diode (D_1) is turned on and the output terminal will show a positive voltage. It can be seen that the conduction time of the output voltage waveform decreases when the output current is greater than zero compared to ideal waveform. In case of $I_A < 0$, this case opposite of $I_A > 0$. That is, the conduction time of the output voltage waveform increases when the output current is less than zero compared to ideal waveform.

C. Dead time effect of unipolar SPWM

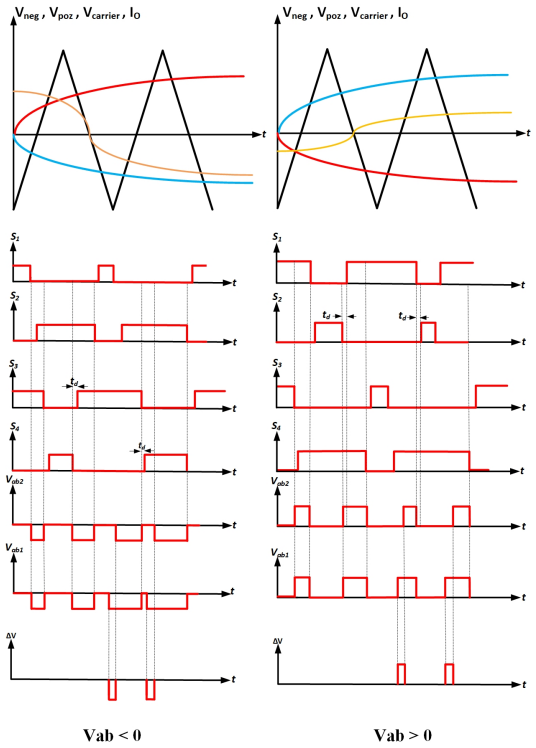
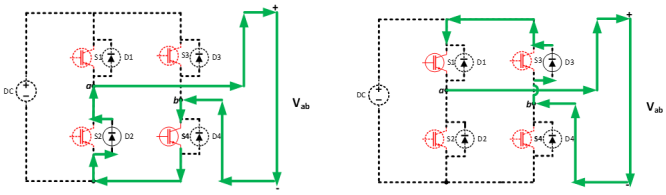


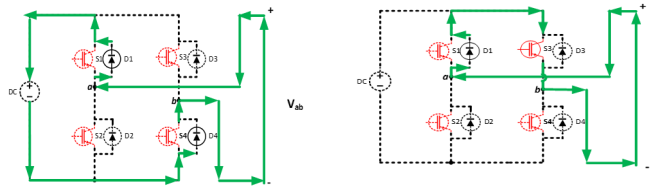
Fig. 5: Dead time effect with different voltage and current polarity.

As mentioned above, dead time effect analysis of unipolar *SPWM* is different than bipolar *SPWM*. Figure 5 shows dead time effect of unipolar *SPWM*. To analysis dead time effect, it necessary to ideal, actual gating waveform with dead time and output voltage in both cases. While load is ohmic-inductive, gate signals and output voltage waveforms are given in Figure 5. The above-mentioned graphs are drawn from the starting points of the T/2 and periods to a certain point. When these graphs are analyzed, it will be possible to find out how the variation of the output voltage between the ideal state and the actual state for a period due to dead time effect. In addition, variation of output voltage is known as error voltage. When analyzing Figure 5, it is sufficient to examine four situations depending on output voltage and output current for one fundamental period. Thus, these situations are $V_{ab} > 0, I > 0$; $V_{ab} > 0, I < 0$; $V_{ab} < 0, I > 0$; $V_{ab} < 0, I < 0$, respectively [16]. In case of $V_{ab} > 0, I > 0$, this situation can be explained in two steps. S_1 is turned off while S_4 is turned on, the output current flows through S_4 and D_2. Thus, actual output voltage V_{ab2} is zero during dead time t_d. S_4 is turned off while S_1 is turned on, the output current flows through S_1 and D_3. Thus, actual output voltage V_{ab2} is zero during dead time t_d. When the actual voltage V_{ab2} is compared with ideal voltage, it is seen that the actual voltage diminishes two pulses with dead time t_d and magnitude of V_{DC}. In case of $V_{ab} > 0, I < 0$, S_1 is turned off while S_4 is turned on or S_1 is turned on while S_4 is turned off, the output current flows through D_4 and D_1. Thus, actual output voltage V_{ab2} is V_{DC} during dead time t_d. When the actual voltage V_{ab2} is compared with ideal voltage, it is seen that the actual voltage no diminishes with dead time t_d

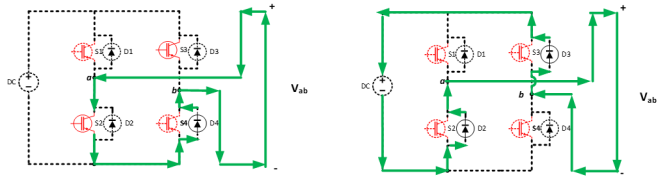
and magnitude of V_{DC}. In case of $V_{ab} < 0, I > 0$, S_2 is turned off while S_3 is turned on or S_2 is turned on while S_3 is turned off, the output current flows through D_3 and D_2. Thus, actual output voltage V_{ab2} is $-V_{DC}$ during dead time t_d. When the actual voltage V_{ab2} is compared with ideal voltage, it is seen that the actual voltage no diminishes with dead time t_d and magnitude of V_{DC}. That is, the output voltage is unaffected by the dead time. In case of $V_{ab} < 0, I < 0$, this situation can be explained in two steps. S_2 is turned off while S_3 is turned on, the output current flows through S_3 and D_1. Thus, actual output voltage V_{ab2} is zero during dead time t_d. S_3 is turned off while S_2 is turned on, the output current flows through S_2 and D_4. Thus, actual output voltage V_{ab2} is zero during dead time t_d. When the actual voltage V_{ab2} is compared with ideal voltage, it is seen that the actual voltage diminishes two pulses with dead time t_d and magnitude of $-V_{DC}$. In the light of this information, inductor current direction is shown in Figure 6 as six diagrams.



(a) $V_{ab} > 0, I > 0$ (S_4, D_2) (b) $V_{ab} > 0, I > 0$ (S_1, D_3)



(c) $V_{ab} > 0, I < 0$ (D_1, D_4) (d) $V_{ab} < 0, I < 0$ (S_3, D_1)



(e) $V_{ab} < 0, I < 0$ (S_2, D_4) (f) $V_{ab} < 0, I > 0$ (D_2, D_3)

Fig. 6: Conducting devices based on polarity of output voltage and output current.

Considering the above analysis, the following assumptions need to be made to formulate the effect of dead time quantitatively [30]. First of all, the carrier frequency of the circuit must be sufficiently greater than the fundamental frequency. Secondly, the inverter output current is virtually sinusoidal, and voltage variation occurs almost equidistantly. Lastly, switching components should have a minimal reverse storage time which is negligible. According to the analysis and assumptions above, the error voltage is calculated based on the ideal voltage and the actual voltage with dead time as follows:

$$\Delta V = \Delta V_1 - \Delta V_2 = +2 f_c t_d V_{DC} \qquad I_{\text{out}} > 0, V_{ab} > 0 \quad (1)$$

$$\Delta V = \Delta V_1 - \Delta V_2 = -2 f_c t_d V_{DC} \qquad I_{\text{out}} < 0, V_{ab} < 0 \quad (2)$$

where V_{DC} is the DC input voltage, f_c is the switching frequency, and t_d is the dead time.

III. Simulation Results

The simulation of a full-bridge single-phase inverter circuit is carried out in uncompensated state and compensated state for *RL* and *R* load at a certain dead time period. Sinusoidal Pulse Width Modulation technique is used to control the a full-bridge single-phase inverter circuit. This circuits are simulated in Power Simulation (PSIM) software. Waveforms of the output voltage and output current are obtained and total harmonic distortion values are calculated for both cases. The results obtained for compensated and uncompensated state are compared and evaluated.

A. Power stage and control structure of circuit

In the first step, the full bridge single-phase inverter circuit is modeled at resistive load for uncompensated state and compensated state. The simulations of the power circuit are performed using PSIM. In addition, the open loop operation of the circuit is examined by generating switching signals with *SPWM* method. In this simulation, DC input voltage and low pass filter values are 400V, 3.60mH, 15μF, respectively. *LC* filter values are calculated depending on the amount of fluctuation of inductance current, switching frequency and DC bus voltage. The power and control circuit of single-phase full bridge inverter with resistive load are shown in Figure 7.

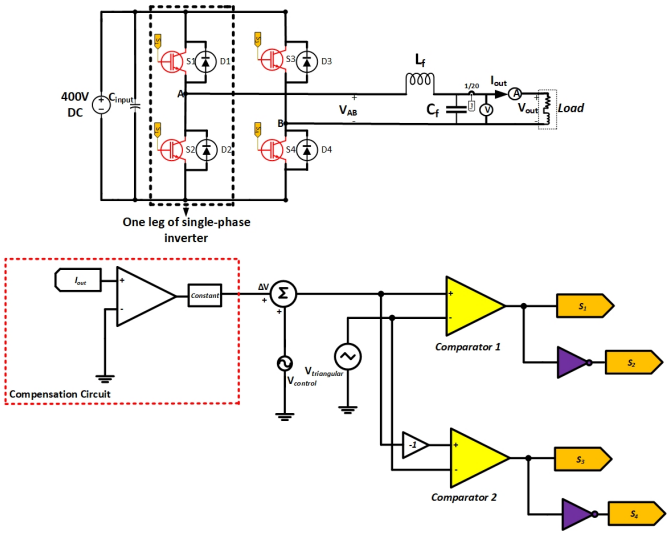


Fig. 7: Power and control circuit of single-phase full bridge inverter.

B. Compensated circuit

As mentioned before, time compensation methods are used to reduce this negative effect. According to this method, if the pulse width is changed at the zero points of the current, the distortion of the output waveforms is reduced. Thus, *THD* values are reduced. That is, the reference signal must

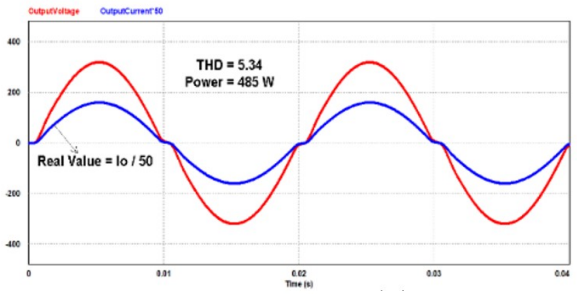
change for the compensation to be applied to the circuit in this simulation. In this simulation, this method is applied by designing the following formula.

$$V_{control,update} = \begin{cases} V_{control} + \Delta V & \text{if } I_{\text{out}} > 0 \\ V_{control} - \Delta V & \text{if } I_{\text{out}} < 0 \end{cases} \quad (3)$$

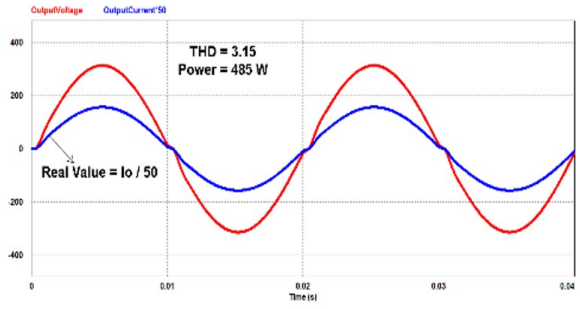
where, $V_{control}$ is the reference signal of the inverter circuit in the uncompensated state and ΔV is the error voltage as seen in formulas (1) and (2). This error voltage should be added to $V_{control}$ to determine the new reference signal. Thus, this signal is updated and *PWM* signals are sent to the respective MOSFETs for compensation according to the polarity of the output current.

C. Uncompensated and compensated state with resistive load

Figure 8 shows the output voltage and output current when the full bridge inverter was connected to a 100Ω resistive load, both in the absence of dead time compensation and in its presence. In the uncompensated state, it can be observed that the output current remains at zero for a longer duration compared to the compensated state due to the effect of the dead time. As a result, the output voltage is more significantly affected at that instant. In light of this information, it is anticipated that there will be an increase in harmonic distortion values (*THD*) in the uncompensated state will be higher than in the compensated state. The simulation results also support this hypothesis. As depicted in Figure 8, the *THD* value of the output voltage decreases by 41.01% at a resistive load in the compensated state. Thus, the adverse effects of the dead time are mitigated to a significant extent using the compensation method.



(a)

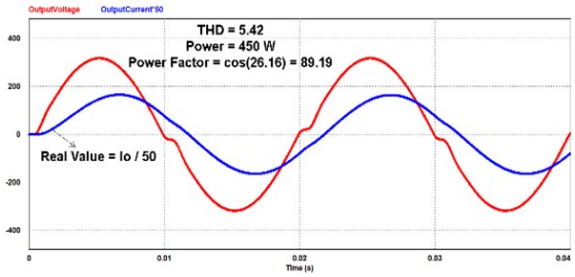


(b)

Fig. 8: Output voltage and output current waveforms with resistive load; (a) Uncompensated state; (b) Compensated state.

D. Uncompensated and compensated state with resistive-inductive load

Figure 9 shows the output voltage and output current when the full bridge inverter was connected to an 85Ω and 143mH resistive-inductive load, both without and with dead time compensation. Comparing Fig. 9(a) with Fig. 9(b), the compensation method provides a significant decline of about 31.54% in the distortion caused by dead time.



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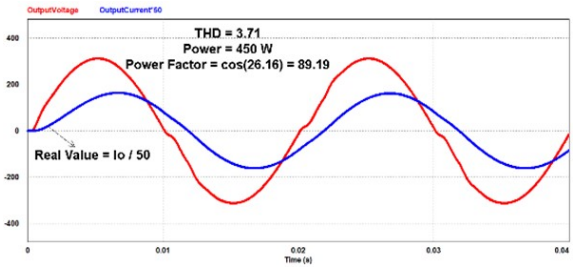


(b)

Fig. 9: Output voltage and output current waveforms with resistive-inductive load;(a) Uncompensated state; (b) Compensated state.

IV. Experimental Results

Experimental tests with the single-phase full bridge inverter were carried out for resistive and resistive-inductive load at compensated and uncompensated state. The operating parameters of the inverter and component list are given in Table 1.

A. General working blocks of designed system

In Figure 10, a comprehensive block diagram illustrates the experimental setup utilized for the inverter testing. This diagram encompasses various crucial components such as the DC input voltage, capacitors, optocouplers, and isolated DC sources. Central to this setup is the microcontroller, which oversees the general functioning and synchronization of the components. Moreover, the inclusion of an isolated current sensor adds to the precision of the system by providing real-time current measurements. The inverter power circuit, an essential part of the structure, ensures the necessary power conversion, while an output low-pass filter has been incorporated to refine the output quality. To offer a more tangible perspective, Figure 11 visually represents the inverter's power circuit as implemented in a controlled laboratory environment.

TABLE I: Keysystem specifications and component list of the inverter circuit.

Parameters	Symbols	Values	Component List	
Input Voltage	V_{in}	$400V$	Mosfet	FGH20N60SFD-600V/20A
Output Voltage	V_{out}	220V_{rms}	Inductors	3.60mH
Input Current	I_{in}	1.4A max	Optocoupler	TLP350
Output Current	I_{out}	0-3A	Output Capacitor	$4\mu F$
Switching Frequency	$f_s = 1/T_s$	20kHz	Input Electrolytic Capacitor	470µF
Dead Time	t_{d}	$1\mu s$ (2% of T_s)	Input Ceramic Capacitor	$2.2\mu F$
Line Frequency	f_{L}	50Hz	Microcontroller	STM32F407G
Filter Inductance	L	3.60mH	Comparator	LM311N
Filter Capacitive	C	$15\mu F$	Current Transducer	LEM HX05- NP

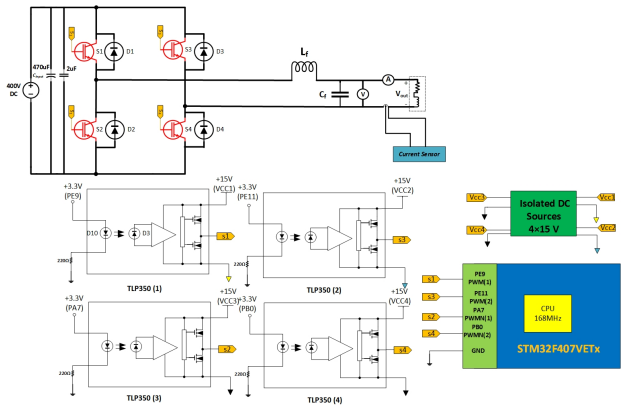


Fig. 10: Block diagram of full bridge single-phase inverter.

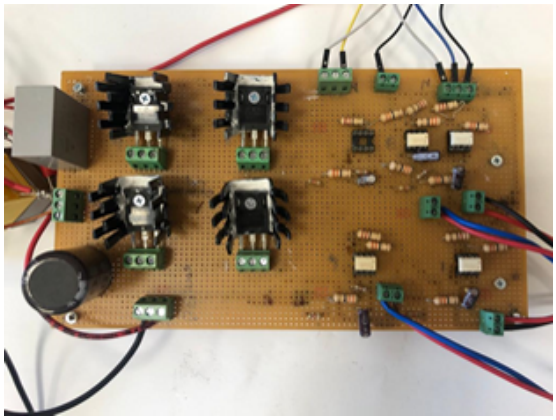


Fig. 11: Full bridge inverter circuit with power circuit.

counter and the sine table values, depending on whether the dead time is compensated or not, where the flow diagram of the *SPWM* algorithm is given in Figure 12.

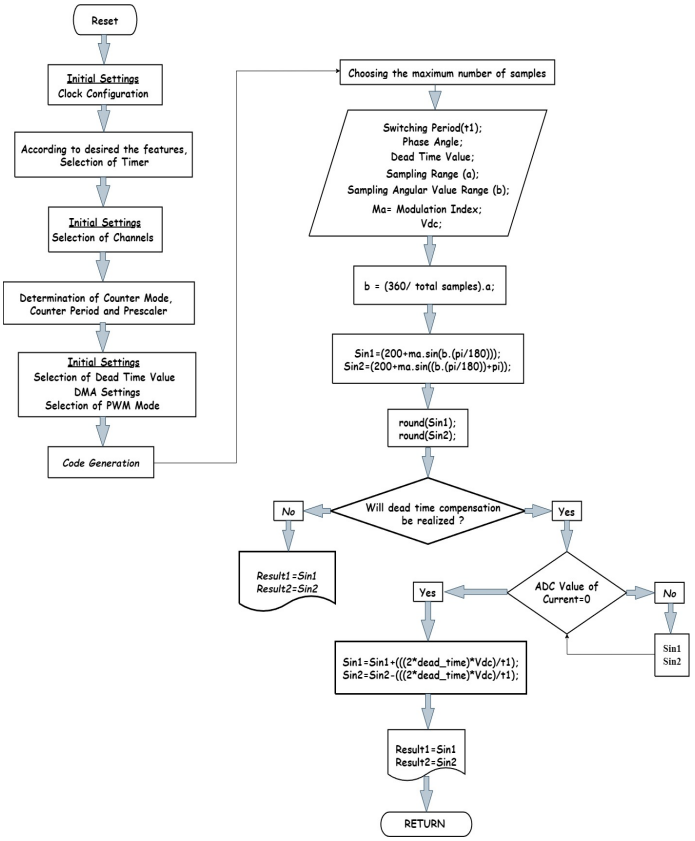


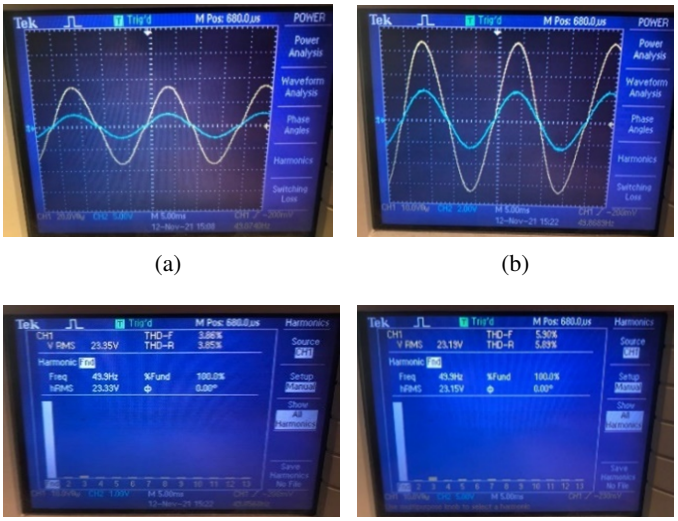
Fig. 12: The Flow Diagram of *SPWM* Generation.

B. Software design

Control signals of mosfet are generated using digital *SPWM* algorithm running on a high-performance microcontroller [31]. Firstly, various adjustments are arranged easily at the beginning such as counter mode, clock configuration and dead time value by using microcontroller development tool as desired. Then, it is created a sine table by writing the relevant codes and used the functions of the timers. The reason is that the microcontroller uses the counter instead of the triangle wave. Finally, necessary signals will be generated by comparing the

C. Uncompensated and compensated state with resistive load

In case of experimental study, Figure 13 shows the output waveforms and *THD* values of the output voltage at uncompensated and compensated states in case of a resistive load. When comparing Figure 13(a) and 13(b), it can be seen that the compensated method decreases the distortion caused by dead time by about 34.46%. In addition, the relation between the output voltage and *THD* values for the resistive load in the uncompensated and compensated states is shown in Figure 14.



(a) (b)

(c) (d)

Fig. 13: Output voltage and output current waveforms with resistive load; (a) Compensated state; (b) Uncompensated state; (c) THD value in compensated state; (d) THD value in uncompensated state.

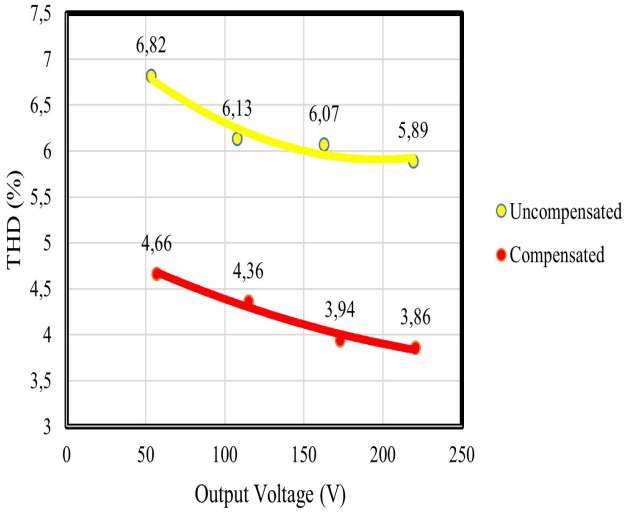
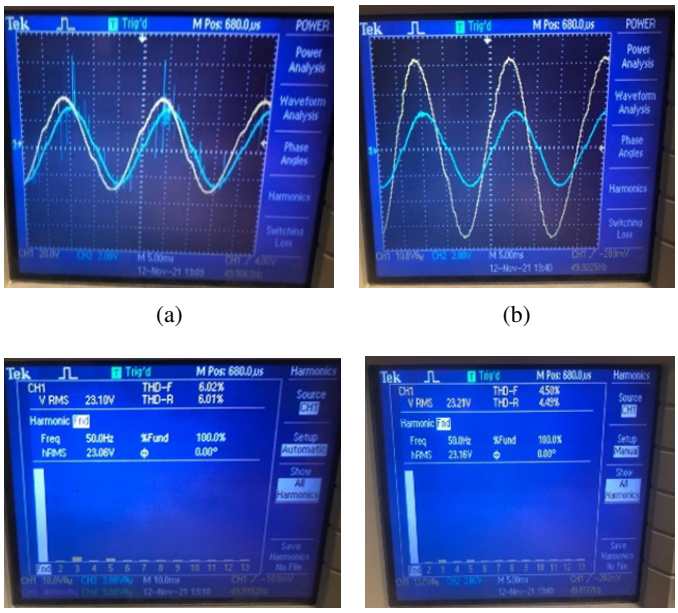


Fig. 14: Relation between THD and output voltage in resistive load.

D. Uncompensated and compensated state with resistive-inductive load

Figure 15 provides a clear representation of the output waveforms, offering a detailed view of the differences in total harmonic distortion (*THD*) measurements between the compensated and uncompensated states when subjected to a resistive-inductive load. Upon closely observing Figure 15, it becomes evident that there's a significant reduction in the *THD* value associated with the output voltage in the compensated state. Specifically, the reduction is around 25.24% when compared with its uncompensated counterpart. This observation underscores the effectiveness and potential benefits of the method we've employed. Furthermore, if we direct our attention to Figure 16, it presents an intriguing overview of the relationship dynamics between the output voltage and *THD* values. This relationship becomes even more apparent when assessing an resistive-inductive load across both states, offering a comparative perspective between the uncompensated and compensated scenarios.



(a) (b)

(c) (d)

Fig. 15: Output voltage and output current waveforms with resistive-inductive load; (a) Uncompensated state; (b) Compensated state; (c) THD value in compensated state; (d) THD value in uncompensated state.

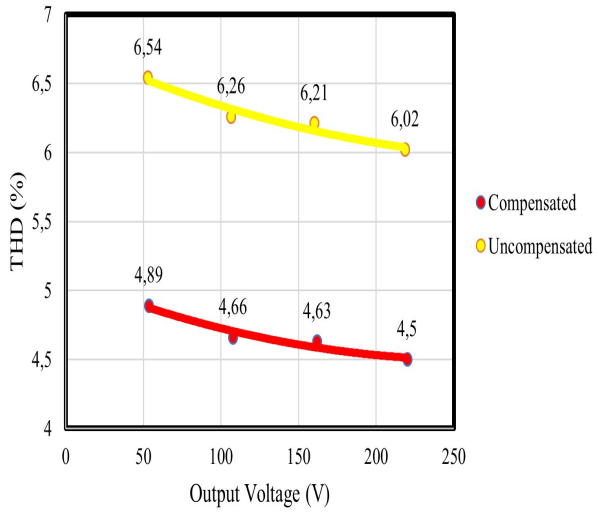


Fig. 16: Relation between THD and output voltage in resistive-inductive load.

Under the given conditions where the DC input voltage is set at 400 V, Table 2 provides a comprehensive overview of the results from experimental evaluations. These results give insights into the performance differences between the uncompensated and compensated states across varying load conditions, specifically focusing on resistive and resistive-inductive loads.

TABLE II: Experimental measurement results for 2% (1 μs) dead time.

State	Uncompensated State		Compensated State	
Load	Resistive	Resistive-inductive	Resistive	Resistive-inductive
Input Current (A)	1.235	1.18	1.313	1.178
Output Voltage (V)	219.2	218.5	220.7	220
Output Current (A)	2.164	2.31	2.176	2.304
$THD_V(\%)$	5.89	6.02	3.86	4.50

V. Conclusion

In this paper, the dead time effect of unipolar sinusoidal pulse width modulation for full bridge single-phase inverter is thoroughly analyzed and a method is proposed to compensate dead time in *SPWM* controlled inverter. The variation of output voltage distortion for compensated and uncompensated states is examined and tested for resistive and resistive-inductive load by simulations as well as by experiments. From the results one can observe from the experimental and simulation result that the time compensation method for a dead time of 2% result in a reduction of *THD* value of inverter output voltage. According to simulation results, *THD* value of the output voltage is decreased as 41.01% at R load and 31.54 % at *RL* load. On the other hand, *THD* value of the output voltage is decreased as 34,46% at *R* load and 25,24% at *RL* load in the experimental results. It can be seen from the results that the dead time compensation methods are important part for power converter, which directly affects the output performance, stability and reliability of the control system. Experimental and simulation results demonstrate the usefulness of the compensation method and show that time compensation method has simple control logic and can be realized conveniently and easily. The output voltage of the inverters approaches the sinusoidal wave as the *THD* values decrease and the results confirm to validity of the time compensation method in both simulation and the experimentation.

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