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A Fabrication Method for Memristors with Graphene Top Electrodes and their Characterization

Selin Onay[1,2] Omer R. Caylan[2,4] Goknur Buke[3] Itır Koymen[1,2*]
[1] TOBB University of Economics and Technology, Department of Electrical and Electronics Engineering, Ankara, Türkiye.
[2] Bilkent University, UNAM Institute of Materials Science and Nanotechnology, Ankara, Türkiye.
[3] TOBB University of Economics and Technology, Micro and Nanotechnology Graduate Program, Ankara, Türkiye.
[4] TOBB University of Economics and Technology, Department of Materials Science and Nanotechnology Engineering, Ankara, Türkiye.

ABSTRACT

In recent years, there has been extensive research on the memristor, a non-volatile memory device that demonstrates effective emulation of biological synapses. The implementation of graphene as a top electrode in memristive switching systems presents an intriguing alternative to conventional materials such as Platinum. Graphene, as a carbon-derived material, possesses a remarkable area- to-volume ratio, biocompatibility, adsorption capabilities, and high electrical conductivity and thereby offers a promising avenue for the fabrication of biosensors with superior characteristics. This study reports a novel fabrication method of utilizing graphene as a top electrode in memristive devices. Characterization results of micrometric devices as well as larger memristive devices are also discussed. Larger devices show promising results to be used as memristive sensors. Microstructures have been fabricated successfully through developing a process flow and patterning graphene using photolithography and lift-off. E-beam evaporation and sputtering were used for depositing bottom metal electrodes and active layer respectively. Graphene was produced using the chemical vapor deposition (CVD) method and subsequently transferred using the fishing technique. Ultimately Pt/TiO_2/TiO_x/Graphene memristive devices were fabricated.

Keywords:
Memristor; Graphene; Device fabrication; Graphene patterning; Device characterization

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***Correspondence to**: Itır Köymen,*
E-mail: ikoymen@etu.edu.tr;
Phone: +90 312 292 6900.

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INTRODUCTION

The memristor has been introduced as the fourth basic circuit element in 1971, by Leon Chua. It was noted that there are six different mathematical relations that connect pairs of the four fundamental circuit variables: electric current (i), voltage (v), charge (q), and magnetic flux (Q) (1). One of the relationships mentioned (the charge is the time integral of the current) is derived from the definitions of two of the variables mentioned. Another relationship (the flux is the time integral of the electromotive force, or voltage) is determined by Faraday's law of induction (2). The memristor (a contraction for memory resistor) is an electronic component with two terminals that can change its resistance and was invented based on the principle of symmetry. The memristor links electrical charge and magnetic flux.

With the development of big data analytics (BDA) (3), the internet of things (IoT) (4), and artificial intelligence technology (5), a demand for cutting-edge electronic devices and systems has emerged (6). To function optimally, these systems need to be very power efficient, have a well-designed computer architecture, and be able to process data quickly. There has been significant research interest in memristors and memristive devices over the past decade due to their potential use as non-volatile memory applications (7) and their applications in non-traditional computing (8).

A memristor traditionally consists of a stack of metal, dielectric, and metal layers. The way that a memristor functions relies on the formation and rupture of conductive filament (CF) with defects in the sandwich layer between the two metallic electrodes (9). Once the CF has been formed within a memristor device, the device is able to switch between a high-resistance state (HRS) and a low-resistance state (LRS) in a reversible manner (10). Memristors can be categorized as cation devices, anion devices, and dual ionic devices based on the type of mobile species and migration behavior (11).

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The conduction path in the fabricated devices is made up of a metal that has undergone chemical reduction, resulting in a lower valence state. This conduction path can be viewed as consisting of oxygen vacancies that act as n-type dopants.

Memristive devices are commonly sandwich like structures with two conductive electrodes separated by an active layer. The first reported memristor prototype employed Platinum (Pt) electrodes and a stoichiometric and doped Titanium oxide (TiO_2/TiO_x) active layer (2) this structure remains popular (12). Other examples include gold (Au) electrodes with Zinc Oxide (ZnO) active layer (13), Indium Tin Oxide (ITO) bottom electrodes, Zirconium Oxide (ZrO) active layer and Silver (Ag) top electrodes (14), polyvinylpyrrolidone active layer with Ag electrodes (15), hafnium oxide active layer with Pt electrodes (16). The devices fabricated in this work have an active layer that consists of stoichiometric TiO_2 and doped TiO_x, the bottom electrode is Pt and the top electrode is Graphene.

Graphene has garnered considerable attention due to its exceptional electrical and thermal conductivity, impressive mechanical strength, and remarkable single-atom thickness. These distinctive properties position it as a highly promising material for a diverse array of applications, ranging from flexible electronics and high- performance batteries to ultra-fast transistors and potential advancements in medical devices. The widespread recognition of graphene's potential to revolutionize multiple industries has spurred extensive research and exploration into its capabilities (18). Graphene's high surface-to-volume ratio makes it a particularly attractive material for sensing applications. When it is used as an electrode, all carbon atoms contact the analyte, which results in very high sensitivity. Moreover, no impurities are transferred to the analytes from graphene, electrochemistry of the sensing application thus remains intact. Lastly, graphene is biocompatible (17). All of these characteristics combined with the inherent properties of memristance are promising for developing sensitive, selective, area efficient sensors.

Both graphene and its derivatives, including functionalized graphene, have undergone comprehensive study for their viability as electrode and interface materials in memristive devices. These materials offer significant advantages, such as suitability for device fabrication, exceptional mechanical flexibility, and high optical transparency, all of which can greatly contribute to the advancement and enhancement of memristive technologies. Investigation of prior research reveals a wide spectrum of approaches for patterning graphene, encompassing direct mechanical cleavage, electron beam irradiation, scanning probe lithography, helium ion beam lithography, photocatalytic etching, plasma etching, chemical etching, nanoimprint lithography, and bottom-up growth and synthesis (19). Nevertheless, these methods exhibit certain limitations, such as constraints in scalability, intricate process requirements, high production costs, and potential damage to the graphene's properties and structure during patterning. While each method presents its own set of challenges, the need for a technique that can efficiently pattern graphene without compromising its exceptional characteristics remains a critical goal in advancing its practical applications.

This study aims to explore a convenient, repeatable, and straightforward method for patterning graphene for memristor applications while utilizing the memristor's inherent properties. Larger memristive devices of area 2 cm^2 (hereforth referred to as macro devices) were fabricated to develop fabrication steps and ensure that graphene can be used as a top electrode. The macro devices are fabricated very simply since they do not require any patterning steps. Following successful characterization and sensor measurements, memristors of micrometric dimensions (hereforth referred to as micro devices) were fabricated and electrically characterized. The ultimate objective is to use graphene as a sensitive top electrode for memristive sensors. By acknowledging the constraints of various methodologies, this research focuses on patterning CVD grown and transferred graphene via negative photolithography and lift-off. Furthermore, this paper presents measurement outcomes, encompassing results from current-voltage characterization and the sensing of memristors comprising $Pt/TiO_2/TiO_x$/ Graphene structures.

MATERIAL AND METHODS

Chemical Vapor Deposition (CVD) for Graphene Growth

Initially, copper foils (Alfa Aesar, 13382, 99.8% purity, 25 μm; cut to dimensions of 50 mm × 50 mm) are placed onto a flat quartz boat and positioned within a quartz tube to align with the heating zone. Argon gas (Ar) is flowed through the tube at a rate of 100 sccm for 10 minutes. After purging with Ar, the Ar flow is decreased to 50 sccm and hydrogen gas (H_2) at a flow rate of 50 sccm is introduced into the tube, and heating is commenced. Once the temperature reaches 1000°C, the copper foil is annealed under hydrogen and Ar gas for a duration of 1 hour. Following this 1- hour interval, methane gas (CH_4) at a flow rate of 5 sccm is introduced alongside Ar gas (50 sccm) and hydrogen gas (50 sccm) to facilitate graphene growth over a period of 30 minutes. Post-growth, rapid cooling of the sample is conducted within Ar and hydrogen atmosphere.

Graphene Transfer

A solution of 1 M $FeNO_3$ (200 ml) is poured into a glass petri dish, and the samples are positioned on the liquid's surface. Approximately 30 minutes later, the copper foil is fully etched by the $FeNO_3$ solution. The removal of $FeNO_3$ is executed with care, after which deionized water is introduced into the petri dish, taking precautions to avoid disruption of the graphene layer floating on the liquid. This rinsing process is reiterated until complete removal of $FeNO_3$ is ensured. In the concluding step, the graphene layer, which remains on the water's surface, is transferred onto the designated substrate. The substrate is immersed in the water, allowing the graphene to settle onto it. Finally, the sample is carefully lifted from the water.

Macro Device Fabrication

Macro devices were fabricated prior to the fabrication of micro devices to develop repeatable and reliable recipes. The first step of the fabrication process is e-beam evaporation. The chamber is pumped down to 6×10^{-3} mTorr before deposition. Chromium was used as an adhesion layer. During Cr deposition, the electric current was gradually raised to 8 mA to achieve a consistent deposition rate of 0.2 Å/s. Once it was confirmed that this was a stable condition, current was increased 0.5 mA per minute until reaching 12 mA to achieve a deposition rate of 0.5 Å/s. While developing the recipe, Cr of 50 nm thickness was deposited. Subsequent coatings, including the ones for the microstructures, were executed based on this process.

During Pt deposition, rapid increments in the applied current to the Pt crucible led to the occurrence of sparking, this caused both inefficient use of resources, unstable deposition rates and poor uniformity. As such, the deposition was carried out very slowly. However, the longer process still meant that the chamber heated up significantly since Pt requires high applied current due to its higher melting point. 90mA current was reached in 3 hours by initially increasing the current in steps of 0.5 mA every 30 seconds. After the Pt had melted, the current step was increased to 1 mA every 30 seconds. A 0.1 Å/s deposition rate was achieved while applying a current of 91mA. For the initial sample used to develop the recipe, a Pt layer of 23 nm was coated. All the following Pt depositions were based on this process. With all the measures to prevent sparking, unstable deposition rates, taking breaks during the deposition to allow the chamber to cool, this recipe ended up being very challenging to carry out. Therefore, it was decided to deposit Pt as a thin capping layer for Cr with a thickness of 7 nm.

TiO_2 was sputtered in RF mode using a TiO_2 target 20 nm thick in 20 minutes with conditions involving 20 sccm Ar, ~7 mTorr chamber pressure, 100 W power, 16% CT, 56% CL using Vaksis PVD Handy Twin Sputtering System-3 at Bilkent UNAM. Prior to starting the reaction, chamber pressure is pumped down to below 5E-6 Torr. TiO_x layer was sputtered with the Leybold L560 Box Coater in the Advanced Research Laboratory. TiO_x layer was sputtered using a Titanium target with Argon, while giving a minimal amount of oxygen (<5%) to prevent the cessation of the reaction. 20 nm thick TiO_x was coated with 200 sccm of Argon, 4 sccm of O_2, 150 W power conditions at 3 Å/s deposition rate. The macro device fabrication is then completed through the transfer of a graphene layer onto the substrate. Fig. 1 shows layers and fabrication process of the macro Pt/TiO_2/TiO_x/Graphene device.

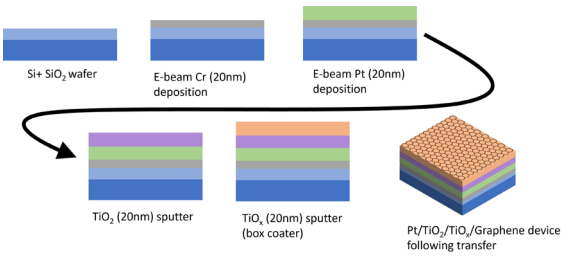

Figure 1. Layers and fabrication process of the macro Pt/TiO_2/TiO_x/Graphene device involving sequentially e-beam deposition, sputtering and graphene transfer

Micro Device Fabrication

The fabrication of memristor devices with graphene top electrodes arranged in a crossbar pattern is made possible by a set of 3 masks: Mask 1 for the bottom electrode, Mask 2 for the active layer and graphene, and Mask 3 for the top contact pads. There are 52 1 cm^2 chips on wafer with 3 different structure types and varying dimensions. Table 1 shows the pad dimensions for the memristive device with graphene top electrode.

Table 1. Pad dimensions for the micro memristive structures with graphene top electrodes

	Pad dimensions	*Active layer dimensions*
Large single device	*100 µm × 100 µm*	*100 µm × 226.09 µm*
Small single device	*21.74 µm × 21.74 µm*	*21.74 µm × 52.17 µm*
Large 8×8 crossbar	*47.83 µm × 47.83 µm*	*12.3 µm × 534.78 µm*
Small 8×8 crossbar	*21.74 µm × 21.74 µm*	*21.74 µm × 60.87 µm*
12×12 crossbar	*21.74 µm × 21.74 µm*	*8.7 µm × 408.7 µm*

Fig. 2 illustrates the structure of the single device, which consists of a top layer made of Cr and Pt electrode pads, an active layer made up of a stoichiometric TiO_2/TiO_x topped with graphene, and a bottom layer made of Cr and Pt electrode pads. The horizontal lines in the mask set are created using the bottom electrode mask, while the vertical lines are created using the top electrode mask.

Prior to fabricating the device featuring a graphene top electrode, a more traditional memristor with a platinum top electrode had already been fabricated and characterized (20). As such, the fabrication process had been tested and

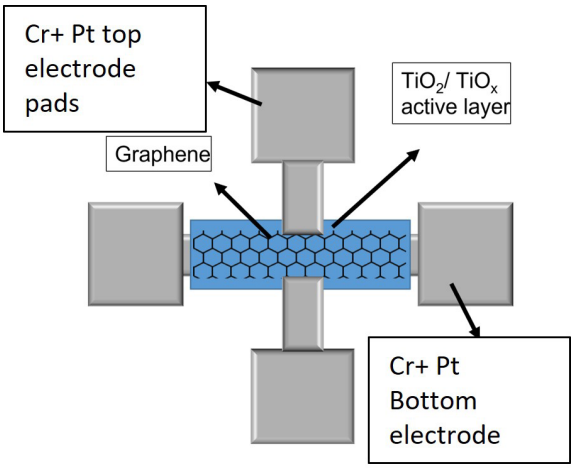

Figure 2. Top view of micro memristor structure with graphene top electrode consisting of Cr+Pt top electrode pads, TiO_2/ TiO_x active layer, Cr+Pt bottom electrode

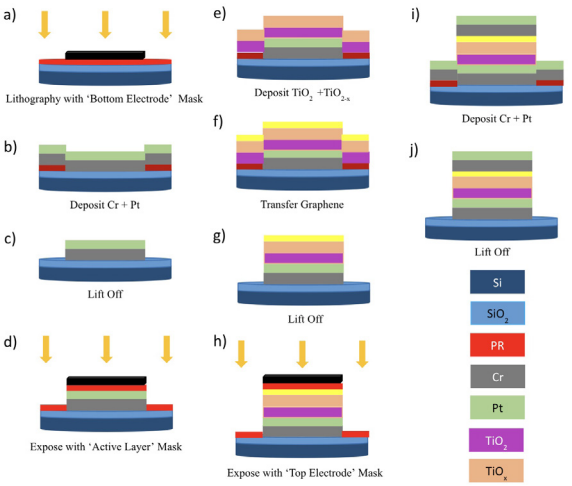

Figure 3. Fabrication process flow of micro Pt/TiO_2/TiO_x/Graphene device with graphene top electrode including (a)lithography with bottom electrode mask, (b)depositing Cr+Pt, (c)lift off, (d)exposing with active layer mask, (e)depositing TiO_2/TiO_x (f) transferring graphene, (g)lift off, (h)exposing with top electrode mask, (i) depositing Cr+Pt, (j)lift off.

verified except for the graphene transfer, patterning and characterization.

Fig. 3 illustrates the fabrication process of memristor with graphene top electrode. A Si wafer with SiO_2 (300nm) passivation layer was used. Then, photolithography technique was initially used to create the bottom electrode, as shown in Fig. 3(a), using a mask aligner. AZ5214E was chosen as the photoresist for the photolithography stage due to its ability to facilitate image reversal (21). In the mask aligner, the contact mode was selected as vacuum+hard and the separation, which means the distance between the mask and the substrate during alignment, was determined as 50 µm. The mask thickness was chosen as 2.3mm, the 4-inch wafer thickness as 0.5mm, and the photoresist thickness as 1.4 µm. The UV exposure dose was determined as 50 mJ/cm². Prior to the flood exposure step, it is essential to undergo an annealing process, also known as hard bake, for 2 minutes on each layer. Afterward, by adjusting the UV exposure dose to 230 and performing the flood exposure step without photomask, the lithography process was completed just as it was for each layer. The top of the wafer, which was obtained after the development stage using AZ400K as a developer, was coated with 20 nm layer of Cr and 7 nm layer of Pt, as depicted in Fig. 3(b), using e-beam process that was developed and described for the macro devices. Following the application of the optimized lift-off technique using acetone, as shown in Fig. 3(c), the photolithography stage for the active layer commenced, as illustrated in Fig. 3(d). Upon the completion of the development phase, the top of the wafer was coated with 20 nm layer of TiO_2 and then 20 nm layer of TiO_x using sputtering, as illustrated in the Fig. 3(e).

The sputtering was carried out using the same recipe that was described for macro devices. This combination of materials allows for resistive switching to occur through the movement of oxygen vacancies within the active layer.

Graphene was transferred directly after the sputtering of TiO_x, as depicted in Fig. 3(f). Upon transferring the graphene onto the wafer, the lift-off technique was applied, as shown in the Fig. 3(g), and the patterned graphene was examined using a microscope. Fig. 4 shows the orange line border indicating the graphene area on a 4-inch wafer. After completing the photolithography and development stages for the top electrode, as depicted in Fig. 3(h), which will form the final layer of the device, the top of the wafer was coated with 7 nm layer of Pt on 20 nm layer of Cr using the e-beam evaporator, as shown in Fig. 3(i). By utilizing the optimized lift-off stage with acetone, as depicted in the Fig. 3(j), the desired device was obtained. Fig. 5 shows microscope

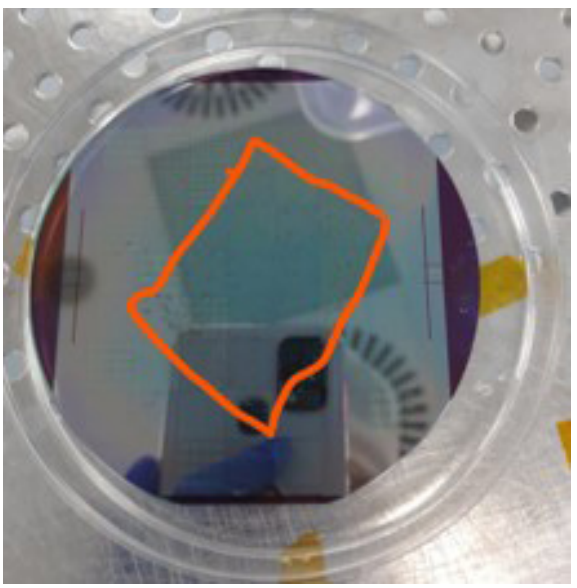

Figure 4. Photograph of micro patterned 4-inch full wafer just after graphene transfer on top of photoresist TiO_2/TiO_x before lift-off is completed to pattern active layer and graphene. The area with graphene is bordered by orange line for clarity.

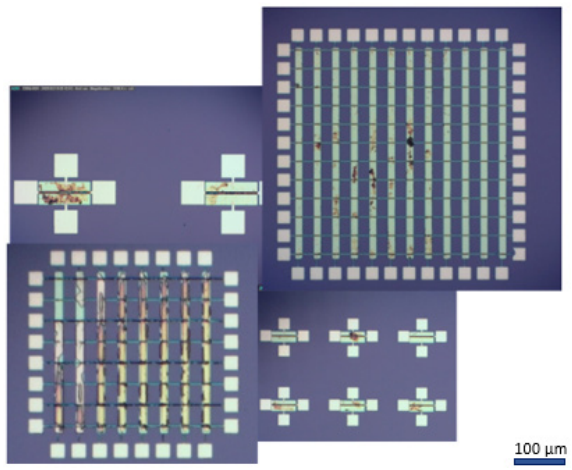

Figure 5. Optical microscope photographs of the fabricated micro memristive structures with graphene top electrodes

photographs of the graphene top electrode microstructures in which the electrode pads were coated and patterned after transferring the graphene.

RESULTS AND DISCUSSION

$Pt/TiO_2/TiO_x$/Graphene Macro Devices

Upon completing the fabrication of conventional memristors with platinum top electrodes, we initiated the production of graphene top electrodes using macro samples for convenience. Therefore, we obtained novel devices. The fishing method was employed for transferring the graphene. This method can be used to transfer large, macroscopic samples of graphene, which can be convenient for certain applications.

A Sigma Aldrich micro pipette was utilized to control the amount of liquid that was dripped into the macro memristor. The ratio of glucose syrup to water was 1:10 in both experiments.

The graphene macro device, which has the sample dripped and connected to the NI PXIe4139, appears as illustrated in Fig. 6. By connecting the device to the NI PXIe4139, it is possible to perform detailed electrical measurements and gain insight into the device's behavior and performance.

The measurements were conducted by exciting the devices with an input current signal and measuring the resulting voltage across it. Hence, strictly speaking Fig.7 shows a V-I curve where input signal is current, this figure clearly depicts the memristive behavior exhibited by the graphene top electrode macro device where the R_{OFF}/R_{ON} ratio is 80.

Fig. 8(a) presents the memristance measurement results for three different conditions: without a sample (represented by blue), with a water drop (represented by black),

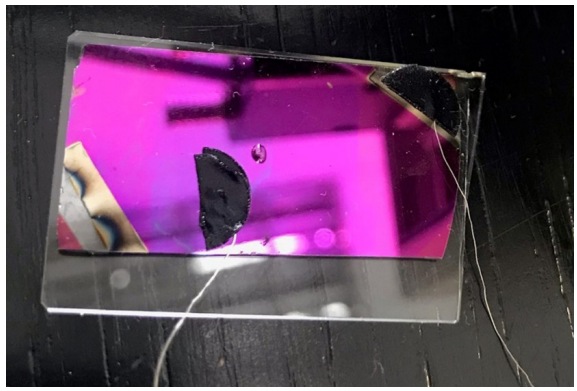

Figure 6. Fabricated macro $Pt/TiO_2/TiO_x$/Graphene device's measurement setup with sample

and with a 1 µl glucose syrup water drop (represented by green). As shown in the figure, the addition of a 1µl glucose syrup water drop led to lower memristance values.

In the absence of liquid on the graphene surface, the memristor exhibits high ROFF values (450 kΩ in the first cycle, 320 kΩ-350 kΩ in the second cycle). The addition of a 4 µl water drop resulted in a ROFF value that was similar to the value obtained in the absence of a sample, but lower (400 kΩin the first cycle, 250 kΩ-280 kΩ in the second cycle). The addition of a 1 µl drop of a glucose syrup water mixture resulted in a significant decrease in the ROFF value, which became stable at 173 kΩ. The RON values were measured as follows: 104 kΩ with the addition of glucose syrup, 122 kΩ with water, and 125-129 kΩ in the control condition with no sample present. These results provide sufficient evidence to establish a trend.

Fig. 8(b) shows the results of observations of water drops with varying amounts of glucose syrup. The figure illustrates the memristance measurement results for three distinct conditions: the absence of a sample, represented by blue; the presence of a 1 µl glucose syrup water drop, represented by green; and the presence of a 4 µl glucose syrup water drop, represented by red. The results obtained from mixing 4 µl of glucose syrup with water were similar to those obtained when using only water. When the droplet with 4 µl glucose syrup was deposited, ROFF was 315 kΩ and 280

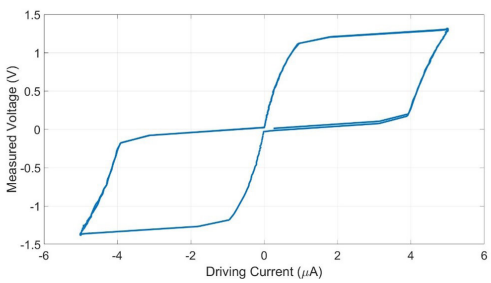

Figure 7. Driving current vs. measured voltage curve of graphene top electrode macro memristive device driven by a square wave current of 83 Hz 5µA amplitude with pinched hysteresis

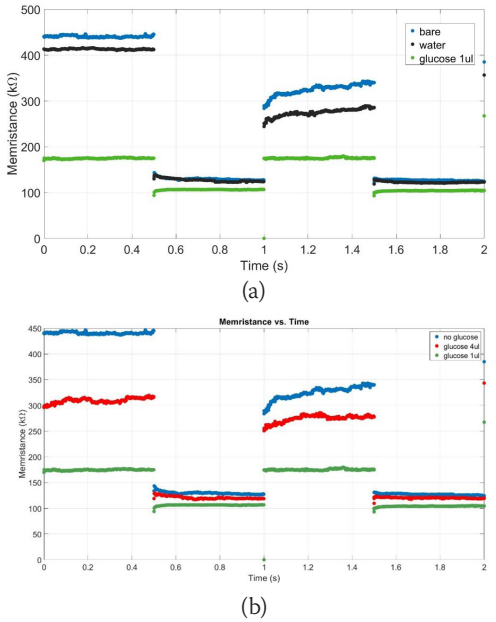

Figure 8. (a) Memristance measurement results of macro Pt/TiO_2/TiO_x/Graphene device without sample, with water drop, with 1µl glucose syrup water drop (b) Memristance measurement results of macro t/TiO_2/TiO_x/Graphene device without sample, with 1 µl glucose syrup water drop, with 4 µl glucose syrup water drop

kΩ and RON was 120 kΩ. Depositing a liquid sample on top of the graphene electrode clearly changes the conductivity mechanism of the electrode and possibly influences the active layer underneath.

Pt/TiO_2/TiO_x/Graphene Micro Devices: Graphene Characterization

Fig. 9 shows patterned graphene with optimized lift-off. Achieving a successful result with graphene after lift-off typically depends on the ability to maintain the continuity of the graphene layer during the transfer process (22). In order to maintain the continuity of graphene, it is important to use a high-resolution photolithography system, choose carefully the photoresist material and determine the lift-off time (23). If the lift-off time is not carefully controlled, it can lead to damage to the graphene layer. This may involve conducting experiments to determine the optimal lift-off time for a particular application or using advanced techniques such as atomic force microscopy to monitor the lift-off process in real- time.

In the context of lift-off processes, Raman spectroscopy plays a pivotal role in confirming the existence and quality of graphene (24). The top of the active layer is covered with graphene, Fig. 10 (a) shows the device and area that was analyzed, and Fig. 10(b) showcases discernible G and 2D peaks, signature of graphene. Raman analysis substantiates the existence of few-layer graphene with structural integrity and continuity.

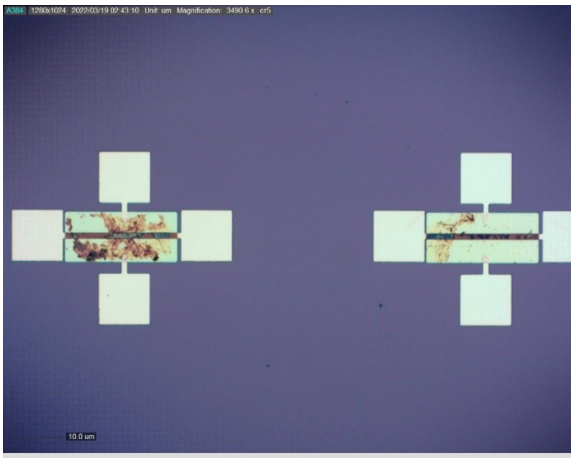

Figure 9. Top view optical microscope photograph of micro memristive device after graphene patterning with optimized lift-off

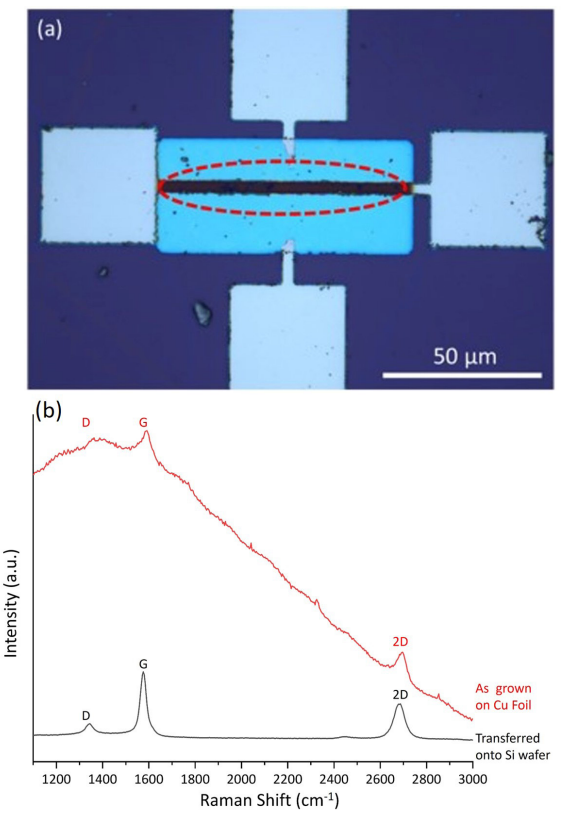

Figure 10. Verification of few-layer graphene (a) Top view optical microscope photograph of the micro Pt/TiO_2/TiO_x/Graphene device the red dashed circle marks the area where Raman Spectroscopy is performed (b) Raman spectrum of graphene prior to transfer to the wafer (shown in red) and after having been transferred and patterned (shown in black) on the micro Pt/TiO_2/TiO_x/Graphene device

Pt/TiO_2/TiO_x/Graphene Micro Devices: I-V Characterization

I-V measurements can be used to assess the device's performance and determine input dependent variations in its resistance. Electrical characterization results in Fig. 11 show that the graphene top electrode micro memristive

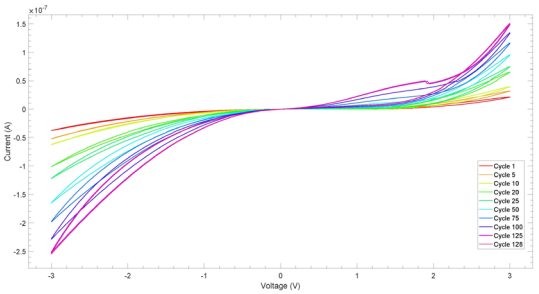

Figure 11. I-V Measurements of micro Pt/TiO_2/TiO_x/Graphene device

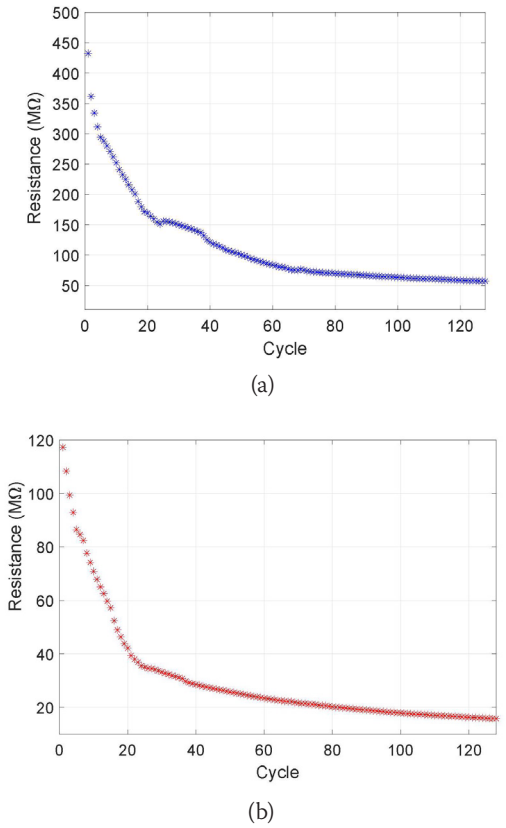

Figure 12. Resistance values of the device were measured at V_{read}=2.1V to show the cycle-to-cycle variation in each quadrant(a) Resistance of micro Pt/TiO_2/TiO_x/Graphene device for positive quadrant during 128 cycles (b)Resistance of micro Pt/TiO_2/TiO_x/Graphene device for negative quadrant during 128 cycles

device clearly exhibits diodic behavior in both the positive and negative quadrants. Unlike the macro devices, distinct resistance states are not demonstrated by this device. However, the resistance is input dependent. Moreover, there is a cycle-to-cycle variation in resistance. this can be deduced when one compares the I-V plot from earlier cycles to later cycles: the red plot (Cycle 1) shows a high resistance and magenta plot (Cycle 128) shows a much lower resistance. This is better demonstrated in Fig. 12 which depicts the drop in device resistance from one cycle to the next. This drop in resistance is more rapid at first in both quadrants e.g. as shown in Fig. 12 (a) a drop from 450 MΩ to 150 MΩ is observed in the HRS value in the positive quadrant during the first 20 cycles, after which the resistance settles more gradually to around 50 MΩ during the next 108 cycles. This trend applies to both quadrants. These micro devices exhibit much higher resistances and are susceptible to charging. This would explain the cycle-to-cycle variation. The device resistance in both quadrants exhibit some hysteresis and consecutive cycles show that resistance decreases gradually due to excitation.

CONCLUSION

A fabrication method to utilize graphene as a top electrode in memristive devices is presented. Electrical and structural characterization results demonstrate that: (i) graphene is a promising material to utilize memristive devices as sensors and (ii) the developed fabrication method and lift-off method yields continuous, patterned graphene top electrodes. Both sets of devices, macro and micro, were fabricated using the same deposition and transfer methods. The microstructures were patterned using photolithography and lift-off. Electrical characterization was carried out in all cases by applying the input signal to the top electrode and grounding the device from the Pt bottom electrode. The first and most fundamental aim of electrical characterization was to demonstrate that the graphene in fact functions as an electrode i.e. an applied current results in a potential difference across the grounded bottom electrode and the graphene electrode, or if the input is a voltage signal, that this input results in a current that flows from the bottom electrode to the graphene electrode. Secondly, as the aim was to utilize memristive dynamics, it was important to verify the that these devices exhibited memristance. Both were demonstrated through I-V measurements as shown in Fig. 7 and Fig. 12. Both macro and micro devices exhibit input dependent memristance. In the case of the macro device distinct resistance states were observed which enabled sensor measurements to show that these Pt/TiO_2/TiO_x/Graphene devices could discern between a state of having no deposited sample, a water drop, and a glucose drop.

These experiments yielded convincing results. Lastly, since the fabrication method is novel to our knowledge graphene had to be tested with surface measurement techniques such as Raman to corroborate that it remained continuous after the lift- off process. These measurements also produced positive results.

This work has attained encouraging results. Memristive devices with graphene top electrodes have the potential to have a significant impact in the future, given the many advantages of graphene as a material. They may be used in a variety of applications, including in memory and computing

devices, as well as in sensors and energy storage systems. Graphene is a promising material for use in memristive devices, due to their excellent electrical and mechanical properties, as well as their high strength and flexibility.

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CONFLICT OF INTEREST

Authors approve that to the best of their knowledge, there is not any conflict of interest or common interest with an institution/organization or a person that may affect the review process of the paper.

AUTHOR CONTRIBUTION

Selin Onay: Fabrication, Writing- original draft
Omer R. Caylan: Graphene synthesis, transfer, Raman measurements
Goknur Buke: Graphene characterization analysis, writing- review and editing
Itır Koymen: Conceptualization, Electrical characterization, Methodology, Analysis, Supervision, Writing-review and editing

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