GU J Sci 30(3): 273-280 (2017)

Gazi University

**Journal of Science**

http://dergipark.gov.tr/gujs

# Interface Effects of Annealing Temperatures in Al/$HfO_2$/p-Si (MIS) Structures

Şadan ÖZDEN[1,*], Osman PAKMA[2]

[1]*Department of Physics, Faculty of Science, Muğla Sıtkı Koçman University, 48000, Muğla, Turkey*

[2]*Department of Physics, Faculty of Science and Art, Batman University, 72100, Batman, Turkey*

**ArticleInfo**

*Received: 26/03/2017*
*Accepted: 25/05/2017*

**Keywords**

*High dielectric materials,*
*sol-gel,*
*MIS devices*

**Abstract**

In this study, Al/$HfO_2$/p-Si (MIS) structures were prepared by using the sol-gel method for three different annealing temperatures. The current-voltage (I-V) and capacitance-voltage (C-V) characteristics of these structures were investigated by taking into consideration the effect of the interfacial insulator layer and surface states ($N_{ss}$) at room temperature. All of the structures showed non-ideal I-V behaviour with ideality factor (n) in the range between 2.35 and 4.42 owing to interfacial insulator layer and surface states. The values of $N_{ss}$ and barrier height ($\phi_b$) for three samples were calculated. The values of n and $N_{ss}$ ascend with increasing the insulator layer thickness (δ) while the values of $\phi_b$ decreases.

## 1. INTRODUCTION

Metal-semiconductor (MS) and metal-oxide-semiconductor (MOS) diodes are of great importance for contributing to the understanding of the semiconductor surface and surface states. Any insulator layer, produced between metal and semiconductor by means of the natural or deposition process, causes the metal-insulator-semiconductor (MIS) diode having non-ideal behavior. Thus, the "ideality factor (n), surface states ($N_{ss}$), and barrier height ($\phi_b$) of an MIS structure significantly differ from the expected magnitudes, which is mainly caused by the potential drop across the insulate layer due to the interface states at insulator/Si interface [1-7]. Recently, the growth of various insulators on single crystalline silicon, such as $SnO_2$ [8], $Si_3N_4$ [9], $TiO_2$ and hafnium dioxide ($HfO_2$) [10-11], in MIS structures has been subject to extensive research as an alternative to silicon-dioxide ($SiO_2$). The small number of surface states, high dielectric permittivity and high breakdown voltage are among the important advantages of these films when compared to $SiO_2$. MIS diodes produced by $HfO_2$ thin films are also of considerable importance due to the same advantages.

$HfO_2$ is one of the most common and stable compounds of hafnium. Therefore $HfO_2$ is used in optical coatings, and as a high-κ dielectric in DRAM capacitors and in advanced metal-oxide-semiconductor devices [12]. In view of the these facts, the experimental investigations on Al/$HfO_2$/p-Si (MIS) structures prepared by the sol-gel method at three different preparation temperatures have been carried out and their main electrical parameters such as $\phi_b$, n and $N_{ss}$ have been investigated by taking into account the effect of the interfacial insulator layer. To explain the forward bias I-V and $C^{-2}$-V characteristics, the model provided in literature has been used [3-6].

*Correspondingauthor, e-mail:sozden@mu.edu.tr

## 2. EXPERIMENTAL

### 2.1. Al/$HfO_2$/p-Si Structures Preparation

To prepare the $HfO_2$ solution, 0.0063 mol hafnium tetrachloride was dissolved in 15 mL ethanol, to which 0.08 mol $H_2O$ and 0.013 mol $HNO_3$ were added and the solution was kept in a magnetic stirrer for 2 hours. Finally, before coating the film, the solution was maintained at 50 °C for 4 hours.

Metal-oxide-semiconductor (Al/$HfO_2$/p-Si) structures were manufactured on the 1-inch diameter float zone (100) p-type (boron-doped) single crystal silicon wafer with a thickness of 280 μm and a resistivity of 1–10 Ω.cm. For the fabrication process, Si wafer was degreased through the RCA cleaning process (i.e., a 10 minute boiling in $NH_4OH + H_2O_2 + 6$ DI (18 MΩ deionised water), which was followed by a 10 minute boiling in $HCl + H_2O_2 + 6$ DI) [10, 13]. Then, it was subjected to the drying process in $N_2$ atmosphere for a duration time. After that, high-purity aluminum with a thickness of 1500 was thermally evaporated from the tungsten filament onto the whole back surface of the Si wafer under the pressure of $10^{-6}$ Torr. In order to obtain a low-resistivity ohmic back contact, Si wafer was sintered at 580 °C for 3 minutes in $N_2$ atmosphere. The native oxide on the front surface of the substrate was removed in $HF : H_2O$ (1 : 10) solution, and finally, the wafer was rinsed in deionised water for 30 s before forming an $HFO_2$ layer on the p-type Si substrate. The prepared $HFO_2$ solution was coated on the shiny side of the cleaned p-Si surface at 2000 rpm by the sol-gel spinning technique. The $HfO_2$/p-Si structures were annealed for five minutes at 100, 200, and 300 °C in $N_2$ atmosphere after each coating process. The process was repeated in the same way until the required film thickness was obtained and the structure was finally exposed to annealing at 500 °C in $N_2$ atmosphere for 1 h.

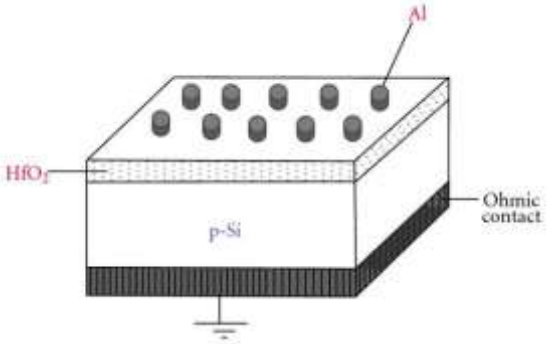


***Figure 1.*** *Schematic diagram of Al/$HfO_2$/p-Si (MIS) structure.*

A high-purity aluminum layer (2000 Å) was coated on the surface in a vacuum under the pressure of $10^{-6}$ Torr in order to obtain a rectifying contact on the front surface of p-Si coated with $HfO_2$. The structure of Al/$HfO_2$/p-Si/Al (MIS) structures is given in Figure 1. The preparation data of $HfO_2$ thin films on Si wafer substrate are given in Table 1.

***Table 1.*** *Preparation data of $HfO_2$ thin films prepared on Si wafer substrate.*

| Nr. | Structure | Treatment Temperature and Time | Insulator layer, thickness δ(Å) |
|---|---|---|---|
| S1 | Al/$HfO_2$/p-Si | 100 °C, 5 min. | 126 |
| S2 | Al/$HfO_2$/p-Si | 200 °C, 5 min. | 108 |
| S3 | Al/$HfO_2$/p-Si | 300 °C, 5 min. | 95 |

### 2.2. Characterization

The insulator layer thicknesses of prepared devices were measured by Avantes spectrometer (AvaSpec-ULS2048). The current-voltage (*I-V*) and capacitance-voltage (*C-V*) measurements, carried at 500 kHz with a test signal of 50 $mV_{rms}$, were performed by Keithley-4200 semiconductor characterization system (SCS) at room temperature and in a darkened and sealed metal box, respectively.

## 3. RESULTS AND DISCUSSION

The energy band diagram of an MIS structure at forward bias is presented in Figure 2. The parameters $\phi_m$, $\chi$, $\Delta$ and $\delta$ are the work function of metal, the electronic affinity of the semiconductor, the voltage drop across the interface insulator layer, and the thickness of the insulator layer, respectively. The parameter $\phi_0$ is commonly defined as the neutral level of surface states taken from the valance band edge at the semiconductor surface [14]. $V_p$ is the potential difference between the Fermi level and the top of valence band in the neutral region, and $\phi_e$ is the effective barrier height.

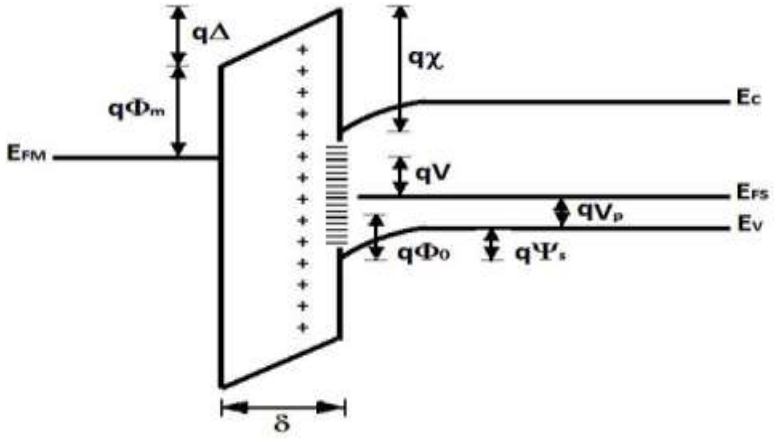


***Figure 2.*** *The energy band diagram of a MIS system under non-equilibrium condition.*

From the energy band diagram, the potential drop $\Delta$ across the interface layer can be determined by Gauss's law [7, 14];

$$\Delta = -\left[\frac{E_g}{q} + \chi - \phi_e - \phi_m\right] = \frac{\delta}{\varepsilon_i}\left(Q_{sc} + Q_{it} + Q_f\right) \tag{1}$$

where $Q_{sc}$ is the semiconductor depletion layer charge, $Q_{it}$ is the interface trap charge at bias $V$, $Q_f$ is the fixed surface charge at the semiconductor interface and $\varepsilon_i$ is permittivity of the insulator layer. The depletion charge is given by

$$Q_{sc} = -\left[2q\varepsilon_s N_A(\phi_e - V_n)\right]^{1/2} \tag{2}$$

where $N_A$ is the doping concentration and $\varepsilon_s$ is the permittivity of semiconductor. The interface state charge is:

$$Q_{it} = -qN_{ss}(q\phi_e - q\phi_0) \tag{3}$$

where $N_{ss}$ is the density of the interface states. From the above equations, the following expressions can be written as:

$$c_1 = 2q\varepsilon_s N_A \delta^2 / \varepsilon_i^2 \tag{4a}$$

$$c_2 = \varepsilon_i / (\varepsilon_i + q^2 \delta N_{ss}) \tag{4b}$$

$$\phi_e = c_2(E_g / q + \chi - \phi_m) + (1 - c_2)\phi_0 + c_2(\delta Q_f / \varepsilon_i) = \phi_b + c_2(\delta Q_f / \varepsilon_i) \tag{4c}$$

where $\phi_b$ is the barrier height without fixed surface charge at thermal equilibrium and can be defined by

$$\phi_b = c_2(E_g / q + \chi - \phi_m) + (1 - c_2)\phi_0 \tag{5}$$

The depletion layer capacitance per unit area of a MS contact without interfacial layer can be given by

$$C = \left[q\varepsilon_s N_A / 2(V_d - V)\right]^{1/2} \tag{6}$$

From equation (6), the quantity of $C^{-2}$ can be written as

$$C^{-2} = 2(V_d - V)/q\varepsilon_s N_A \tag{7}$$

When a metal-semiconductor contact with interfacial layer (MIS) is considered, the depletion capacitance $C$ can be become [2],

$$C = c_2\left\{q\varepsilon_s N_A/2\left[\phi_b - c_2V - V_n + c_2(\delta Q_f/\varepsilon_i)\right]\right\}^{1/2} \tag{8}$$

and

$$C^{-2} = 2\left[\phi_b - c_2V - V_n + c_2(\delta Q_f/\varepsilon_i)\right]/c_2^2 q\varepsilon_s N_A \tag{9}$$

$c_2$ can be written as follows from the slope of the $C^{-2}$-$V$ plot

$$c_2 = \frac{2}{q\varepsilon_s N_A\left[d(C^{-2})/dV\right]} \approx \frac{N_A^{'}}{N_A} \tag{10}$$

where $N'_A$ is the experimental value of doping concentration and $N_A$ is the theoretical value of doping concentration. From the intercept of $C^{-2}$-$V$ plot with the voltage axis, the value of $\phi_b$ can be obtained as

$$\phi_b = (c_2V_0 + V_n) - c_2(\delta Q_f/\varepsilon_i) \tag{11}$$

From equations (6) and (11), the effective barrier height at thermal equilibrium may be defined as

$$\phi_e = (c_2V_0 + V_n) \tag{12}$$

where $V_0$ is the intercept voltage. According to equation (11), the barrier height without the fixed surface charge can be given by

$$\phi_b = (c_2V_0 + V_n) \tag{13}$$

In order to obtain $\phi_b$ or $\phi_e$, from equations (12) and (13), it is necessary to known the Fermi energy $V_n$. From equation (4b), the value of $c_2$ is a function of $\delta$ and $N_{ss}$.

Capacitance-voltage ($C$-$V$) measurements are performed at a sufficiently high frequency ($f \geq$500 kHz) to prevent the interface states responding to the ac signal [15, 16]. Therefore, the forward and reverse bias $C$-$V$ characteristics at 500 kHz for three different annealing temperatures are shown in Figure 3. The applied voltage was varied between -4 V and +4 V. From an MS or MIS structure, the doping density concentration ($N_A$), and the diffusion potential ($V_d$) can be directly achieved from the slope and the intercept with the voltage axis of $C^{-2}$ vs. $V$ plot [1, 2]. $C^{-2}$ vs. $V$ plots were shown in Figure 4. Values of $N_A$ and $c_2$ were calculated for all structures according to Eq. (10) using the slope data obtained from $C^{-2}$ vs. $V$ plots.

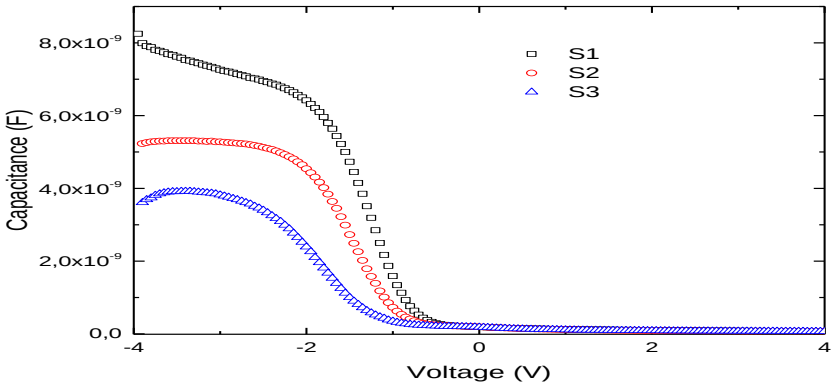


***Figure 3****. High frequency (500kHz) capacitance – voltage characteristics of Al/HfO₂/pSi (MIS) structures at room temperature.*

Then the values of $\phi_b$ were calculated, as the values of $c_2$ and $V_n$ are known. There is a linear correlation between $\phi_b$ and $c_2$ as shown in Figure 5. From the extrapolation of the line to $c_2$=1 the value of $\phi_b$ was found to be equal to 1.032 eV and also from the extrapolation of that to $c_2$=0 the value of neutral level $\phi_0$ of surface states was obtained as 0.12 eV.

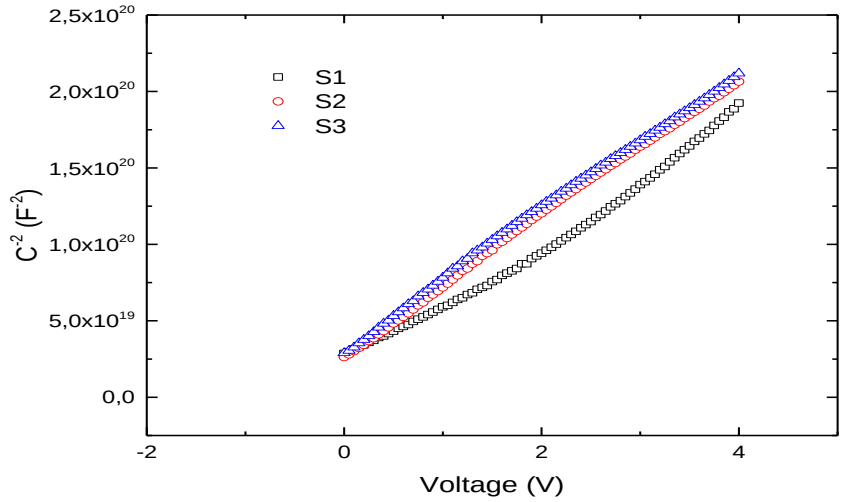


***Figure 4.*** *$C^{-2}$-V characteristics for 500 kHz of the Al/$HfO_2$/p-Si MIS structures at room temperature.*

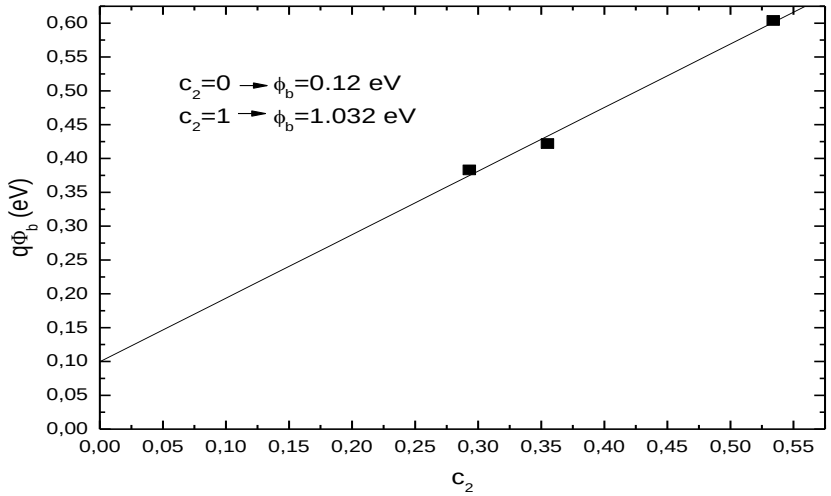


***Figure 5.*** *$\phi_b$ - $c_2$ plot of the Al/$HfO_2$/p-Si MIS structures at room temperature.*

Due to the existence of an insulator layer at M/S interface, it is assumed that there is a relation between the applied forward bias voltage $V$ ($V>3kT/q$) and the current $I$. According to the thermionic emission (TE) theory, the current is expressed as [1],

$$I = I_o \exp\left[\frac{qV}{(1+q^2\delta N_{ss}/\varepsilon_i)kT}\right] \tag{14}$$

where $I_0$ is the reverse saturation current and is given as

$$I_0 = AA^*T^2 \exp\left(-\frac{q\phi_b}{kT}\right) \tag{15}$$

where $\phi_b$, $A$, $A^*$, $n$, $q$ *and* $T$ are zero-bias barrier height, the rectifier contact area, the effective Richardson constant (32A/cm$^2$K$^2$ for p-type Si), ideality factory, the electron charge and the temperature in K, respectively. The value of $1+q^2\delta N_{ss}/\varepsilon_I$ can be considered as the ideality factor of the MIS structure. According to equation (4b), this factor should be equal to $1/c_2$.

Figure 6 shows the forward bias *lnI-V* characteristics of Al/$HfO_2$/p-Si (MIS) structures at the room temperature. The determined values of the ideality factor (n) range from 2.35 to 4.42. These values of *n* are appreciably high. Such behavior of ideality factor can be attributed to the interfacial insulator layer and interface states.

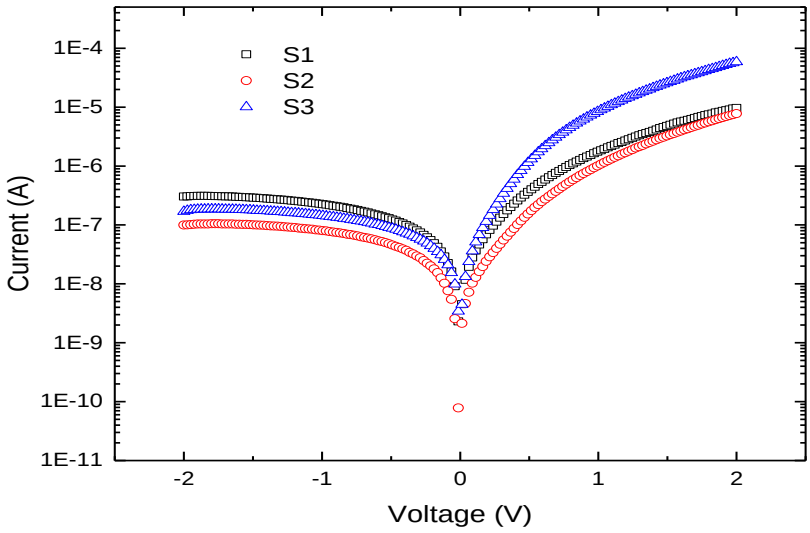


***Figure 6.*** *LnI-V characteristics of Al/$HfO_2$/p-Si (MIS) structures at room temperature.*

For a sufficiently thick interfacial insulator layer, the interface states are in equilibrium with the semiconductor and they cannot interact with the metal [2, 7, 14]. When $N_{ss}$ are in equilibrium in semiconductor, the general expression for the ideality factor, as deduced by Chard and Rhoederick [2], reduces to

$$n = 1 + \frac{\delta}{\varepsilon_i}\left[\frac{\varepsilon_s}{W_D} + qN_{ss}\right] \tag{17}$$

where $W_D$ is the width ot the depletion region and expressed as

$$W_D = \left[(2\varepsilon_s / qN_A)V_d\right]^{1/2} \tag{18}$$

Subsituting the value of permittivity of $HfO_2$ ($\varepsilon_i = 25\varepsilon_0$) [17, 18] and the thickness of $\delta$ in equations (17), the value of density of $N_{ss}$ for three different repeated annealing temperatures were thus obtained. In addition, the values of density of $N_{ss}$ for three different annealing temperatures were also obtained by using the value of $c_2$ and $\delta$ in equation (4b). These results were given in Table 2. As can be seen in Table 2, in these two cases, the value of density of interface states increases with increasing insulator layer thickness.

***Table 2.*** *Various parameters obtained from C-V (500 kHz) and I-V characteristics of Al/$HfO_2$/p-Si (MIS) structures at room temperature.*

| *Nr.* | *$1/c_2$* | *n* | $\phi_b$ (C-V) (eV) | $N_{ss}$ ($1/c_2$) ($10^{13}$ $eV^{-1}cm^{-2}$) | $N_{ss}$ (*n*) ($10^{13}$ $eV^{-1}cm^{-2}$) |
|---|---|---|---|---|---|
| S1 | 4.92 | 4.42 | 0.434 | 2.303 | 2.132 |
| S2 | 3.81 | 3.21 | 0.574 | 2.054 | 2.258 |
| S3 | 2.54 | 2.35 | 0.638 | 1.357 | 1.654 |

There is a difference between obtained barrier heights from C-V and I-V measurements. This situation frequently reported for MIS and MOS devices and can be caused by the existence of an interfacial layer and barrier inhomogenities. Sensitivities of C-V and I-V techniques to these effects are different [19].

## 4. CONCLUSION

The *I-V* and *C-V* characteristics of Al/$HFO_2$/p-Si (MIS) structures by using the sol-gel method were measured at room temperature for three different annealing temperatures. The calculated values of *n* were found in the range between 2.35 and 4.42, which may be the cause of the interface states densities localized at $HfO_2$/p-Si interface and the effect of insulator layer thicknesses at Al/p-Si interface. The values of $N_{ss}$ for three samples with different insulator layer thickness were also calculated. While the values of *n* and *Nss* decrease with decreasing the insulator layer thickness, the values of $\phi_b$ increase. In addition, the value of $\phi_b$ and $\phi_0$ was obtained to be 1.032 eV and 0.12 eV with help of correlation between $\phi_b$ and $c_2$, respectively. The experimental results caused by the thickness-dependent change in the interface states of insulator layers were consistent with the previous studies [3, 7]. Moreover, the obtained values of interface states were comparable with the order of magnitude of Al/$SnO_2$/p-Si and Al/$SiO_2$/p-Si (MIS) structures [20, 21].

## CONFLICT OF INTEREST

No conflict of interest was declared by the authors

## REFERENCES

[1] Sze, S. M., Kwok, K. Ng., Physics of Semiconductor Devices, John Wiley, New Jersey, USA, (2007).

[2] Card, H. C., Rhoederick, E. H., "Studies of tunnel MOS diodes I. Interface effects in silicon Schottky diodes", J. Phys. D, 4: 1589-1601, (1971).

[3] Chattopadhyay, P., Daw, A. N., "On the current transport mechanism in a metal - insulator - semiconductor (MIS) diode". Solid-State Electron., 29: 555-560, (1986).

[4] Turut, A., Karabulut, A., Ejderha, K., Bıyıklı, N., "Capacitance - conductance characteristics of Au/Ti/$Al_2O_3$/n-GaAs structures with very thin $Al_2O_3$ interfacial layer", Materials Res. Expr., 2: 046301-046310, (2015).

[5] Turut, A., Dogan, H., Yıldırım, N., "The interface state density characterization by temperature-dependent capacitance – conductance - frequency measurements in Au/Ni/n-GaN structures", Materials Res. Expr., 2: 096304-096312, (2015).

[6] Szatkowski, J., Sireanski, K., "Interface effects on Mg-$Zn_3P_2$Schottky diodes", Solid-State Electron., 31: 257-260, (1988).

[7] Turut, A., Yalçın, N., Sağlam, M., "Parameter extraction from non-ideal C−V characteristics of a Schottky diode with and without interfacial layer", Solid-State Electron., 35: 835-841, (1992).

[8] Serin, T., Serin, N., Karadeniz, S., Sarı, H., Tugluoglu, N., Pakma, O., "Electrical, structural and optical properties of $SnO_2$ thin films prepared by spray pyrolysis", J. Non-Cryst. Sol., 352(3): 209-215, (2006).

[9] Liu, Q. J., Yao, H., Wang, L., Hou, C. R., Zhao, W. Y., "Translocation of Gold Nanorod Through a Solid-State Nanopore", Science of Adv. Mater., 6(9): 2075 - 2078, (2014).

[10] Pakma, O., Serin, N., Serin, T., "The effect of repeated annealing temperature on the structural, optical, and electrical properties of $TiO_2$ thin films prepared by dip-coating sol–gel method", J. Matt. Sci., 44(2): 401 - 407, (2009).

[11] Wei, H. H., He, G., Liu, M., Liu, Y. M., Zhang, M., Chen, X. S., Sun, Z. Q., "Interfacial Control and Modulation of Band Alignment of Atomic Layer Deposition-Derived $HfO_2$/Si Gate Stack by Rapid Thermal Annealing", Science of Adv. Mater., 6(12): 2652 - 2658, (2014).

[12] Zhu, H., Tang, C., Fonseca, L. R. C., Ramprasad, R., "Recent progress in ab initio simulations of hafnia-based gate stacks", J Mater Sci., 47: 7399–7416, (2012).

[13] Kern, W., Handbook of Semiconductor Cleaning Technology, Noyes, New York, USA, (1993).

[14] Cowley, A. M., Sze, S. M., "Surface States and Barrier Height of Metal-Semiconductor Systems", J. Appl. Phys., 36: 3212-3220, (1965).

[15] Fonash, S. J., "A reevaluation of the meaning of capacitance plots for Schottky-barrier-type diodes", J. Appl. Phys., 54(4): 1966-1975, (1983).

[16] Nicollian, E. H., Brews, J. R., Metal-Oxide Semiconductor (MOS) Physics and Technology, Wiley, New York, USA, (1982).

[17] Balog, M., Schieber, M., Michman, M., Patai, S., "Chemical vapor deposition and characterization of $HfO_2$ films from organo-hafnium compounds", Thin Solid Films, 41(3): 247-259, (1977).

[18] Housa, M., High k Gate Dielectrics, CRC Press, Boca Raton, USA, (2003).

[19] Aydın, M.E., Yakuphanoğlu, F., Eom, J.-H., Hwang, D.-H., "Electrical characterization of Al/MEH-PPV/p-Si Schottky diode by current-voltage and capacitance-voltage methods", Physica B, 387: 239-244, (2007).

[20] Altındal, S., Kanbur, H., Tataroğlu, A., Bülbül, M. M., "The barrier height distribution in identically prepared Al/p-Si Schottky diodes with the native interfacial insulator layer ($SiO_2$)", Physica B, 399: 146-154, (2007).

[21] Özer, M.,D., Yıldız, E., Altındal, S., Bülbül, M. M., "Temperature dependence of characteristic parameters of the Au/$SnO_2$/n-Si (MIS) Schottky diodes", Solid State Electron., 51: 941-949, (2007).