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Analysis of Hybrid Multilevel Inverters Using a Reduced Voltage Stress Switch

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Abstract: In this paper, a new multilevel inverter topology using a reduced number of switches, insulated gate driver circuits and voltage standing on switches is proposed. The presented topology is a hybrid modular multilevel inverter. The operation of the proposed inverter is the same as the conventional three-level inverter. The proposed converter creates positive and zero voltages in phase. The proposed topology combines a three-phase inverter and sub single phase-units. This topology can be used as symmetric and asymmetric converter. One algorithm for determining the magnitudes of DC voltage sources has been presented in the asymmetric state. The validity of the analysis has been proved by simulation and experimental results with a laboratory prototype.

Keywords: Power electronics, energy conversion, multilevel inverter, device reduction.

1. Introduction

In the recent years, many different multilevel inverter topologies and a wide variety of applications have been developed [1–4]. Three multilevel inverter topologies are commonly used, which are the neutral point diode clamped; flying capacitor and the cascaded H-bridge. The multilevel inverter topologies can be used in energy conversion. The power conversion interface is important to load or grid-connect distributed power generation systems.

The cascaded H-bridge multilevel inverter (CHB) combines single-phase inverters. This structure needs low-voltage components to output medium and high voltage levels. Using semiconductors with low peak inverse voltage is a main advantage of CHB. Furthermore, CHB has a high modularity degree. The CHB can be operated as symmetric and asymmetric converter [5-7]. The symmetric CHB makes use of equal DC voltage sources while asymmetric CHB inverters use DC voltage sources with unequal values. The asymmetric

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topology provides a good opportunity to increase the number of levels with reduced total harmonic distortion (THD). Furthermore, the number of voltage levels is maximized when the value of DC voltages form a geometric progression with a factor of three.

One clear disadvantage of the multilevel inverter is the great number of power semiconductor switches needed. Each switch requires a related gate driver and protection circuits. This may lead to the overall system being more expensive and complex. Therefore, in practical implementations, decreasing the number of switches and gate driver circuits is very important. In recent years, new topologies of symmetrical and asymmetrical multilevel inverters have been investigated to increase the number of levels with a small number of switches and gate driver circuits [7-12]. A new multilevel converter topology, which can synthesize all possible additive and subtractive combinations of input DC levels in the output voltage waveform with fewer power electronic switches has been introduced in [12]. The operation of this topology is identical to the asymmetrical CHB with factor of three. This topology produces nine levels by eight switches.

Another disadvantage of multilevel inverters is that the small voltage levels are typically produced by isolated voltage sources or a bank of series capacitors. Isolated voltage sources may not always be readily available and series capacitors require a voltage balancer circuit [13, 14].

This paper presents a new three-phase multilevel inverter topology based on the three-level inverter configuration. In fact, the proposed converter produces positive levels only in phase. This inverter increases the number of output voltage levels by using a minimum number of power switches and driver circuits. Finally, experimental results obtained from the three phase inverter confirm the correct performance of the proposed topology in generating the voltage levels.

2. Multilevel Inverter

Figure 1 shows the power circuit of the proposed three-phase multilevel inverter. In this inverter, each phase consists of series-connected basic units. Based on the desired value of the output voltage, the number of output voltage levels, and the voltage stress of switches, a number of basic units is used in series. Figure 2 shows the basic unit. In the proposed structure, the DC sources that are marked as V_1 are used for all phases.

As Figure 2 shows, the proposed basic unit consists of two DC voltage sources, one bidirectional switch (T_{2a}) and two unidirectional switches (T_{1a} and T_{3a}). The basic unit is able to produce three voltage levels (two positive levels and one zero level) at the output. In any

time instant, only one switch is turned on. Switches cannot be ON simultaneously to avoid the occurrence of short circuits across the DC sources. The output voltage levels of the basic unit based on switching patterns are described as:

If the switch T_{1a} is ON, V_{O1} =0.

If the switch T_{2a} is ON, $V_{O1} = V_1$.

If the switch T_{3a} is ON, $V_{O1} = 2V_1$.

As Figure 1 shows, the new cascaded multilevel inverter can be made by a series connection of *n* basic units. The phase voltage of the proposed inverter is equal to adding the output voltage of each unit and it can be written as follows:

$$V_{OA} = V_{OA1} + V_{OA2} + ... + V_{OAn}, \tag{1}$$

where *n* is the number of series connected basic units in any phase.

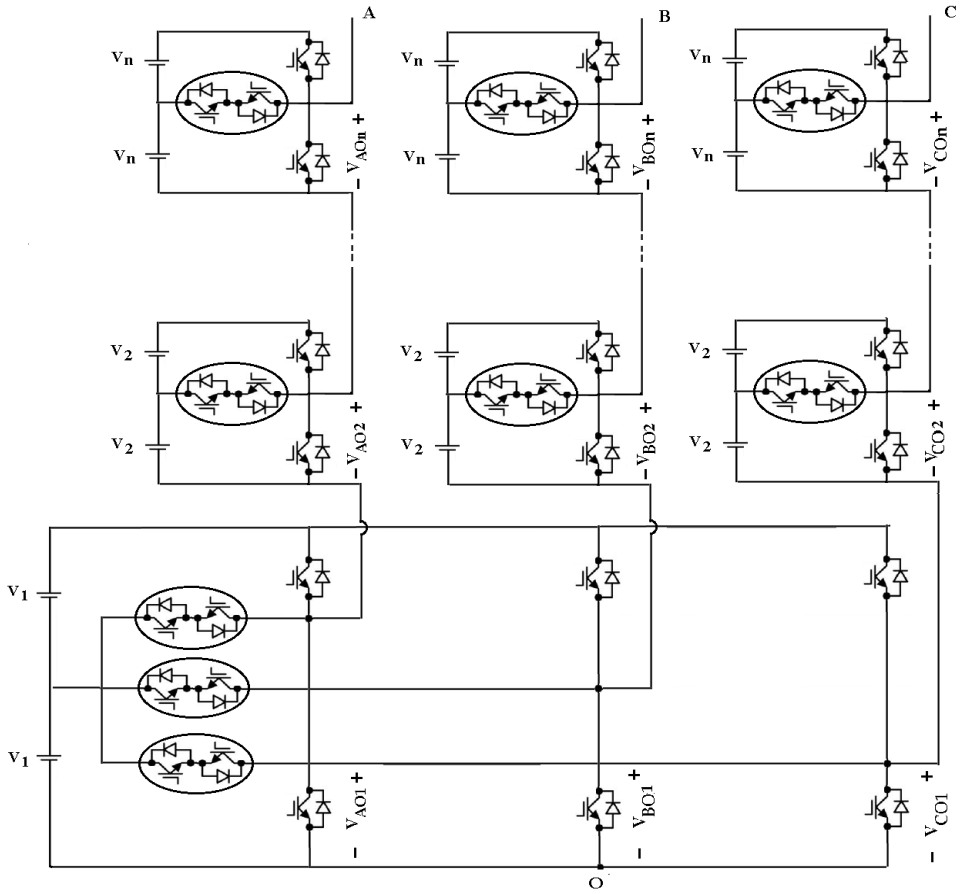


FIGURE 1. Power circuit of the proposed three-phase multilevel inverter.

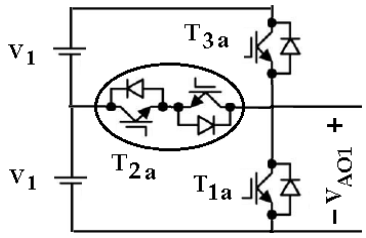


FIGURE 2. Basic unit.

In the proposed multilevel inverter, in three-phase, the number of switches (N_{sw}), driver circuits (N_{driv}) and DC voltage sources (N_S) is calculated as:

$$N_{sw} = 9n \tag{2}$$

$$N_{driv} = 9n \tag{3}$$

$$N_S = 6n - 4 \tag{4}$$

The bidirectional switches include two IGBTs or MOSFETs with two anti-parallel power diodes [15]. The cost of the switch depends on its voltage rating. In the proposed basic unit, the voltage stress of bidirectional switches is half of the voltage stress of unidirectional switches and the voltage stress of IGBTs or MOSFETs in bidirectional switches is equal to a quarter of the IGBTs or MOSFETs of unidirectional switches. One driver circuit is used in the bidirectional switch if a switch with a common emitter configuration is used. Therefore, the number of driver circuits for the bidirectional switches is the same as that of the unidirectional switches in the basic unit.

The proposed converter acts as symmetric and asymmetric multilevel inverter. In the following, two methods are introduced for determining the amplitude of the DC voltage sources, which are synthesized in the proposed topology.

In the symmetric topology, the magnitude of all DC voltage sources is equal [7]. The maximum number of levels (m_{ph}) of the phase voltage is given by:

$$m_{ph} = 2n + 1 \tag{5}$$

The maximum number of levels (m_{LL}) of the phase to phase voltage is given by:

$$m_{LL} = 4n + 1 \tag{6}$$

Let $V_1 = V_2 = ... = V_n = \frac{V_{dc}}{2}$. Then, the maximum output positive voltage of each phase is:

$$V_{AO\max} = nV_{dc} \tag{7}$$

In the proposed symmetric multilevel inverter, the voltage stress of bidirectional (VS_{bisw}) and unidirectional switches (VS_{unisw}) is calculated as follows:

$$VS_{bisw} = \frac{V_{dc}}{2} \tag{8}$$

$$VS_{unisw} = V_{dc} \tag{9}$$

In this part, the working principle of the proposed converter is explained with the help of the inverter that is shown Figure 3. Figure 3 shows the proposed converter that comprises two units in any phase.

Table 1 shows the ON switches look-up table of the 5-level proposed converter. In this study, $V_1=V_2=V_{dc}/2$. To obtain any desired voltage level, two switches need to be ON simultaneously as observed from Table 1. The structure and operation of other phases is the same as phase A. The only differences are the phase angles of the switching signals. In this work, the fundamental frequency switching technique has been used [16]. Figure 4 shows the operation of the symmetric proposed multilevel inverter. This structure generates five voltage levels in the output phase. Figure 4(a) shows the output voltage of the units. Each unit generates a quasi-square waveform. Figure 4(b) reveals the phase output voltages (V_{ph}). Figure 4(c) shows the phase to phase voltage. This voltage has nine levels. The voltages of switches are shown in Figure 5. These figures verify (8) and (9). The *dv/dt* of switches in units is half of the DC voltage of each unit.

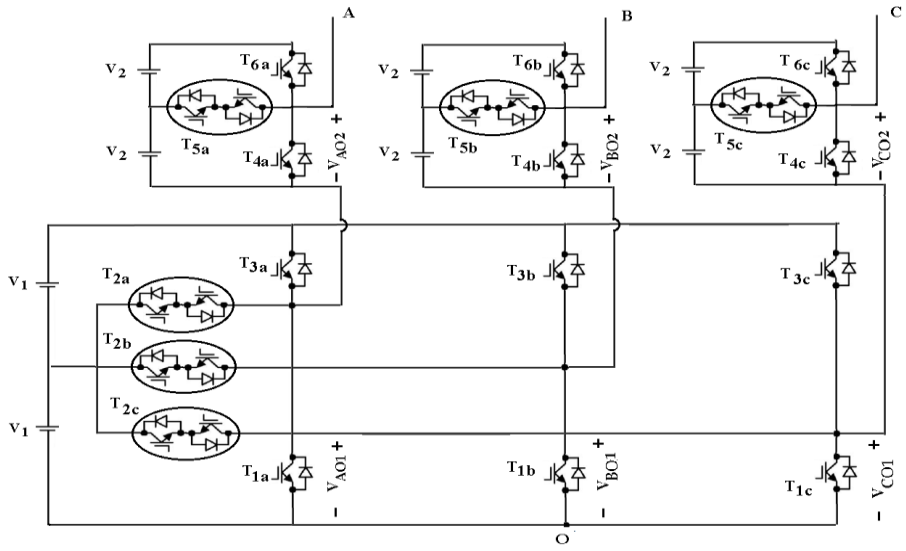
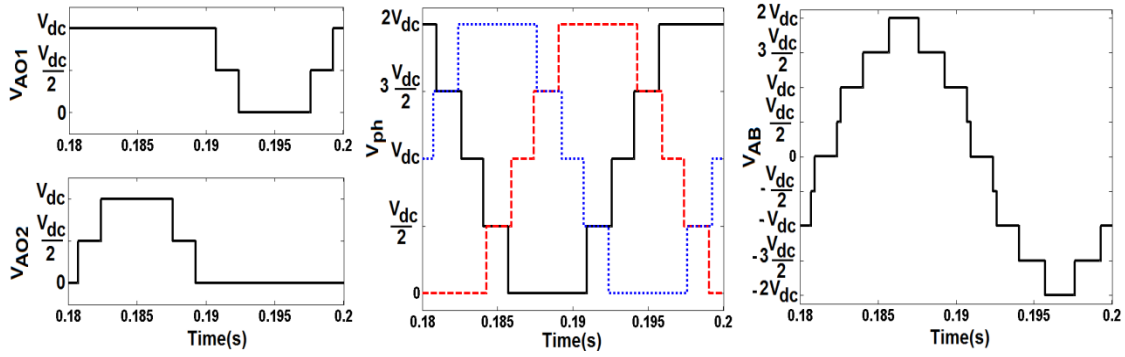


FIGURE 3. Proposed converter with two units in any phase.

Table 1: Look-up table of the 5-level inverter.

Level	0	$\frac{V_{dc}}{2}$	V_{dc}	$3\frac{V_{dc}}{2}$	$2V_{dc}$
ON switches	T_{1a}, T_{4a}	T_{2a}, T_{4a}	T_{3a}, T_{4a}	T_{3a}, T_{5a}	T_{3a}, T_{6a}

Let V_1=V_2=20 V. Figure 6 illustrates the harmonic content of the phase to phase voltage of the symmetric inverter. For this case, the THD value of the symmetric inverter is measured as 11.19%.



(a) (b) (c)

FIGURE 4. Operation of the multilevel inverter in symmetric state (a) output voltage of the units (b) phase voltages (c) phase to phase voltage.

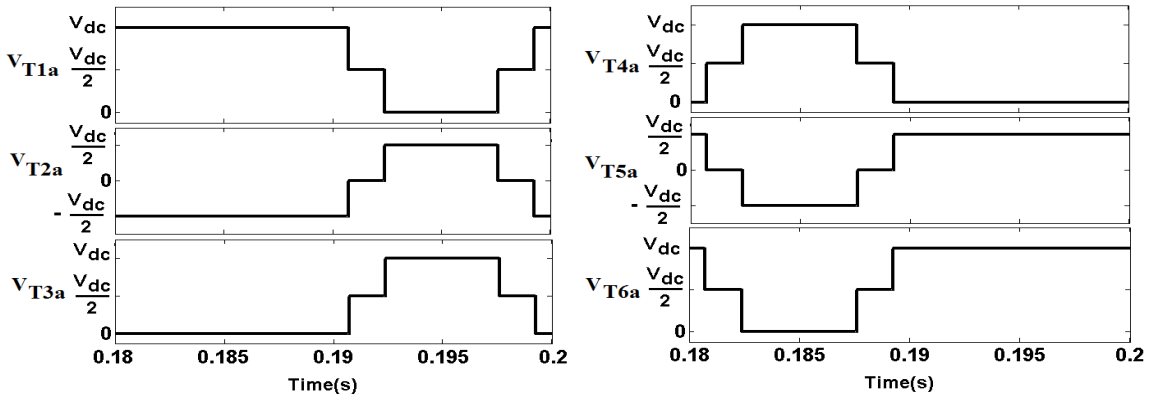


FIGURE 5. The switch voltages.

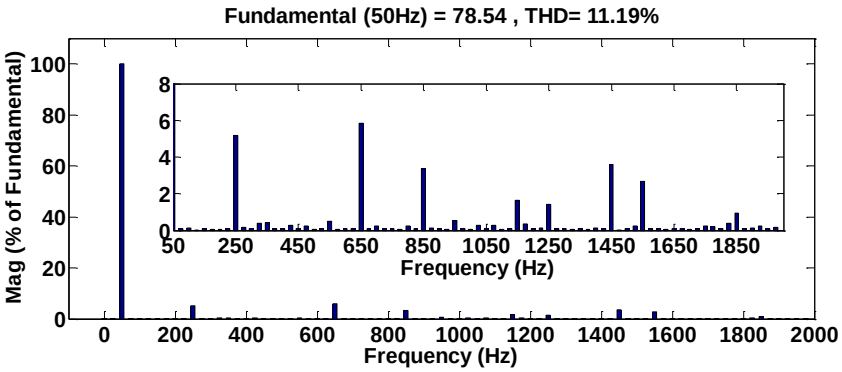


FIGURE 6. Harmonic content of the proposed symmetric inverter.

The asymmetric topology produces higher voltage levels than the symmetric topology while they have same number of components in their structures [11-13]. In asymmetric topologies, determining the value of the DC voltage sources has the most consequential influence in increasing the number of generated output voltage levels.

In the proposed topology, different algorithms to determine the value of the used DC voltage sources can be proposed. In the following, one method for determining the values of the DC voltage sources which is used in the proposed multilevel inverter is analyzed.

The second method for determining the values of the DC voltage sources is the trinary method. The values of the DC sources in each basic unit are calculated as:

$$V_i = 3^{(i-1)}\frac{V_{dc}}{2} \qquad i = 1,2,...,n \qquad (10)$$

The number of phase and phase to phase voltage levels is given by:

$$m_{ph} = 3^n \qquad (11)$$

$$m_{LL} = 2*3^n - 1 \qquad (12)$$

The maximum output voltage of each phase is:

$$V_{AO\max} = \frac{(3^{(n-1)}-1)}{2}V_{dc} \qquad (13)$$

The voltage stress of the switches in different units is given as:

$$VS_{bisw,i} = V_i \qquad i = 1,2,...,n \qquad (14)$$

$$VS_{unisw,i} = 2V_i \qquad i = 1,2,...,n \qquad (15)$$

To study the asymmetric multilevel inverter, let $V_1=V_{dc}/2$ and $V_2=3V_{dc}/2$. Table 2 shows the ON switches look-up table of the 9-level asymmetric proposed inverter.

Table 2: Look-up table of the 9-level converter.

Level	0	$\frac{V_{dc}}{2}$	V_{dc}	$3\frac{V_{dc}}{2}$	$2V_{dc}$	$5\frac{V_{dc}}{2}$	$3V_{dc}$	$7\frac{V_{dc}}{2}$	$4V_{dc}$
ON switches	T_{1a}, T_{4a}	T_{2a}, T_{4a}	T_{3a}, T_{4a}	T_{1a}, T_{5a}	T_{2a}, T_{5a}	T_{3a}, T_{5a}	T_{1a}, T_{6a}	T_{2a}, T_{6a}	T_{3a}, T_{6a}

Figure 7 shows the operation of the proposed multilevel inverter in the asymmetric state. This structure generates nine voltage levels in the output phase and seventeen levels in the output phase to phase. The switch voltages are shown in Figure 8. These figures verify (14) and (15). Let V_1=10 V and V_2=30 V. The harmonic content of V_{AB} is shown in Figure 9 that features a 6.78% THD close to that obtained in the simulation.

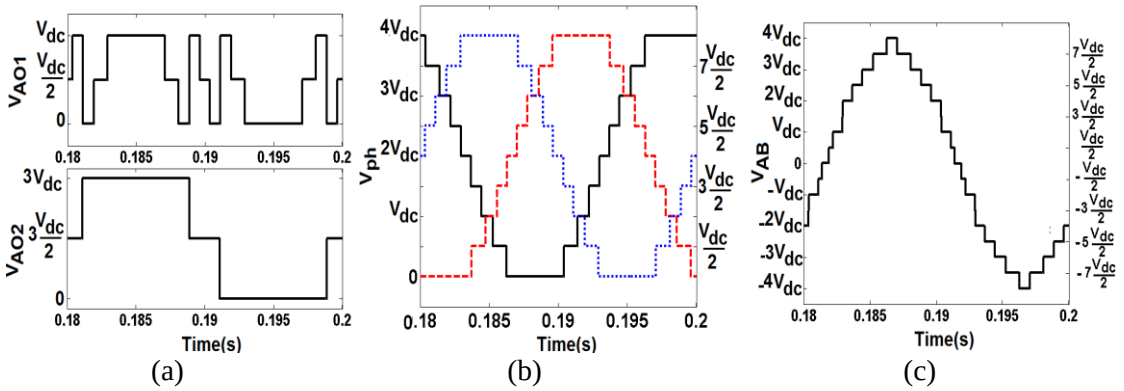


Figure 7. Operation of the multilevel inverter in the asymmetric state (a) output voltage of the units (b) phase voltages (c) phase to phase voltage.

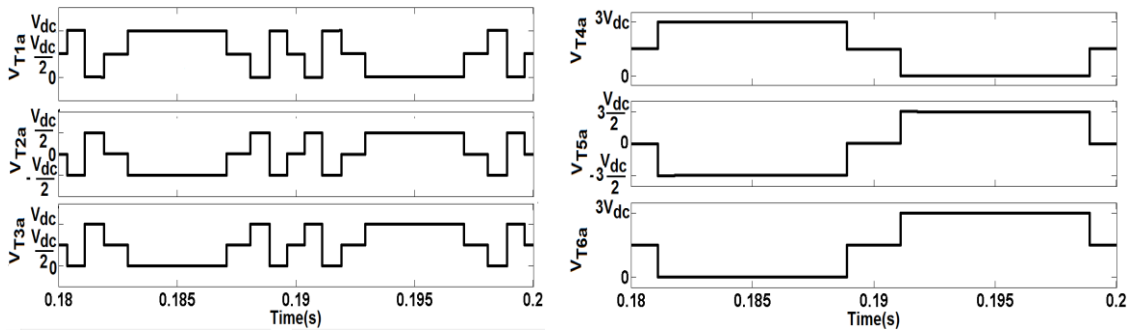


FIGURE 8. The switch voltages.

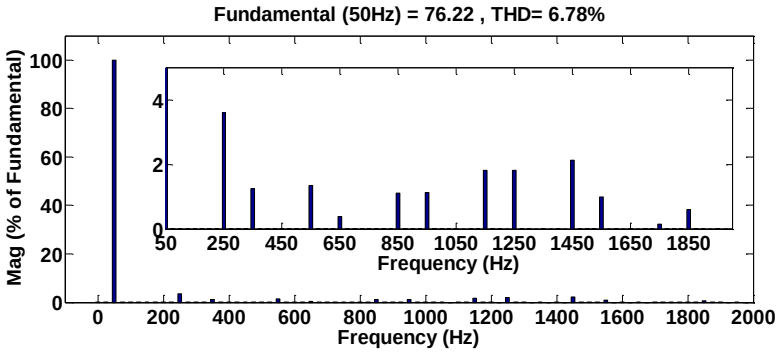


FIGURE 9. Harmonic content of the proposed symmetric inverter.

The proposed topology requires multiple DC voltage sources and this is main disadvantage of the proposed topology. However, in energy conversion, it may be attainable such as power conversion of photovoltaic system or fuel cells [18]. In order to reduce the number of DC voltage sources in the proposed structure, two DC voltage sources in each unit can be replaced by one DC voltage source and two capacitors. Figure 10 shows the proposed topology that uses voltage divider capacitors.

The main aim of introducing the multilevel inverter is increasing the number of output voltage levels while using fewer power electronic components. A reduction of the power electronic devices such as semiconductor switches (IGBTs or MOSFETs) reduces the number of driver and protection circuits. Figure 11 shows a comparison between the proposed inverter, CHB and the proposed inverter in [7] in the symmetric state. The proposed converter needs fewer switches than CHB but the number of switches is higher than that of the proposed inverter in [7] at a large number of voltage levels. Another important problem in inverters is the ratings of semiconductor switches. In other word, switches with high voltage and current ratings have a higher cost than switches with low voltage and current ratings. For the proposed topology with voltage divider capacitors, the number of DC voltage sources is calculated as:

$$N_S = 3n - 2 \tag{16}$$

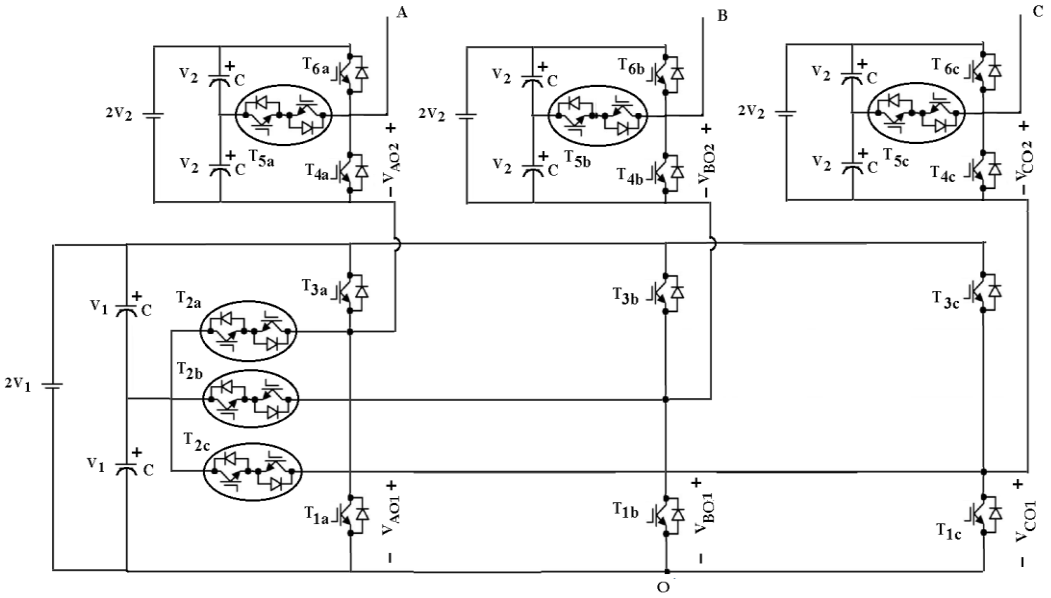


FIGURE 10. Proposed topology with voltage divider capacitors.

3. Comparison

In the proposed topology and cascaded topologies, the currents of switches is equal to the rated current of the load. This is, however, not the case for the voltage. In [7-11], new topologies for multilevel inverters are proposed that consists of a basic unit and a full bridge converter. The switches of the full bridge converter in these topologies have high voltage stress while the proposed structure does not have switches with high voltage stress. In fact, these topologies do not have the main advantages of multilevel inverters. The voltage stress of switches in the proposed topology has been shown in (8), (9), (14) and (15). In [19] and [20] two symmetrical and asymmetrical topologies are presented. Summary descriptions of selected topologies are shown in Table 3. In the Table 3, *n* is number of DC voltage sources. Figure 8 defines the proposed topology for multilevel inverter in [20]. Although this topology uses unidirectional switches and reduces the number of switches in comparison with CHB multilevel inverter, some switches (H_1, H_2, H_4 and H_5) in this topology have high voltage stress.

Figure 12 compares the number of power electronic switches in the proposed multilevel inverter based on its proposed algorithms with the proposed cascaded inverter in [7]. This figure is given for a three-phase system. The proposed cascaded inverter in [7] in the best state operates in a binary system. The proposed converter generates higher voltage levels than the proposed inverter in [7] by using the same number of switches in asymmetric states. The number of voltage levels in [20] is the same as in [7] in the asymmetric state. The proposed

converter in [12] generates fifteen levels by using twelve switches in the asymmetric state in one phase. It is seen that the device count is significantly reduced for the proposed topology in asymmetric state.

Table 3: Descriptions of the selected topologies for comparison.

Number of	Symmetric of [19]	Asymmetric of [19]	Symmetric of [20]	Asymmetric of [7, 20]
Voltage levels	$2n+1$	$3n+1$	$2n+1$	$2^{n+1}-1$
switches	$(2n+4)$	$(2n+4)$	$(2n+2)$	$(2n+4)$
on state switches	$(n+1)$	$(n+1)$	$(n+2)$	$(n+2)$

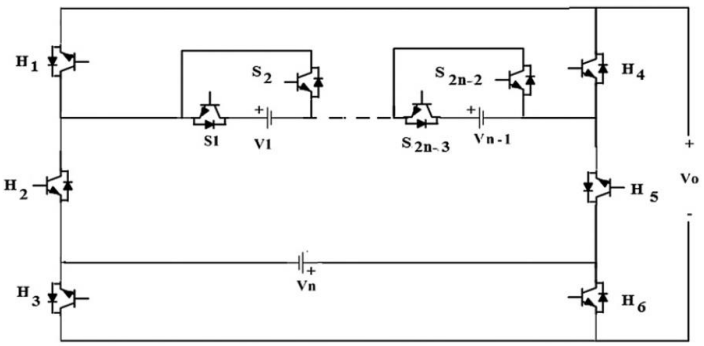
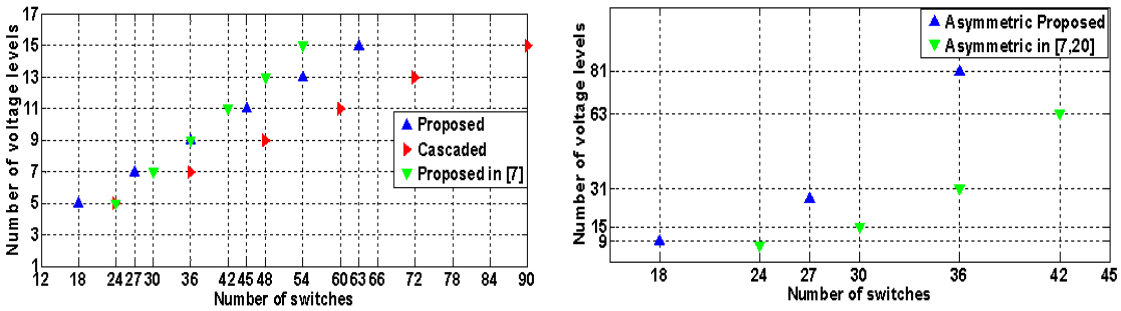


FIGURE 11. The proposed topology for the multilevel inverter in [20].



(a) (b)

FIGURE 12. Compares the number of power electronic switches in the proposed multilevel inverter and the cascaded inverter in [7] (a) symmetric state and (b) asymmetric state.

Another problem in the multilevel inverters is the on-state voltage drop of switches. In CHB, for a *n* cascaded unit, 2*n* switches need to conduct simultaneously to obtain any output level. In the proposed topology, however, only *n* switches need to conduct to obtain a given level. The on-state voltage drop affects the conduction losses [17]. The energy losses depend on the voltage that the switch needs to block. To calculate the total losses, a typical switch is first considered, and individual losses are then added to obtain the total losses of the inverter. Reduction of the number of switches and using switches with low stress voltage reduces losses of inverters.

4. Experimental Results

In this section, the presentation of the proposed multilevel inverter is proven by using the lab prototype results of five and nine level inverters. The proposed topology consists of two series connected basic units in each phase as shown in Figure 3. A prototype of the proposed topology is implemented according to one shown in Figure 13.

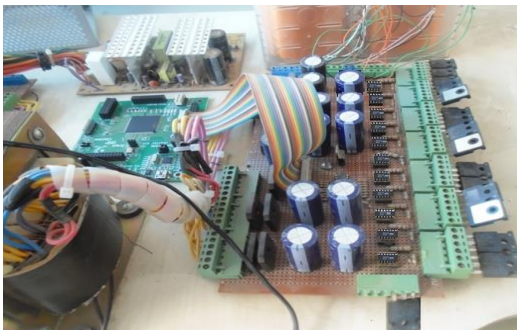


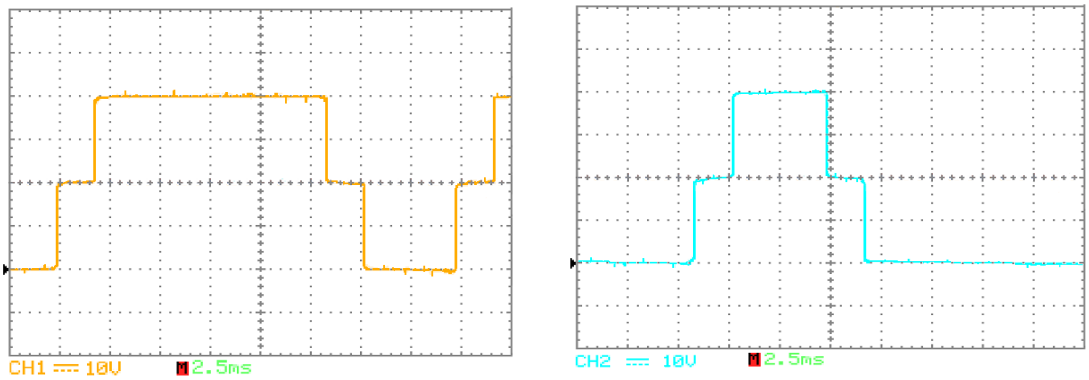
Figure 13. A prototype of the proposed topology.

The prototype inverter was built using BUP403 (600 V, 42A) IGBTs as switching devices and IRS2113 as IGBT driver. The DSPSM320F28335 is used as microcontroller. Multi winding transformer and diode rectifiers create the power supply of switches. The diode rectifiers are GBU-808. The load is an RL load (R=55 Ω and L=72 mH).

4.1. Symmetric State

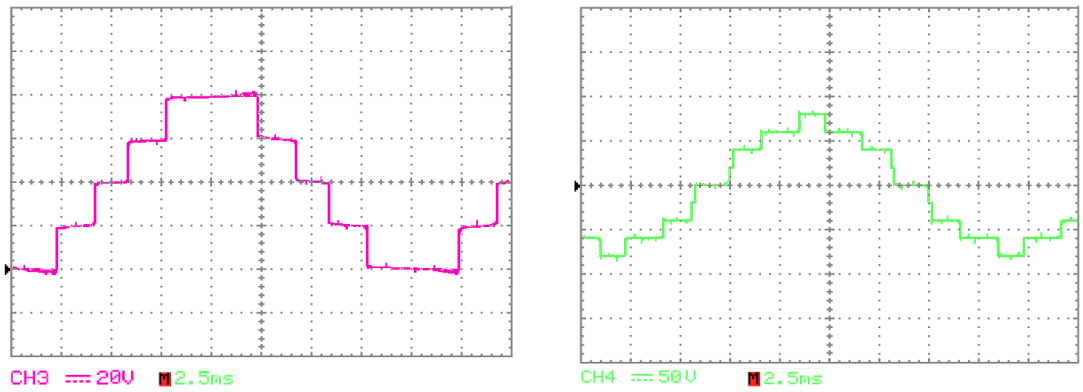
In the symmetric state, the magnitude of the DC voltage sources is 20 V. The proposed inverter is able to generate five levels with the maximum amplitude of 80 *V* at the output. Figure 14 and 15 shows the measured output voltage. The look-up table of the 5-level proposed converter has been shown in Table 1. Figure 14 shows the voltage of the basic units. These voltages are three level voltages. Figure 15(a) shows the phase voltages. The phase to

phase voltage (V_{AB}) is shown in Figure 15(b). The harmonic content of V_{AB} is the same as in Figure 6.



(a) (b)

FIGURE 14. Voltage of the basic units (a) V_{AO1} (b) V_{AO2}.



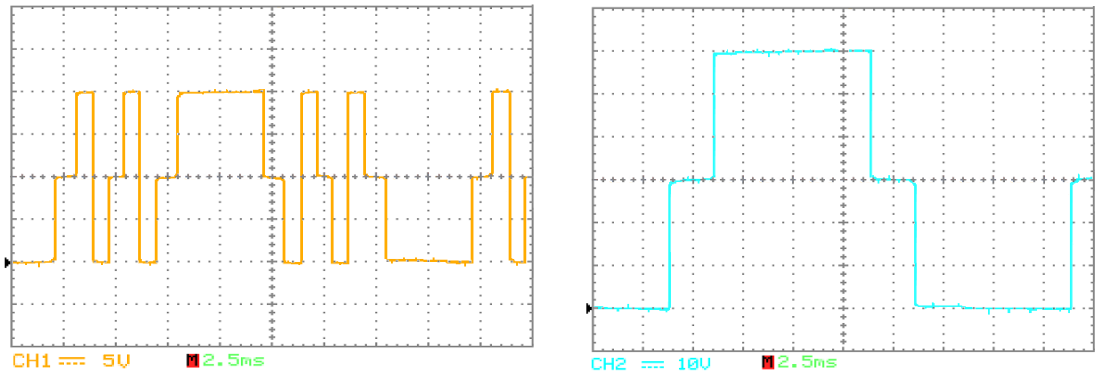
(a) (b)

FIGURE 15. Measured output voltages in the symmetric state (a) phase voltages (b) phase to phase voltage (V_{AB}).

4.2. Asymmetric State

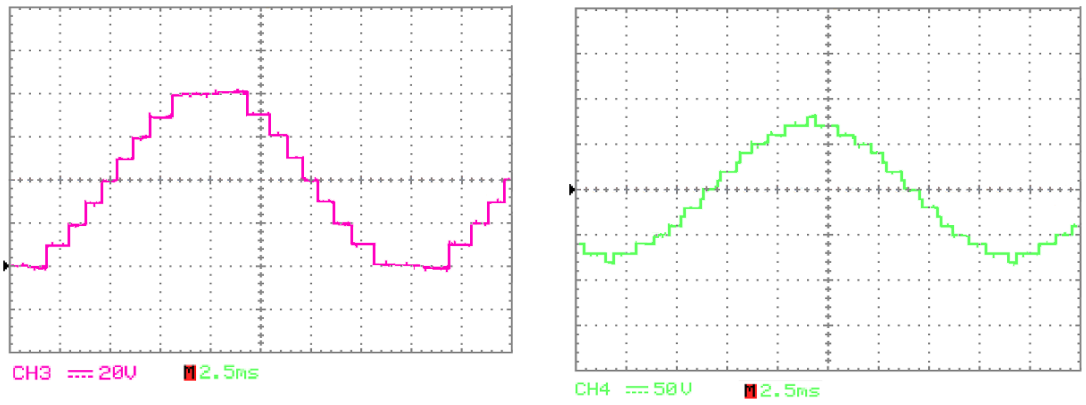
The magnitude of its DC voltage sources are determined by using the proposed algorithm in the asymmetric state. The value of the used DC voltage sources in the first unit is considered as 10 V and in the second unit will be 30 V. Figure 16 shows the output voltage of the basic units. The values of the maximum voltage of the basic units are not equal. Figure 17(a) shows the output phase voltage that is the sum of the basic units' voltage. The phase to phase voltage

is shown in Figure 17(b). The phase to phase voltage (V_{AB}) has seventeen levels. The harmonic content of V_{AB} is the same as in Figure 9.



(a) (b)

FIGURE 16. Voltage of the basic units (a) V_{AO1} (b) V_{AO2}.



(a) (b)

FIGURE 17. Measured output voltages in the asymmetric state (a) phase voltages (b) phase to phase voltage (V_{AB}).

5. Conclusions

In this paper, a new and innovative symmetric and asymmetric topology is proposed for multilevel inverters. A reduced number of switches and gate driver circuits is the main feature of the proposed topology. The operation of the proposed inverter is the same as the conventional three-level inverter. The proposed converter creates a staircase voltage. Two different algorithms to determine the magnitude of the DC voltage sources are proposed in

symmetric and asymmetric states. Comparisons among CHB, the proposed inverter and some of the novel topologies show the significant advantages of the proposed topology. The symmetric 5-level and asymmetric 9-level topologies based on the proposed topology are simulated in the MATLAB/SIMULINK software and implemented experimentally to confirm the high performance of the proposed topologies.

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