Research Article GU J Sci, Part A, 11(1): 137-146 (2024) 10.54287/gujsa.1413932

Gazi University
Journal of Science
PART A: ENGINEERING AND INNOVATION
http://dergipark.org.tr/gujsa

Analysis of Current-Voltage Properties of Al/p-si Schottky Diode with Aluminium Oxide Layer

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Keywords

Schottky Diode
Current-Voltage
Ideality Factor
Barrier Height
Atomic Layer Deposition

Abstract

In our study, the effects of the metal oxide (aluminum oxide, Al_2O_3) thin film placed between the metal and the semiconductor on the diode's characteristics were investigated. The Al_2O_3 thin film was suitable for its growth on a p-type silicon substrate by the atomic layer deposition (ALD) technique. In this study, a diode structure with an oxide interlayer was fabricated. To investigate the electrical parameters of the fabricated Schottky diode, measurements of current-voltage (I-V) were carried out at room temperature and in the 5 V voltage range. Using the I-V measurements, diode parameters such as the barrier height (Φb), the ideality factor (n), and the current density (I0) were evaluated using the theory of thermionic emission (TE) and Cheung's method. Using the TE method and Cheung's method, the approximate values of Φb, n parameters were calculated as 0.77 eV, 5.43, and 0.77 Ev, 5.97, respectively. According to calculations, the developed Schottky diode is a rectifier diode and has been determined to have photodiode properties. This research offers an understanding of the production and electrical characteristics of Schottky devices based on Al_2O_3.

Cite

Dikicioğlu, E., & Polat, B. (2024). Analysis of Current-Voltage Properties of Al/p-si Schottky Diode with Aluminium Oxide Layer. *GU J Sci, Part A, 11* (1), 137-146. doi:10.54287/gujsa.1413932

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Article Process

Submission Date 03.01.2024
Revision Date 18.01.2024
Accepted Date 09.02.2024
Published Date 19.02.2024

1. INTRODUCTION

Schottky diodes (SDs) are one of the important topics for research based on both theoretical and experimental findings in the fields of physics and electronics. While these types of structures have an important place in revealing the measurable electrical magnitude of semiconductor technology, their usage areas are gradually increasing due to the knowledge of their distinctive features and ease of production. Metal-semiconductor (MS) contacts, also known as Schottky diodes, are also called structures that can respond to sudden transitions between the voltage drop parameters applied at high frequencies, rapid direction change, and conductivity as well as insulation properties. In other words, important features that distinguish these diodes from other structures are that they have a very fast switching ability, low series resistance, and a minimum forward voltage drop. Considering these advantages, MS contacts maintain their place as the most used contacts in the field of semiconductor technology (Buyukbas et al., 2023; Sze, 1981). Schottky diodes are used in many electronic devices today, with the development of technology. Schottky diodes have minimal forward voltage drop, low series resistance, and fast switching (Sze, 1981). Metal insulator semiconductor (MIS) structures and Metal-Oxide Semiconductor (MOS) structures are formed by placing an insulating layer between the metal and semiconductor layers using an artificial or natural oxidation method (Nicollian & Brews, 1982). The schematic view of the metal-semiconductor Schottky diode is given in Figure 1.

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MIS and MOS structures are quite similar in terms of layer structure and formation techniques. The thickness of the insulating layer at the interface separates these two similar structures. The insulating layer in MOS structures is thicker than in MIS structures (Nicollian & Brews, 1982). An insulating intermediate layer is created between the semiconductor and metal layers using a natural or artificial oxidation method. Thus, the MIS structure is obtained. The insulator in the intermediate layer between the metal and the semiconductor regulates the charge transitions between these layers over time by insulating the layers from each other (Kong et al., 2019).

Metal-oxide-semiconductor Field Effect Transistors (MOSFETs), a crucial component of integrated circuits in the contemporary electronics industry, are largely composed of MOS structures. MOSFET structures are basic electronic circuit elements that have a great impact on the development of chip and transistor technologies. Therefore, all studies on any MOS device first require an understanding of the basic operating principles of MOS structures.

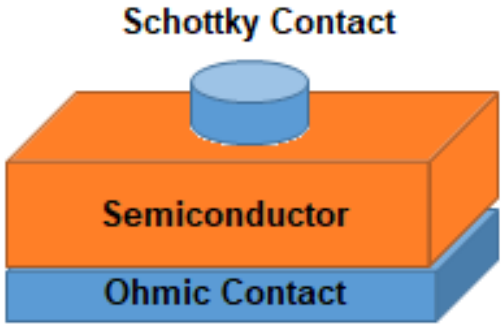

Figure 1. *Schematic view of the contacts of a metal-semiconductor Schottky diode*

Metals with work functions selected depending on the semiconductor type (p-type/n-type) are used in the preparation of MIS and MOS structures as rectifier contacts. Metals such as gold (Au), aluminum (Al), and silver (Ag) with high purity values are preferred to change the purity of the metal and make it higher. As a semiconductor, silicon (Si) material is generally preferred as it has a stable structure at high temperatures and is cheaper to manufacture. The quality of the insulating layer and the semiconductor surface placed between the M/S in MIS structures significantly affect and greatly increase the performance, reliability, and accuracy of the Schottky diode. Increasing leakage current in MIS structures may negatively affect the performance of the device. Therefore, to minimize the leakage current in these structures, the insulating interface layer is selected from materials with a high dielectric constant. MIS structures with low leakage current enable the construction of integrated electronic devices that have a fast response time, reduce power losses, and operate more stably. To reduce the amount of leakage current in MIS structures, materials with high dielectric constants such as Al_2O_3, HfO_2, and $SrTiO_3$, which have a dielectric constant higher than the dielectric constant of the SiO_2 layer, are preferred (Choi et al., 2023; Tongpeng et al., 2023; Seven et al.,2024). Since Al_2O_3 has a dielectric constant that is significantly greater than SiO_2, it has been recommended as a material that can be used as an insulating material in electronic applications as well as MOS and MIS structures. The dielectric constant of Al_2O_3 is 9.0, and the dielectric constant of SiO_2 is 3.9.

Aluminum oxide (Al_2O_3) is a compound whose chemical formula consists of Al and O atoms. Aluminum oxide is a white powder in its pure form and is a component of many minerals found in nature. The crystal structure of aluminum oxide can be found in both amorphous and crystalline forms. Its crystal structure exists in two main forms, alpha-Al_2O_3 (α) and gamma-Al_2O_3. In the α form, Al^{3+} ions are arranged in a hexagonal coating arrangement and O^{2-} ions are arranged according to this arrangement. In gamma form, they occur in cubic structures. Figure 2 shows the schematic representation of the α-Al_2O_3 hexagonal close-packed lattice structure (Troncy, 2021). Aluminum oxide has high-temperature resistance, high hardness, and chemical resistance, and thanks to these properties, it is preferred in applications such as ceramics, metallurgy, chemical industry, glass industry, catalyst, fiber composite, and electronics. Al_2O_3 has a high dielectric constant (high-k ~9), large bandgap (~7 eV), high thermal conductivity, mechanical strength, and high-temperature resistance. This means that aluminum oxide can store electric charges better. Because of these superior properties, it is a

technologically important material and one of the most studied among all oxides. Aluminum oxides are used as a suitable insulation material for MIS structures thanks to their physical and chemical properties (Troncy, 2021). For this reason, Al_2O_3 was preferred as the oxide layer in this study.

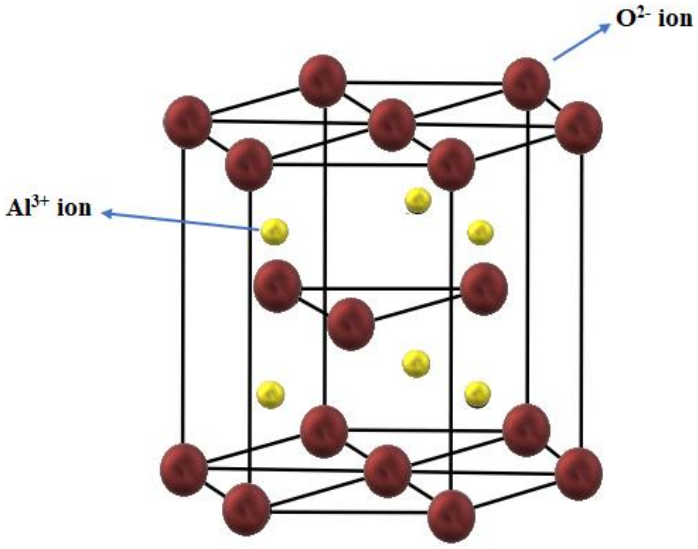

Figure 2. *α-Al_2O_3 Hexagonal Close-Packed Lattice Structure*

There are many methods to grow the Al_2O_3 insulating interfacial layer. Atomic layer deposition (ALD) is one of the most preferred methods due to the control over film homogeneity and great chemical versatility. The ALD method has been widely used recently because it is more advantageous than other growth techniques and can be controlled while growing the layer (Schilirò et al., 2023). ALD method; It is a chemical vapor coating method that provides thickness control at values below nanometers, where the chemical reactions occurring periodically on the surface are self-limiting and allow the production of films with high homogeneity at low temperatures by preventing reactions in the gas phase by separating the precursor gases (Suntola, 1992). By holding the gas phase precursors to the surface at low temperatures without reaching extremely high temperatures, the ALD process creates high-quality thin coatings. This method aims to obtain a smoother, homogeneous surface, thus minimizing the interfacial effect and obtaining an ideal structure (Ji et al., 2023). With this method, a better-quality layer can be grown and the thickness of the grown layer can be easily determined. Due to such advantages, the ALD method was preferred when growing the Al_2O_3 insulating interfacial layer.

In this study, we have produced the Al/Al_2O_3/p-type Si diode using the ALD technique. We used I-V measurements to determine the electrical parameters of this structure. In the I-V measurements, we then calculated the diode parameters such as the barrier height (Φ_b), current density (I_0), and ideality factor (n) using the TE method and the Cheung method.

2. MATERIAL AND METHOD

In this study, a p-type silicon crystal with a thickness of 380 μm, (100) surface orientation, and a resistivity of 1-10 Ω-cm, shiny on one side and matte on the other, was used. Firstly, the p-type Si substrate was purified by applying chemical purifying procedures. Then, an Al ohmic contact with a 124 nm thick high-purity was formed on the matte surface of the p-type silicon substrate to create an ohmic contact.

In the second step, a 17 nm thick Al_2O_3 as an interfacial layer was grown and deposited on the entire shiny surface of the crystal using the ALD technique. With the utilization of ALD at 170 ^{0}C which is a low substrate temperature, Al_2O_3 was deposited on the bright surface of the wafer. Al_2O_3 thin film was deposited at 170 ^{0}C using aluminum (trimethylaluminum-TMA) and oxygen (water-H_2O) precursors. Thus, a 17 nm thick Al_2O_3 thin film was obtained. Nitrogen (99.999%) was used as cleaning and carrier gas to separate the precursor cycles. Table 1 gives the recipe for the Al_2O_3 film grown on a Si substrate with ALD.

Table 1. *Al_2O_3 coating recipe on Si substrate with ALD*

Precursor	Trimethylaluminum (TMA)
H_2O pulse time (ms)	15
Purge time (ms)	10
Precursor pulse time (ms)	100
Purge time (ms)	20
Operating temperature (°C)	170
Cycles	125

After growing a 17 nm Al_2O_3 film on the p-type Silicon substrate, it was time to create Schottky contacts. In this last stage, approximately 128 nm Al metal was coated on Al_2O_3 using the Physical Vapor Deposition (PVD) technique to create a Schottky contact. The metal contacts are circular and 1.5 mm in diameter.

A depiction of the produced Al_2O_3/p-Si Schottky diode is given in Figure 3. After the calculations, it was seen that the Al_2O_3/p-Si Schottky diode has a rectifying feature. Electrical measurements were carried out to obtain the I-V characteristics of the Al/Al_2O_3/p-Si Schottky diode. The energy band diagram of the Al/Al_2O_3/p-Si Schottky diode is given in Figure 4.

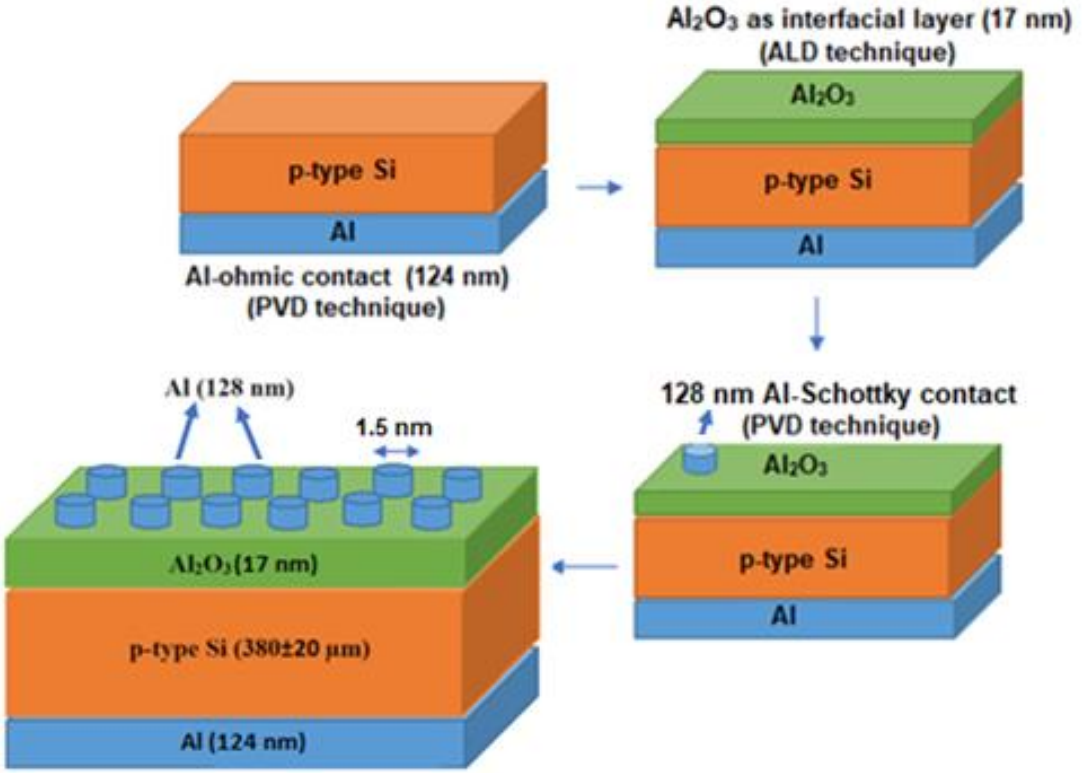

Figure 3. *Layer-by-layer view of Al/Al_2O_3/p-type Silicon diode*

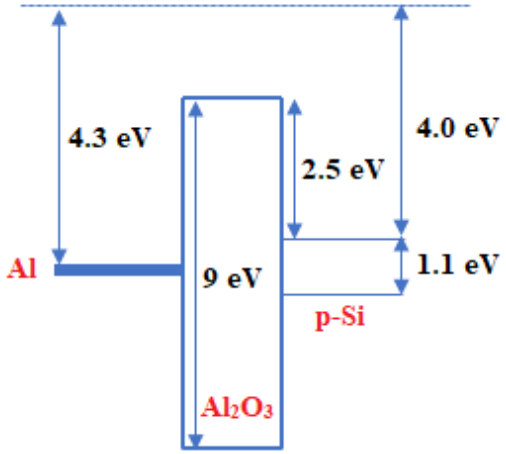

Figure 4. *Energy band diagram of Al/Al_2O_3/p-type Silicon MIS schottky diode*

3. RESULTS AND DISCUSSION

To investigate the electrical characteristics of the Al/Al_2O_3(17 nm) /p-type Si design, electrical data was gathered through I-V measurements. All measurements were carried out in a dark environment at room temperature (300 K). The current-voltage graph is presented in Figure 5.

As can be seen in Figure 5, the graph of the ln (I)-V drawn using the I-V characteristic of the Al/Al_2O_3/p-Si diode measured in the dark environment is given. When the I-V characteristics of the Al/Al_2O_3/p-Si diode in the dark are examined, it is seen that this structure has good rectification properties and exhibits a rectifying diode behavior. The rectification ratio (RR) of the diode was obtained as $1.08x10^5$. The ln(I)-V graph's upward curving at high currents is caused by series resistance's dominant effect on the current curve in the forward polarization area, which can originate from either the contact wires or the mass resistance of the MOS structures. The R_s effect and the existence of interfacial states cause the I-V curves to bend downward at sufficiently high supply voltages.

The insulating layer created naturally or artificially between the metal and semiconductor transforms this structure into a MIS structure. This insulating layer significantly affects the parameters of the I-V characteristics. A single current conduction mechanism may be effective at a certain temperature and over the entire voltage range, or two or more current conduction mechanisms may be effective at the same time (Kong et al., 2019).

TE method was used to study the electrical properties of its structure. Due to the presence of the interface layer in MOS structures, the relationship between forwarding bias voltage and current for V>3kT/q is given (Sze, 1981; Rhoderick & Williams, 1988):

$$I = I_0 \, exp\left(\frac{qV}{nkT}\right)\left[1 - exp\left(-\frac{qV}{kT}\right)\right] \tag{1}$$

In ideal Schottky diodes, unless the applied voltage is high, current conduction follows the TE model. The current expression is written as;

$$I = I_0 \, exp\left(\frac{qV}{nkT}\right) \tag{2}$$

The semi-logarithmic ln(I)-V graph's straight-line intersection at V=0 yields I_0 (the saturation current) value;

$$I_0 = AA^*T^2 \, exp\left(-\frac{q\varphi_b}{kT}\right) \tag{3}$$

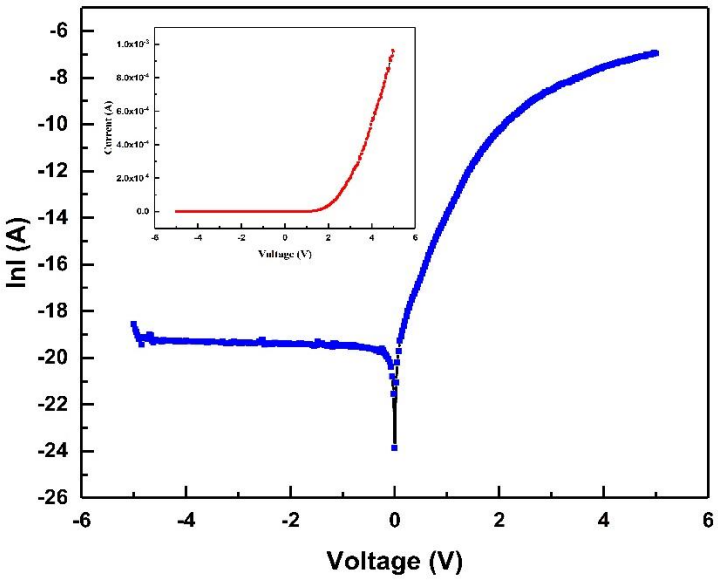

Figure 5. *Investigation of the ln(I)–V characteristics of the produced Al/Al_2O_3(17 nm) /p-type Si Schottky diodes*

Here *n* represents the ideality factor, q signifies the electronic charge, k symbolizes the Boltzmann constant, T denotes the temperature in Kelvin, I_0 represents the reverse saturation current, A* is determined as the Richardson constant (32 A/cm^{2}K^2 for p-type Si), A is known as the diode area, V represents the applied voltage and Φ_b denotes the effective barrier height.

In the graph of the ln(I)-V, it is expected to be a line. If the graph is nonlinear, the ideality factor is large, and the diode has moved away from ideality. In practice, many Schottky diodes deviate from the TE method. This non-ideal diode behavior is described by using a dimensionless parameter *n*, called the ideality factor, in the current expression. Equation (2) and the slope of the linear zone in the ln(I)-V plot can be used to calculate the ideality factor. The ideality factor is a metric frequently used to evaluate how much practical diodes deviate from the ideal TE characteristic (Sze, 1981).

$$n = \frac{q}{kT}\frac{dV}{d(ln\, I)} \tag{4}$$

Φ_b can be derived from Eq. (5) as are given by

$$\varphi_b = \frac{kT}{q} ln\left(\frac{AA^*T^2}{I_0}\right) \tag{5}$$

The Φ_b value was calculated from the intersection points of the forward trend ln(I)-V graph at room temperature. The ideality factor, as per the TE method, ought to be 1. The ideality factor depends on the presence of an insulating layer between the metal-semiconductor, the series resistance, and the distribution of the interfacial density of states (N_{ss}) in the forbidden energy band gap (Kong et al., 2019). The ideal situation where n = 1 has not been encountered. Because the applied voltage affects the obstacle height to some extent. The reason for this effect is the natural formation of an insulating oxide layer approximately 5–20 Å thick at the metal-semiconductor interface, even in near-ideal Schottky diodes (Kong et al., 2019).

The method developed by N.W Cheung and S.K. Cheung was used to calculate the values of *n*, Φ_b, and *Rs* (Wang, 2004). Cheung's model is applied to the non-linear high-voltage area of the forward bias of the I-V graphs (Cheung & Cheung, 1986). Based on this approach, *n*, Φ_b. R_s, and H(I) can be expressed as

$$\frac{dV}{d(\ln I)} = n\frac{kT}{q} + IR_s \tag{6}$$

$$H(I) = V - \frac{nkT}{q} ln\left(\frac{I}{AA^*T^2}\right) \tag{7}$$

$$H(I) = n\varphi_b + IR_s \tag{8}$$

The Φ_b was determined from the linear section of the forward bias I-V curve. Figure 6 displays the H(I) vs I and dV/dlnI vs I graphs for an Al/Al_2O_3/p-type Si diode at 300 K.

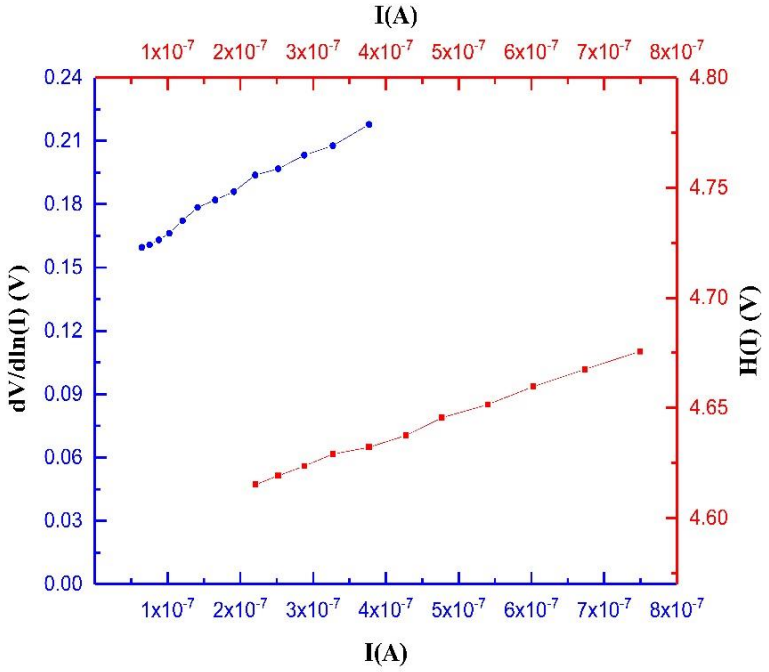

Figure 6. *H(I) vs I and dV/d(ln I) vs. I characteristics of produced Al/Al_2O_3 /p-type Si Schottky diode*

The graph of dV/d(ln I) versus I is a straight line with a slope of R_s and an intercept of nkT/q on the y-axis. This is because Eq. (6) results in a linear relationship in the lower left curvature region of the forward bias I-V characteristics. The R_s value is calculated from the gradient of the dV/d(ln I) vs. I curve, while *n* is determined from the intersection point of the curve. In Eq. (8), the value of R_s is determined from the gradient of the H(I) vs I curve, and the value of Φ_b is obtained from the point where the curve is cut off, using the *n* value calculated in Eq. (6).

As seen in this figure, the semi-logarithmic ln(I)-V slope can be obtained by extrapolating the straight line and this can be used to extract the ideality factor of the diode design. Φ_b, I_0, and *n* values gained from current-voltage measurements over the Al/Al_2O_3/p type Si Schottky diode are shown in Table 2.

Table 2. *Diode parameters of Al/Al_2O_3/p-Si Schottky structure*

Methods		n	Φ_b (eV)	R_s (kΩ)	I_0 (A)	RR
Standard (TE) Method		5.43	0.77	-	2.43E-09	$1.08x10^5$
Cheung	dV/dlnI vs I	5.97	-	186.11		
	H(I) vs I	-	0.77	114.20		

In this study, *n* and Φ_b were determined from forward I–V features using the TE method and Cheung method. From the flat supply I-V graphs of the produced diode structure, *n* values were calculated as 5.43 and 5.97,

and Φ_b values were calculated as 0.77 eV and 0.77 eV, respectively, using the TE method and Cheung methods. Regarding the Al/Al_2O_3/p-Si Schottky diode structure, we can say that although its rectification feature is good, it exhibits a non-ideal diode behavior due to its high ideality factor. The n value of the TE theory is close to the n value of the Cheung method, as shown in Table 1. The diode's non-ideal behavior (n>1) indicated the existence of interfacial states. The reason why the values of the ideality factor are greater than unity is due to series resistance, interface impurities, barrier inhomogeneity, and interface states. Because of the dispersion of the interface states at the interface and the existence of an insulating interface layer between the metal and semiconductor, the computed n value is greater than 1 (Singh, 1985; Szatkowski & Sierański, 1988). The Φ_b values for both methods are consistent with each other for the diode. We have presented in Table 3 the diode properties of different Schottky diodes with Al_2O_3 interlayers created by other researchers at 300 K, coated with different coating methods and with different thicknesses, to compare them with our current work.

Table 3. *Comparison of diode parameters for various types of Schottky diodes with Al_2O_3 interlayer*

Diodes	Interlayer Coating Methods	n	Φ_b (eV)	RR	References
Al/Al_2O_3 (17 nm)/*p-Si*	ALD	5.43 (TE) 5.97 (Cheung)	0.77 0.77	$1.08x10^5$	Present work
Al/Gr/Al_2O_3 (17 nm)/p-Si	RF magnetron sputtering	3.89 (TE) 5.54 (Cheung)	0.69 0.68	10^3	(Efil et al., 2020)
Au/ Al_2O_3 (30 nm)/*p*-Si/Al	Spin coating	1.59	0.91	3.58×10^4	(Deniz et al., 2022)
Al/ Al_2O_3 (2.5 nm)/p-Si	ALD	3.014 (TE) 3.44 (Cheung)	0.75 0.97	-	(Yıldız & Cavuş, 2016)
Al/ Al_2O_3 (4 nm)/p-Si	ALD	1.82	0.50	$4.74x10^4$	(Kosal et al., 2019)
Au/Al_2O_3(50 nm)/n-Si	RF magnetron sputtering	1.23	0.77	-	(Eymur &Tuğluoğlu, 2021)

As indicated in Table 3, variations in the technique and thickness employed to form the interface layer in the measurements impacted the *n* and Φ_b values. When the study of Efil et al. (17 nm Al_2O_3) and our study (17 nm Al_2O_3) are compared, it is seen that graphene improves the n value. It is thought that the coating method (RF magnetron sputtering) also affects this change. The reasons for the high ideality factor values in our study are interface impurities, series resistance, interface states, and barrier inhomogeneity. When Φ_b values are compared with all coating methods, it can be seen that they are almost compatible with each other. The RR value is higher than structures coated with RF magnetron sputtering and spin coating.

4. CONCLUSION

At room temperature and in the dark, we examined the I-V characteristics of the Al /Al_2O_3 (17 nm) /p-type Si structure. The standard TE method and Cheung's method were used to measure and assess the electrical characteristics of this semiconductor, including the ideality factor and barrier height. The electrical properties that belong to the Al/Al_2O_3/p-Si diode are very sensitive to voltage. The electrical characteristics of the structure are crucial for accurately and consistently evaluating the interface states. Using the TE method and Cheung's method, the approximate values of Φ_b, *n* parameters were calculated as 0.77 eV, 5.43, and 0.77 Ev, 5.97 respectively. The deviation of the ideality factor value from the ideal was attributed to the Al_2O_3 insulating layer between the semiconductor/metal and the special distribution of interfacial states. In practice, for an ideal situation, n =1. However, since the applied voltage affects the obstacle height to some extent, this situation has rarely been encountered in the literature. The reason for this effect is the natural formation of a thin oxide layer with a thickness of at least 5-20 Å at the metal-semiconductor interface, even in Schottky diodes that are closest to ideal. The deviation of the obstacle height from the ideal situation resulting from its dependence on the applied voltage is expressed as $1/n=1-(\delta\Phi_b/\delta V)$. Since some of the applied voltage falls on the diode and some on the oxide layer, the barrier height becomes a function of the applied voltage. Another reason why the ideal factor is greater than 1 is that the series resistance value is large. Due to the voltage drop across the insulating

layer, the voltage across the diode decreases. This decrease in voltage causes the current-voltage characteristics to deviate from the ideal situation. In summary, the reasons for the high ideality factor values in our study are interface impurities, series resistance, interface states, and barrier inhomogeneity. This research offers an understanding of the production and electrical characteristics of Schottky devices based on Al_2O_3.

As a result, many studies have been carried out by preparing various insulation layers for the metal-semiconductor interface, and various models have been developed. Al_2O_3 shows advantages over SiO_2 and SnO_2, which have been widely used in micro-electronics to date, and thus allows the production of higher quality, longer lasting, and faster Schottky structures, transistors, and integrated circuits. Therefore, it is expected that studies on the production of various dielectric and oxide films with high dielectric coefficients using the atomic layer deposition technique will remain current and important in the coming years. In future studies, the thickness of Al_2O_3 can be changed in a way that will positively affect the electrical properties of Al_2O_3 and coating can be done with different methods as alternatives to the ALD method. Additionally, the effects can be examined by applying different types and ratios of coating on the Al_2O_3 layer. According to the findings, it was observed that the thickness of the Al_2O_3 structure and the coating method significantly affected the ideality factor, series resistance, and barrier height properties.

AUTHOR CONTRIBUTIONS

Methodology and writing-reviewing, E.D., B.P.; editing, E.D.; conceptualization and software, E.D., B.P. All authors have read and legally accepted the final version of the article published in the journal.

CONFLICT OF INTEREST

The authors declare no conflict of interest.

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