The Eurasia Proceedings of Science, Technology, Engineering & Mathematics (EPSTEM)
ISSN: 2602-3199

The Eurasia Proceedings of Science, Technology, Engineering & Mathematics (EPSTEM)

Volume 1, Pages 69-75

ICONTES2017: International Conference on Technology, Engineering and Science

DETERMINATION THE EFFECTS OF DUTY CYCLE AND SWITCHING FREQUENCY ON EFFICIENCY OF BOOST CONVERTER FOR FIXED LOAD APPLICATIONS

Enis Baris Bulut
Trakya University

Korhan Cengiz
Trakya University

Abstract: Recent years, power converters have been a significant part of daily applications such as PV systems, wind turbines, electrical vehicle chargers and adapters. Due to the arising energy demand and the energy restrictions of the environment, energy efficiency of power converters become crucial. Energy efficiency of these converters can be enhanced using appropriate converter topology, effective modeling and control algorithms. Therefore, in this study, we aim to model and analyze the power losses of boost converter to determine best usage interval in terms of duty cycle and switching frequency. The proposed model is designed by using Simulink and the results in terms of efficiency and power losses are obtained and analyzed in MATLAB. The results of this study demonstrate that, appropriate selection of duty cycle and switching frequency provide lower power losses and thus higher efficiencies.

Keywords: Power converters, boost converter, power loss model, converter efficiency

Introduction

As an expected result of technological improvements and electricity dependent lifestyles, energy demand of the world is increasing rapidly. Using our limited energy sources efficiently and increasing the efficiency of electrical devices are two of the most important topics of electrical and electronics engineering. Power converters are a part of these devices that needs improvement in efficiency manner. Power electronic circuits, in other words "power converters" are widely used in industrial and daily life. Power converters are circuits that used for converting voltage and current waveforms, frequencies and amplitudes to demanded waveforms and values. These converters are being used in numerous areas such as mobile chargers, electrical vehicles, renewable power plants, SMPS circuits and motor drives. Mathematically modelling those converters may help us to understand their dynamics and working principles [1]. With accurate models, it will be easier to produce efficient converters and save energy. Also, as those devices being used in mobile devices such as electrical vehicles and drones, smaller size and lower weight converters can be designed with the help of increased efficiency values [2].

In this study, Boost (Step-up) type DC/DC power converter have been selected to mathematically model its power loss characteristics. The main reason of selection of the boost converter is that those converters have been widely used in renewable power plants and demand for that type of converter increases day-by-day. As photovoltaic panels produces low voltages, before supplying a load or connecting to grid, it has to be stepped-up. Also, same situation is also occurring in wind turbines, which also produces varying voltages according to wind speed. So, after rectification of wind turbines output voltage, generally a boost converter circuit is used for boosting voltages to demanded values. To understand efficiency mechanisms of boost converters, a mathematical power loss model of mentioned converter have been derived with the help of previous studies [1,3-8]. According to these power loss model and calculations, it is aimed to understand efficiency mechanism of boost converter, to be able to use those converters in their most efficient working intervals. In this study, these

- Selection and peer-review under responsibility of the Organizing Committee of the conference

*Corresponding author: Enis Baris Bulut- E-mail: ebarisbulut@trakya.edu.tr

efficiency intervals have been calculated with respect to switching frequency and duty cycle. To obtain the mathematical results of derived model, MATLAB/Simulink software have been used. Converters electrical model designed in Simulink. Then, needed instantaneous, average and RMS values of currents/voltages have been taken to MATLAB editor part. Lastly, developed power loss calculation algorithm have been used to determine power loss characteristics of the DC/DC boost converter.

Briefly, in first step, mathematical power loss model of boost converter have been derived. In second step, computer based simulations and calculations of mentioned model have been done. In the last step, according to obtained results, efficiency map of boost type DC/DC converter have been obtained.

Boost Converter Topology

DC/DC Boost Converters are be using for increasing the voltage value [2]. Although there are numerous boost converter topologies, in this study, traditional DC/DC Boost Converter have been used to derive power loss model and efficiency analysis (Figure 1).

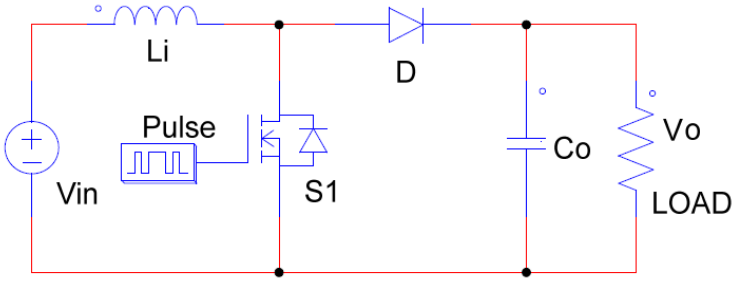

Figure 1. Ideal DC/DC boost converter

In this converter topology, semiconductor switch S1 is closed (conducting) for charging the inductor (Li) for D*Ts time, where D stands for the Duty Ratio of gating pulse and Ts stands for switching period of the switch S1. On the other step of boosting operation, for (1-D)*Ts time, switch S1 is opened (not conducting) to allow charged inductor (Li) to supply voltage to load-side. After necessary mathematical derivations, voltage gain function of boost converter can be obtained as stated in (1).

$$V_o = \frac{V_i}{1-D} \tag{1}$$

Where V_o is the output voltage and V_i is the input voltage of the boost converter.

As can be understood from the equation 1, boosting ability of a DC/DC boost converter is a function of Duty Ratio (D) and also this ability is increasing with the increase of D. A typical voltage gain function of a non-ideal traditional boost converter can be seen in Figure 2.

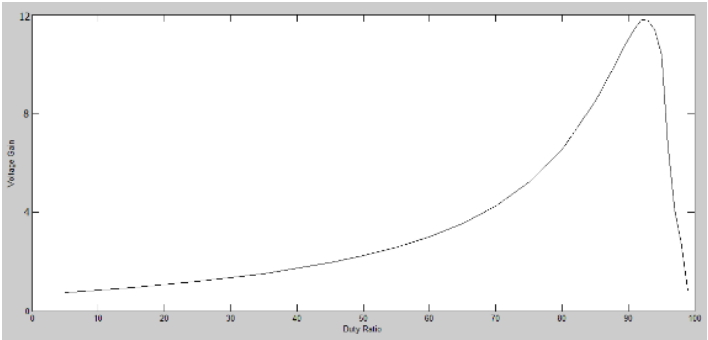

Figure 2. Voltage gain of a non-ideal DC/DC boost converter

Mathematical Model

Power losses of a boost converter circuit can be concluded in three main parts such as fixed losses, conduction losses and dynamic losses [1]. Fixed losses are the losses that are caused by the controller circuitry of boost converter. So, fixed losses are not dependent on element or working interval selection of the converter. As these losses are negligibly low and not caused by the working strategy of boost converter, they will be neglected in

propose mathematical power loss model. In Figure 1, the ideal boost converter topology have been given. However, for mathematical power loss model, all imperfections must be included in simulation environment. In Figure 3, non-ideal boost converter topology can be seen. Following mathematical derivations will be done according to variable names stated in Figure 3, for the sake of simplicity.

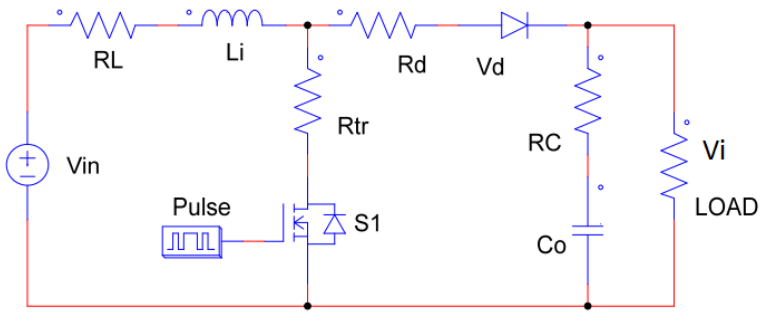

Figure 3. Non-ideal circuit model of a DC/DC boost converter (with only inner resistances)

Conduction losses are mainly caused by inner resistances of the elements and voltage drops on them. In a typical boost converter, there are four imperfect elements that have internal resistances and parasitic capacitances, which cause additional conduction and switching losses. Due to the skin effect, inner resistances of elements can be change with respect to changing switching frequencies. However, this change is small enough to be neglected and due to that reason those changes are neglected in this mathematical model.

Firstly, as an inductor is a wire that enwrapped over a ferrite core, that wire certainly has an inner resistance. From the Ohm's Law, power loss on inductor will be:

$$PL_{cond} = (IL_{rms})^2 * R_L \quad (2)$$

Where R_L is the inner resistance of inductor and IL_{rms} is the RMS value of the current passing through inductor.

Also, output capacitor has ESR (Series Resistance), too. According to Ohm's Law:

$$PC_{cond} = (IC_{rms})^2 * R_C \quad (3)$$

Where R_C is the internal series resistance of capacitor and IC_{rms} is the RMS value of the current passing through capacitor.

Semiconductor switches are also has an on-state resistance. This resistance will also obey the Ohm's Law and the conduction loss of semiconductor switch will be:

$$Ptr_{cond} = (Itr_{rms})^2 * R_{tr} \quad (4)$$

Where R_{tr} is the on-state resistance of transistor and Itr_{rms} is the RMS value of the current passing through transistor.

Lastly, the diode has also an on-state resistance as a semiconductor device. However, contrary to previous ones, the diode have to be modelled with a reversely connected voltage source and a series resistance due to its chemical properties. In (5), on-state resistance caused power loss equation has been given and in (6), voltage drop based power loss has been given.

$$Pd_{cond} = (Id_{rms})^2 * R_d \quad (5)$$

$$Pd_{drop} = (Id_{ave}) * V_d \quad (6)$$

Where V_d stands for voltage drop on diode and R_d stands for on-state resistance of diode.

Briefly, all conduction losses can be concluded [1]:

$$P_{cond} = PL_{cond} + PC_{cond} + Ptr_{cond} + Pd_{cond} + Pd_{drop} \quad (7)$$

Last and most complicated power loss type is the dynamic losses, which caused by switching characteristics of the converter. These losses are mainly caused by transistor, diode and ferrite core of the inductor. For the sake of accuracy and simplicity, ferrite core losses (P_{core}) is calculated with a function that derived according to product datasheet graphs [9].

Dynamic loss equations of transistor and diode are the main part of dynamic loss model. Gate loss is caused by equivalent input capacitance of FET (Field Effect Transistor) [3, 5].

$$P_{iss} = C_{iss} * V_{cg}^2 * f_{sw} \quad (8)$$

Where C_{iss} is input capacitance, V_{cg} is gate drive voltage and f_{sw} is switching frequency of FET.

Output capacitance of FET is also causes a type of dynamic loss.

$$P_{oss} = 0.5 * C_{oss} * V_{tr}^2 * f_{sw} \quad (9)$$

Where C_{oss} stands for output capacitance and V_{tr} for output/input voltage in continuous current/discontinuous current mode. As this study only includes continuous current mode working interval, following simulation calculations will only include continuous current values of those equation.

In transition process of non-ideal semiconductor switches, contrary to ideal ones, both voltage and current become exist on transistor for a very short time interval. However, when switching frequency increases, overall value of this loss is also increases. In a previous study [6], a function with a "k" constant (between 0.17 and 0.5) have been derived to calculate those losses.

$$P_{Tsw} = \mathrm{k} * (t_r * IL_{max} + t_f * IL_{min}) * V_o * f_{sw} \quad (10)$$

Where t_r is rising time and t_f is falling time of FET device that taken from the manufacturers datasheet. Also IL_{min} and IL_{max} are the minimum and maximum values of inductor currents.

Lastly, transition losses occurring on diode can be calculated with following equation [2]:

$$P_{Dsw} = V_o * (t_{rr} * IL_{min} + Q_r) * f_{sw} \quad (11)$$

Where t_{rr} is reverse recovery time and Q_r is reverse recovery charge of the diode.

In a nutshell, all dynamic losses of a boost converter can be concluded in one equation:

$$P_{dyn} = P_{core} + P_{iss} + P_{oss} + P_{Tsw} + P_{Dsw} \quad (12)$$

Considering all derivations above, total power loss of a boost converter can be calculated with equation (13) which is:

$$P_{total} = P_{cond} + P_{dyn} \quad (13)$$

Simulation Model

Boost converters are highly dynamic circuit topologies. As can be understood from above mentioned power loss equations, instantaneous values of some currents and voltages are needed for an accurate calculation. For that reason, MATLAB/Simulink software simulation and calculation environment have been selected for modelling. In Simulink part of software, a boost converter have been designed. To be able to calculate power losses accurately, in MATLAB editor part, a calculation algorithm written. With taking instantaneous values from Simulink environment to developed script, simulation results have been obtained. Simulation model of the boost converter can be seen in Figure 4.

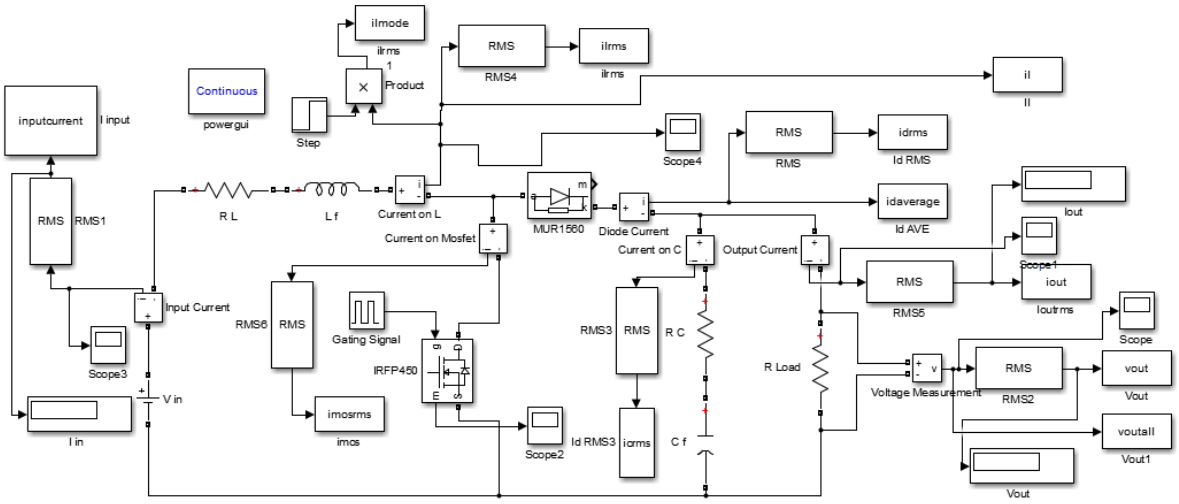

Figure 4. Designed simulation circuit and data collection mechanisms

Circuit parameters have been determined according to datasheet values of the selected components. As transistor, a new generation GaN based Field Effect Transistor from Transphorm Semiconductors have been selected [10]. As diode, MUR1460 have been used and capacitor/inductor values have been calculated to limit output voltage ripple under 5%. Simulation results have been obtained under fixed resistive load condition, selected as 100 Ω. Simulation frequencies selected as 20kHz, 40kHz, 60kHz, 80kHz and 100kHz. For all of these mentioned frequencies, simulations have been done for 0.4, 0.45, 0.50, 0.55, 0.6, 0.65, 0.7, 0.75 and 0.8 duty ratios. All results have been taken in CCM (Continuous Current Mode).

Results

Efficiency values obtained with simulations shown below in Figure 5 and output voltage ripple percentages also shown in Figure 6, as those two parameters are important ones when designing a dc/dc boost converter.

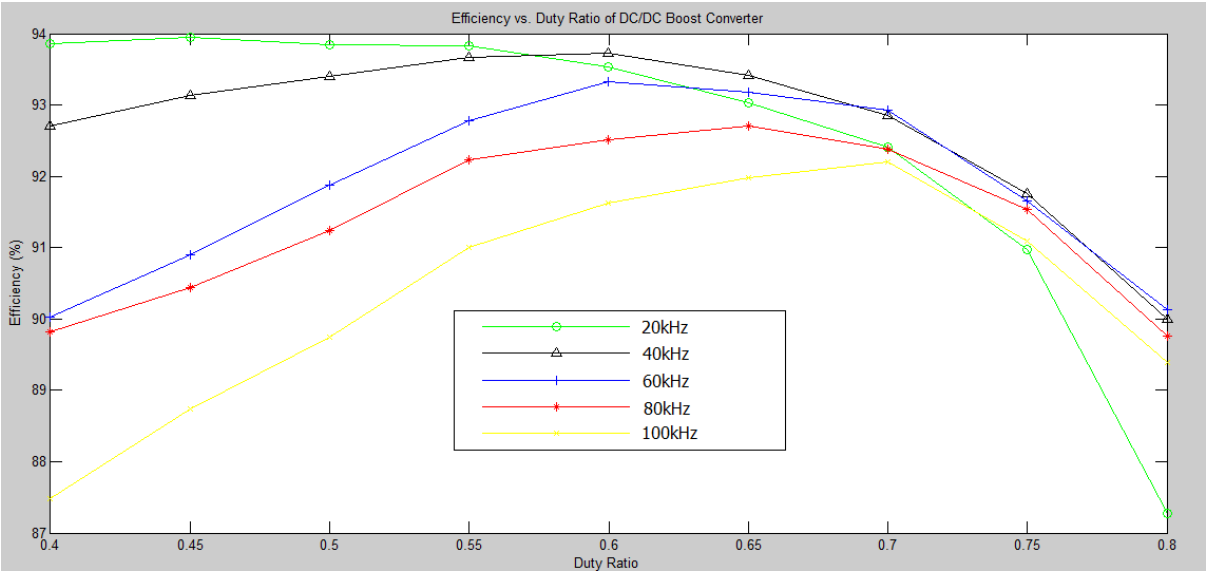

Figure 5. Efficiency vs. duty ratio graph of boost converter with respect to switching frequency

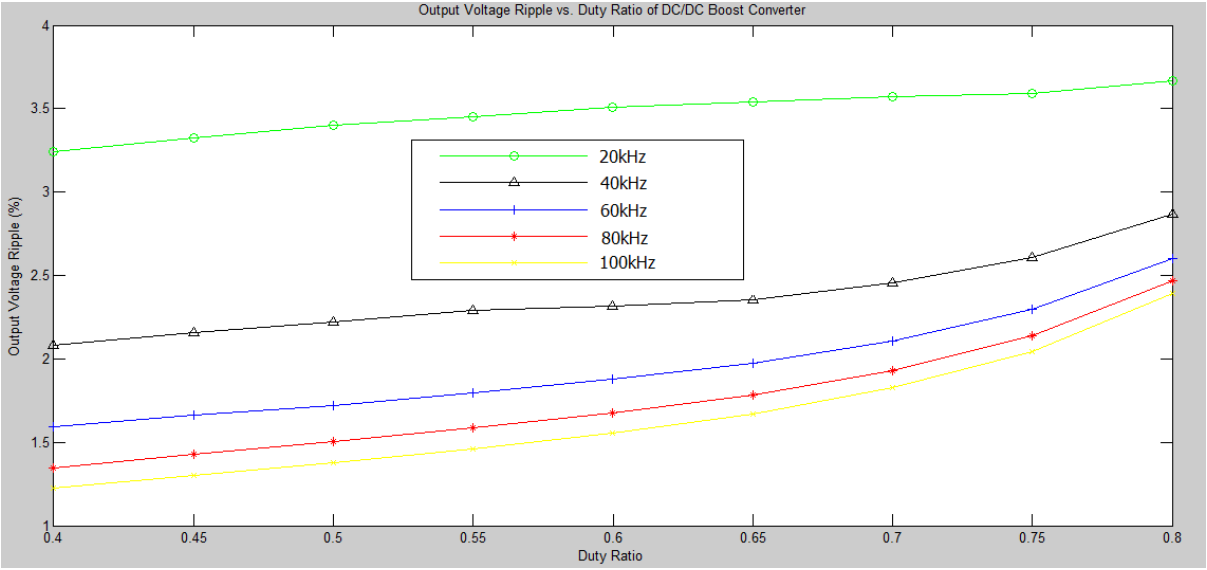

Figure 6. Voltage ripple vs. duty ratio graph of boost converter with respect to switching frequency

With proper reactive element selection (L_i & C_o), output voltage ripple is kept under %5 percent. As can be understood from Figure 6, increasing the switching frequency results in a decrease in output voltage ripple percentage, which is always a demand for converter circuits, to keep load safe. Also, with increasing duty ratio (increasing current), output voltage ripple is also increasing.

According to obtained simulation results, it is seen that dynamic losses are increasing very slowly with the increase of duty ratio. However, as load is fixed in impedance manner, increasing duty ratios also increase the output and input currents. As mathematically proved in previous sections, this increase in current values directly effects the conduction losses. Also, as can be seen from the Figure 5, maximum efficiency at 20 kHz switching frequency is obtained with 0.45 duty ratio. At higher switching frequencies, this duty ratio value shifted to higher duty ratios, which is 0.7 at 100 kHz. This is a result of the relationship between dynamic and conduction losses.

When considering all of the obtained results, it can be said that in CCM working interval, a boost converters' maximum efficiency point tends to shift through the higher duty ratios with the increase of switching frequency.

Conclusion

In this study, a mathematical power loss model derived for a DC/DC boost converter, with the help of several experimentally proven studies. Then, obtained mathematical model transferred to MATLAB simulation environment with a proper circuit model. According to simulation results, it is shown that the efficiency of a DC/DC boost converter, which is working in CCM and under fixed resistive load condition, have tend to shift through the higher duty ratios with increasing switching frequency. In a nutshell, this study showed that the proper duty ratio/switching frequency selection may cause almost 7% of efficiency change in a DC/DC boost converter.

Recommendations

To improve the results and accuracy of proposed mathematical and simulation models, DCM interval analysis may also be considered in following studies. Lastly, as a future work, simulation results will be compared with experimentally designed boost converter, to increase the accuracy of proposed power loss model.

References

Ivanovic Z., Blanusa B., Knezic M. (2011), Power loss model for efficiency improvement of boost converter, *XXII International Symposium on Information, Communication and Automation Technologies*, Sarajevo, Bosnia and Herzegovina

Erickson R. W., Maksimovic D. (2001). *Fundamentals of Power Electronics-Second Edition*, University of Colorado, Boulder, Publisher: Kluwer Academic Publishers

Rodriguez et al. (2010). Insight Into the Switching Process of Power Mosfets: An Improved Analytical Losses Model, *IEEE Transactions on Power Electronics*, 25/6, 1626-1640.

Ren Y., Xu M., Zhou J., Lee F. C. (2006). Analytical Loss Model of Power Mosfets, *IEEE Transactions on Power Electronics*, 21/2, 310-319

Aloisi W., Palumbo G. (2005). Efficiency Model of Boost DC-DC PWM Converters, *International Journal of Circuit Theory and Applications*, 33, 419-432

Wilson Eberle (2008). *Mosfet Current Source Gate Drivers, Switching Loss Modelling and Frequency Dithering Control for MHz Switching Frequency DC-DC Converters*, PhD, Queen's University Kingston, Ontario, Canada

Ivanovic Z., Dokic B., Blanusa B., Knezic M. (2010). Boost Converter Efficiency Optimization in Wind Turbine, *14th International Power Electronics and Motion Control Conference EPE-PEMC*, Ohrid, Macedonia

Van den Boosche A., Valchev V. C. (2006), Modelling Ferrite Core Losses in Power Electronics, *International Review of Electrical Engineering*

Ferroxcube, ETD 49/25/16 ETD Cores and Accessories, Datasheet, Retrieved on July 2017

Transphorm Semiconductors, TPH3206PSB, Datasheet, Retrieved on July 2017