Fırat Üniversitesi Deneysel ve Hesaplamalı Mühendislik Dergisi

FUJECE

Modüler Çok Seviyeli Dönüştürücü Topolojisi İçin En Yakın Seviye Modülasyon Yönteminin FPGA Tabanlı Dijital Kontrol Şemasının Tasarımı ve Deneysel Doğrulaması

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Öz

Modüler çok seviyeli dönüştürücü (MÇD), en yakın seviye modülasyonu (ESM) tekniğinin çoğunlukla MÇD'nin kol gerilimlerini kontrol etmek için kullanıldığı endüstriyel uygulamalar için tercih edilen bir devre topolojisi haline gelmiştir. ESM yönteminin MÇD topolojisi üzerinde dijital kontrol teknikleri kullanılarak uygulanması; esnek tasarım, tam kontrol edilebilirlik, yeniden yapılandırılabilir özellik ve modüler gerçekleştirme nedeniyle araştırmacılar arasında önem kazanmaktadır. Bu amaca ulaşmak için yüksek hız performansı ve paralel işlem yapabilme gibi avantajları sayesinde alanda programlanabilir kapı dizileri (FPGA'lar) kullanılmaktadır. Buna göre, bu makalede, tek fazlı beş seviyeli MÇD topolojisi için ESM yönteminin FPGA tabanlı kontrol şeması önerilmiştir. Bu bağlamda, çok yüksek hızlı tümleşik devre donanım tanımlama dili (VHDL) modülleri, uygulamada kullanılan her bir VHDL modülü ve algoritması sunularak ESM yönteminin önerilen mimari tasarımını gerçekleştirmek için tasarlanmıştır. ESM yönteminin FPGA'da gerçekleştirilmesinin mimari adımları ayrıntılı olarak sunulmuştur. MÇD topolojisindeki anahtarlama elemanlarının kapı sinyalleri simülasyon ortamında gözlemlenmiştir. Son olarak, ESM yönteminin dijital kontrol şemasının uygulanabilirliğini doğrulamak için, tek fazlı beş seviyeli MÇD topolojisi kullanılarak bir deney düzeneği oluşturulmuş ve deneysel bulgular sunulmuştur. Bu çalışmada elde edilen sonuçlara göre, RL yükü kullanılarak kapı sinyalleri, kol gerilimleri ve çeşitli modülasyon indeksi değerleri için çıkış gerilimleri ile akımları içeren sonuçlar sunulmuştur.

Anahtar kelimeler: Çok seviyeli dönüştürücü, Modülasyon, Alanda programlanabilir kapı dizisi, Dijital kontrol

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Design and Experimental Validation Of FPGA Based Digital Control Scheme Of The Nearest Level Modulation Method For Modular Multilevel Converter Topology

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Abstract

Modular multilevel converter (MMC) has become a preferable circuit topology for industrial applications, where the nearest level modulation (NLM) technique is mostly used to control the arm voltages of the MMC. Implementation of the NLM method on MMC topology using digital control techniques is gaining importance among researchers because of flexible design, full controllability, re-configurable property and modular realization. In order to achieve this aim, field programmable gate arrays (FPGAs) are preferred thanks to their benefits such as high speed performance and parallel processing ability. Accordingly, in this article, FPGA based control scheme of the NLM method was proposed for single-phase five-level MMC topology. In this context, very high-speed integrated circuit hardware description language (VHDL) modules were designed to achieve the proposed architectural design of the NLM method by presenting each VHDL module and algorithm used in the implementation. The architectural steps of the FPGA realization of the NLM method were presented in detail. Gate signals of the switching devices of the MMC topology were observed in simulation environment. Finally, in order to validate the applicability of the digital control scheme of the NLM method, an experimental setup was built using single-phase five-level MMC topology and experimental findings were presented. According to the obtained results of this study, the outcomes including gate signals, arm voltages and output voltages with currents were presented for various modulation index values using the RL load.

Keywords: Multilevel converter, Modulation, Field programmable gate array, Digital control

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1. Introduction

Modular multilevel converter (MMC) is an effective converter for power electronics based industrial applications [1-2]. The primary application fields of the MMC consist of high-voltage direct current networks [3], battery systems [4], motor drive applications [5], static synchronous compensator [6], renewable energy system [7], active power filter [8] and power electronic transformer [9].

In the literature, pulse width modulation (PWM) strategies using carrier signals were employed to manage the upper and lower arm voltage of the MMC in the past decade. The most popular ones of them are phase-shifted PWM [10] and level-shifted PWM [11] including phase-disposition PWM [12], phase-opposition-disposition PWM [13] and alternative phase-opposition-disposition PWM [14]. In addition to techniques with carriers, the nearest level modulation (NLM) method is stated as carrier-less technique, which has flexible implementation and directly controls the arm voltages [15].

Recently, digital platforms instead of analog systems have been adopted by the researchers for the implementation of the NLM method because of more practical design and debugging ability. Among digital platforms, field programmable gate arrays (FPGAs) and digital signal processors (DSPs) are the attractive components to realize the NLM method [16]. Design of cascaded H-bridge multilevel inverter is presented using FPGA by implementing multiple carrier phase disposition modulation method. The developed system is confirmed by simulation and experimental findings in [17]. Reference [18] suggests a control method using Xilinx system generator by implementing the phase disposition modulation method for five-level asymmetric stacked multilevel converter. The authors in [19] develop a FPGA implementation of a real-time simulation with the help of a model design method for MMC-H-bridge DC transformer. FPGA based MMC voltage controller implementing bucket odd-even hybrid voltage sorting method using Xilinx VC709 board is reported in [20]. Research reported in [21] presents a FPGA based digital switching controllers of selective harmonic elimination and sinusoidal PWM by designing minimal hardware complexity and logic utilization for a 21-level cascaded H-bridge multilevel inverter. In the implementation process of the NLM method for MMC topology, one of the most important points is that there may be too many semiconductor devices that require to be triggered in parallel. Accordingly, several packages of DSPs are insufficient to synchronously drive too many switches. Therefore, FPGAs are incorporated into the digital control systems of the NLM method as an ideal option thanks to their parallel processing capability [22]. In this context, several publications have focused on the FPGA implementation of the NLM method for MMC topology in recent years. Digital control of the NLM method using FPGA is presented for MMC topology in [23, 24]. However, in these studies, digital implementation of the NLM method is not comprehensively discussed by presenting the each very high-speed integrated circuit hardware description language (VHDL) module and algorithm on FPGA controller platform. In this paper, FPGA based control scheme of the NLM method was proposed for single-phase five-level half-bridge submodule (HBSM) based MMC topology. The major target of this proposal was to suggest the architectural steps of the FPGA realization of the NLM method.

The structure of this article is as follows. In Section 2, MMC topology is introduced. Section 3 reports the basic properties of the NLM method. Section 4 presents the proposed architectural design of FPGA implementation of the NLM method for MMC topology. Simulation and experimental study is provided by showing the gate pulses of the switching elements and experimental findings of the MMC topology in Section 5. Section 6 concludes the presented article.

2. MMC Topology

In Figure 1, circuit configuration of the single-phase MMC is depicted. As shown, DC source is used in the left side while a resistive or resistive-inductive characterized load is attached to the right side of the MMC topology. Upper and lower arm structures are included in a phase. Identical N submodules (SMs) and arm inductances are built in each arm. Output AC phase voltage and current are symbolized with V_{AC} and i_{AC}, respectively. HBSM structure is also illustrated in Figure 1. HBSM contains two semiconductor switches as S_1 and S_2, respectively.

Each HBSM also includes a DC capacitor, which should be connected in parallel. The operation logic of HBSM is tabulated in Table 1. According to this logic operation, there are two available states as 0 and V_c. Furthermore, semiconductor devices S_1 and S_2 are operated in the opposite manner. HBSM generates V_c voltage when S_1 is in the conduction region. Contrarily, HBSM generates zero voltage when S_2 is in the conduction region. As can be understood from these definitions, HBSM is simply controlled, which makes it more preferable in the MMC based power electronics applications [25].

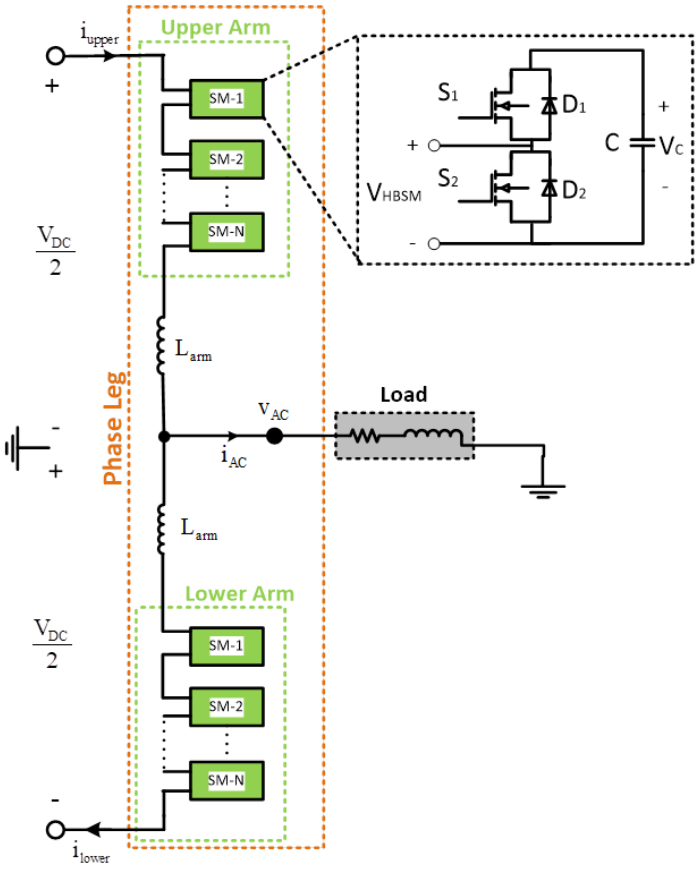


Figure 1. MMC single-phase circuit diagram including HBSM structure

Table 1. Switching states of HBSM

S_1	S_2	Arm Current	Capacitor	V_{HBSM}
1	0	Positive	Charging	V_C
1	0	Negative	Discharging	V_C
0	1	Positive	Unvaried	0
0	1	Negative	Unvaried	0

3. NLM Method

NLM is gaining more interest due to its simple implementation and it is adopted by digital controller applications of MMC to control the arm voltages of the MMC. Also, NLM method avoids the use of carrier signals. The operating principle of the NLM is depicted in Figure 2. Each arm can be effectively regulated with the help of this method.

Equivalent single-phase circuit form of the MMC is represented in Figure 3. Mathematical relations of this circuit are derived in the equations below.

Arm voltages could be computed as follows:

$$V_{upper} = \frac{V_{DC}}{2} - V_{AC} - L_{arm}\frac{di_{upper}}{dt} \quad (1a)$$

$$V_{lower} = \frac{V_{DC}}{2} + V_{AC} - L_{arm}\frac{di_{lower}}{dt} \quad (1b)$$

where L_{arm} is the arm inductance. Upper and lower arm equations are defined under steady-state condition as follows:

$$V_{upper} = \frac{V_{DC}}{2} - V_{AC} - v_L \quad (2a)$$

$$V_{lower} = \frac{V_{DC}}{2} + V_{AC} - v_L \quad (2b)$$

where v_L denotes the voltage drop on the arm inductor and it is negligible. The modulation signal could be defined as given below:

$$V_{AC} = M\frac{V_{DC}}{2}sin(\omega_0 t + \phi) \quad (3)$$

where M, ω_0 and ϕ represent the modulation ratio, angular frequency and phase angle, respectively. In this context, upper and lower arm voltages could be computed using Equation (2a), (2b) and (3) as follows:

$$V_{upper} = \frac{V_{DC}}{2} - M\frac{V_{DC}}{2}sin(\omega_0 t + \phi) \quad (4a)$$

$$V_{lower} = \frac{V_{DC}}{2} + M\frac{V_{DC}}{2}sin(\omega_0 t + \phi) \quad (4b)$$

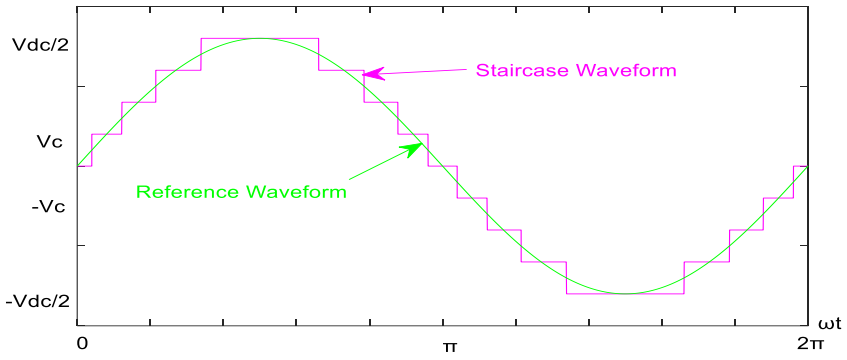


Figure 2. Main principle of the NLM method

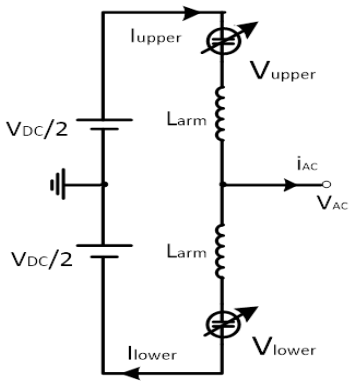


Figure 3. MMC single-phase circuit

The total DC supply voltage could be expressed with regard to the number of SMs and SM capacitor voltage as follows:

$$V_{DC} = NV_c \tag{5}$$

After substituting (5) into (4a) and (4b), the Equations are obtained as given below:

$$V_{upper} = \frac{NV_c}{2} - M\frac{NV_c}{2}sin(\omega_0 t + \phi) \tag{6a}$$
$$V_{lower} = \frac{NV_c}{2} + M\frac{NV_c}{2}sin(\omega_0 t + \phi) \tag{6b}$$

where V_c specifies the step value of the output voltage. If the Equations (6a) and (6b) are normalized, following relations are derived for arm voltages as follows:

$$V_{upper}^{n} = \frac{N}{2}[1 - M\,sin(\omega_0 t + \phi)] \tag{7a}$$
$$V_{lower}^{n} = \frac{N}{2}[1 + M\,sin(\omega_0 t + \phi)] \tag{7b}$$

4. The Proposed Architectural Design of the NLM Method

Details of the architectural design of the NLM method using FPGA are addressed in this section. VHDL is used to carry out the structural design of the method. The modules and algorithm employed in the system are explained in detail.

4.1. Sinusoidal reference creation and rounding module

Sinusoidal signal, which is employed to modulate the arms in MMC topology, is created in this module. Then, rounding function is operated to obtain the nearest voltage level from the sinusoidal reference. Initially, externally created samples of a sinusoidal reference signal with unity amplitude are kept in a look-up table (LUT). On the FPGA, LUT values are saved for subsequent use. One of the important points is to determine the modulation ratio for the generated sinusoidal reference values in the previous step. Normally, modulation index is multiplied with the sine value which is taken from LUT.

Since 10 bit string is used, modulation index (M) is considered based on 2^{10} (1024). Therefore, for the M=0.9, 92 is selected instead of 90, which results 0.89 modulation index value. According to this approach, for different M values, constant k-terms are selected. The required k-term and some of the M values are given in Table 2.

Herein, normal process is applied to multiply M with the sine value which is received from the LUT. But on an FPGA, dividing a number requires several clock cycles. Amplitude of sine signal is between -1024 and 1024. After sine signal is subtracted from 1024, it is multiplied with 2. Then, the obtained value is summed with 512 for rounding process and it is sent to upper and lower arm modules. This process is performed in each sampling period and modulation process is completed.

Table 2. The required k-terms and M values

Desired M	Actual M	k-terms	Selected k-terms
0.9	0.89	90	92
0.8	0.82	80	82
0.7	0.7	70	72
0.6	0.58	60	62

4.2. Clock divider

In digital implementation of the NLM using FPGA, special clocks are generated using the master clock of FPGA. Clock frequency of used FPGA is 100 MHz, which is also known as master clock [26]. The clock frequency can be different depending on the used FPGA card in the implementation [27]. Special clock is necessary for sinusoidal reference. The number of samples used to create the signal is included in the clock period change. In order to create other clocks from the master clock, the counter counts the number of rising edges of it up to previously determined value. When the required edge is completed, new clock is logically changed in the opposite form. Identical number of clock ticks is counted and similar procedure is continuously performed. To generate clocks for special application inside FPGA, clock of sine module is investigated. Herein, 400 samples are used to create a period of sine reference. Therefore, sampling period is computed by

$$T_{s,sine} = \frac{Period\ of\ sinusiodal\ reference}{Number\ of\ samples} = \frac{20\ ms}{400} = 0.05\ ms \tag{8}$$

The counter value can be computed using Equation (8) as stated below:

$$counter_{sine} = \frac{T_{s,sine}}{2T_{master}} = \frac{0.05\ ms}{2*10\ ns} = 2500 \tag{9}$$

Similar procedures using the Equation (8) and (9) are performed to generate clocks for special application within FPGA.

4.3. SM on and SM off nodules

The used semiconductor switches of HBSM, explained in Section 2, are triggered in the opposite manner. When S_1 and S_2 are logically 1 and 0, respectively, the SM becomes ON. Otherwise, when S_1 and S_2 are logically 0 and 1, respectively, the SM becomes OFF. In other words, while SM ON means that the output of HBSM gives the balanced capacitor voltage, SM OFF means that the output of HBSM gives zero voltage. According to this triggering information, SM ON and SM OFF modules are separately created. The details of the SM ON and SM OFF process are presented in the algorithms as given in Figure 4.

4.4. Upper and lower arm gate signal modules

Outputs of sine rounding, SM ON and SM OFF module as well as clock divider become inputs of upper and lower arm modules. Depending on the number of activated SM/SMs in each arm, gate signals of HBSMs are created. While the number of active SM/SMs is equal to N_{active} for upper arm, the number of active SM/SMs is equal to (4-N_{active}) for lower arm. Depending on the N_{active}, both upper and lower arm gate signal modules generate logic signals for semiconductors of used HBSMs in the implementation of MMC topology. Eventually, switching patterns are created for each HBSM. But, dead time module should be designed and it is required between the triggering pulses of two switching elements on any HBSM to protect from the short circuits during switching variations. For this reason, dead time module is established in the architectural design of this work.

SM ON Module Algorithm

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.NUMERIC_STD.ALL;
entity sm_on is
        Port ( clk_on : in STD_LOGIC;
      reset : in STD_LOGIC;
      S1_on : out STD_LOGIC;
      S2_on : out STD_LOGIC);
end sm_on;
architecture Behavioral of sm_on is
  signal logic_s1_on, logic_s2_on : std_logic := '0';
begin
       process(clk_on,reset,logic_s1_on,logic_s2_on)
       begin
       if reset = '1' then
          logic_s1_on <= '0';
          logic_s2_on <= '0';
       else
     if rising_edge(clk_on) then
        logic_s1_on <= '1'; --ON signals for SM (S1=1, S2=0)
       logic_s2_on <= '0';
     end if;
  end if;
      S1_on <= logic_s1_on;
      S2_on <= logic_s2_on;
  end process;
end Behavioral;
```

SM OFF Module Algorithm

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.NUMERIC_STD.ALL;
entity sm_off is
        Port ( clk_off : in STD_LOGIC;
      reset : in STD_LOGIC;
      S1_off : out STD_LOGIC;
      S2_off : out STD_LOGIC);
end sm_off;
architecture Behavioral of sm_off is
  signal logic_s1_off, logic_s2_off : std_logic := '0';
begin
       process(clk_off,reset,logic_s1_off,logic_s2_off)
       begin
       if reset = '1' then
          logic_s1_off <= '0';
          logic_s2_off <= '0';
       else
     if rising_edge(clk_off) then
logic_s1_off <= '0'; --OFF signals for SM (S1=0, S2=1)
       logic_s2_off <= '1';
     end if;
  end if;
      S1_off <= logic_s1_off;
      S2_off <= logic_s2_off;
  end process;
end Behavioral;
```

Figure 4. SM ON and SM OFF module algorithms

4.5. Dead time generator module

Since a semiconductor needs a little amount of time to be ON or OFF, it is well known that turning it on and off instantly is not practical. Hence, if no dead time is provided between the switching instants of the semiconductors on any HBSM, they can all be ON at the same time. This situation causes short circuits and extremely high currents to flow through the semiconductors, possibly damaging the HBSM. Accordingly, a dead time that is greater than the ON and OFF timings of the semiconductors should be incorporated into the switching instants of the semiconductors on the HBSM [28]. Final gate pulses of the semiconductors of HBSMs are created on the output of this module. Note that 200 ns time was selected as a dead time for triggering of the MOSFETs in this implementation.

4.6. Top module

This module combines every VHDL module. The architecture accepts the FPGA's master clock and a reset button as inputs, and it generates gate pulses for every HBMS on the upper and lower arms as the output, then, these pulses are sent to the real circuit. General architecture of the NLM method for single-phase five-

level MMC topology is illustrated in Figure 5. As seen, the top module includes the aforementioned VHDL modules.

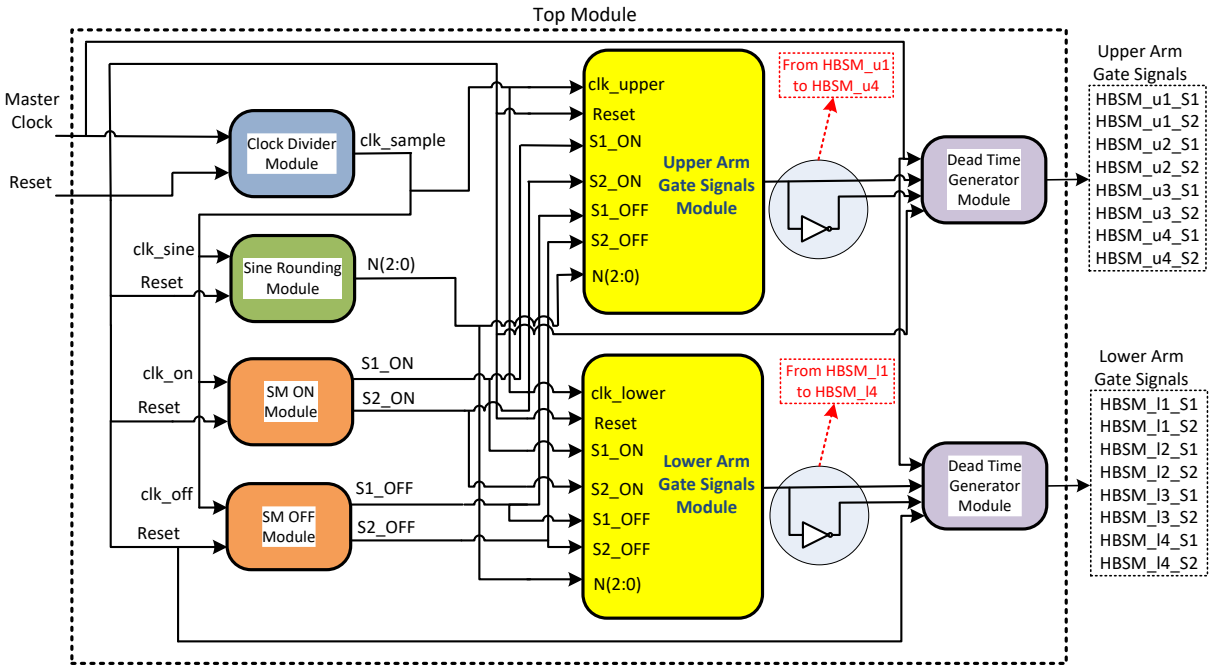


Figure 5. The proposed architectural design of the VHDL modules that creating the gate pulses of single-phase five-level MMC topology on FPGA

5. Simulation and Experimental Study

In this section, in simulation environment, the simulation results of the proposed architectural scheme using FPGA were presented to confirm the suitability of the created gate signals. The NLM method was implemented on Xilinx SPARTAN-6 FPGA controller (100 MHz master clock frequency). Xilinx ISE design computer program was utilized for the purpose of supervising and controlling the modules introduced in the previous section in real time. Table 3 demonstrates the device utilization summary of the used FPGA in the implementation by considering the number of slice registers, LUTs, used as memory and input-outputs (IOs) as performance indicators. According to the Table 3, utilization performance of resources seems satisfactory and the NLM method uses relatively few resources.

Moreover, Figure 6 shows the gate signals during a period. Four HBSM gate signals are presented for upper and lower arm, respectively. Also, clock signal and reset pulse are given. The gate signals are logically changed depending on the N value. It is clearly shown that gate signals of first and second semiconductor of any HBSM are created in the opposite manner. Although the gate signals of the semiconductors on the HBSM appear to be exact inverse of each other in Figure 6, a dead-time exists between the ON/OFF instants of the devices as explained before. A zoomed version of the dead-times between the first and second gate pulses of the HBSM is observed in Figure 7. The dead time value between S_1 and S_2 semiconductors of first HBSM of upper arm is clearly specified.

In addition, Figure 8 represents the gate signals when N value is set to 2. Herein, the gate signals remain continuously same logics since N value is constant. Again, all the gate signals of HBSMs for the arms are exhibited.

Table 3. Device utilization summary

Slice logic utilization	Utilized	Available	Utilization (%)
Number of slice registers	155	18224	1
Number of slice LUTs	250	9112	2
Number utilized as memory	7	2176	1
Number of bonded IOs	18	232	7

To verify the applicability of gate signals for the NLM method, an experimental setup was established. Table 4 describes the circuit parameters used in the MMC topology. A photograph of the experimental prototype is shown in Figure 9 and it contains the components as follows:

- FPGA controller.
- DC supplies to provide balanced capacitor voltages for the HBSMs.
- MMC SMs with gate drivers (consisting of MOSFET and gate driver) [29].
- Oscilloscope to observe the results.

Table 4. Tabulated form of experimental parameters

Item	Value
DC-link supply	40 V
Fundamental frequency	50 Hz
Number of SMs per arm	4
Arm inductor	29 mH
Balanced capacitor voltage	10 V
Load resistor	10 ohm
Load inductor	29 mH

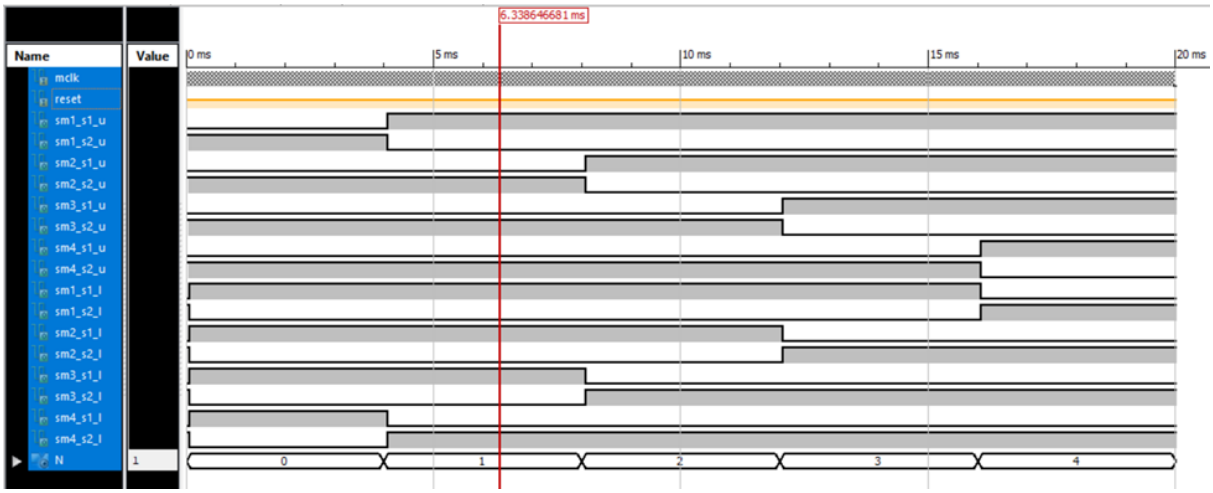


Figure 6. Gate pulses created in Xilinx program for MMC topology

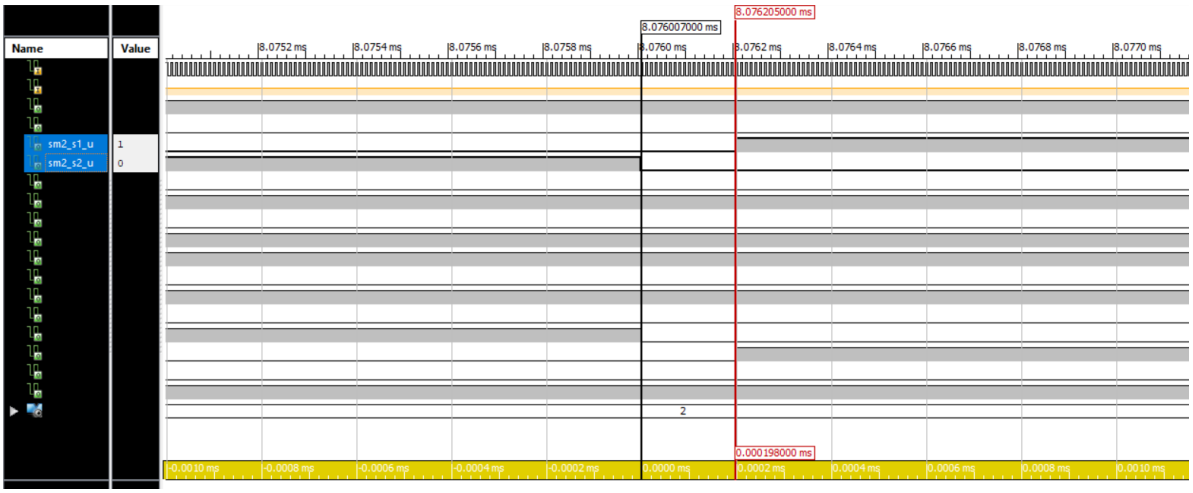


Figure 7. Dead-time between gate pulses in the upper arm

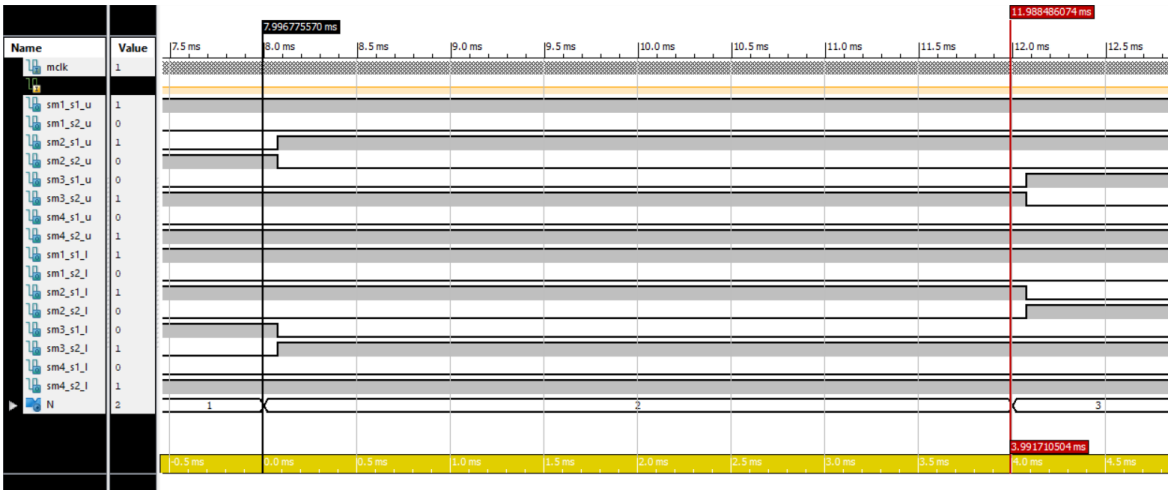


Figure 8. A view of the gate signals when N value is set to 2

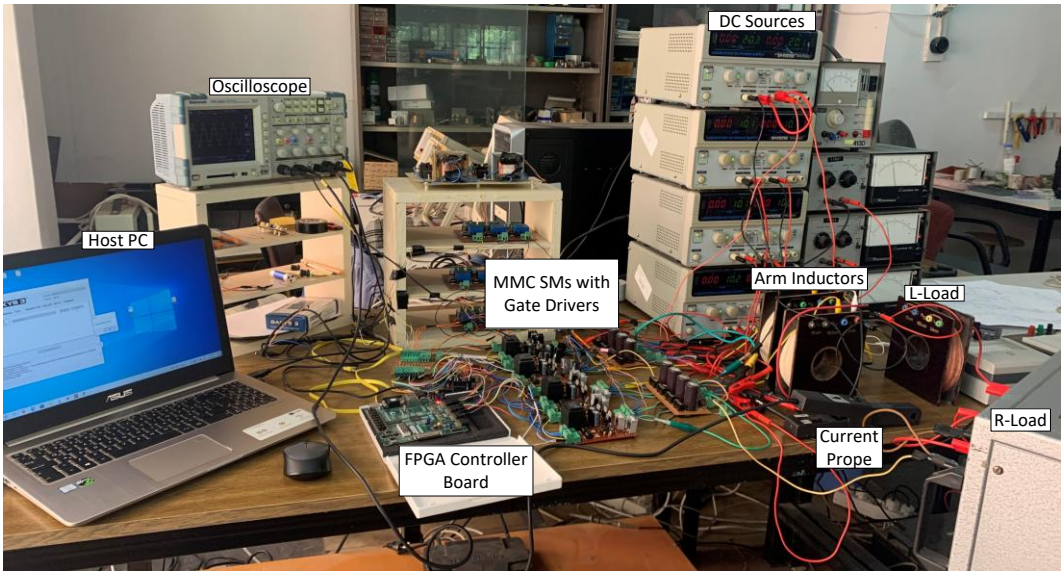
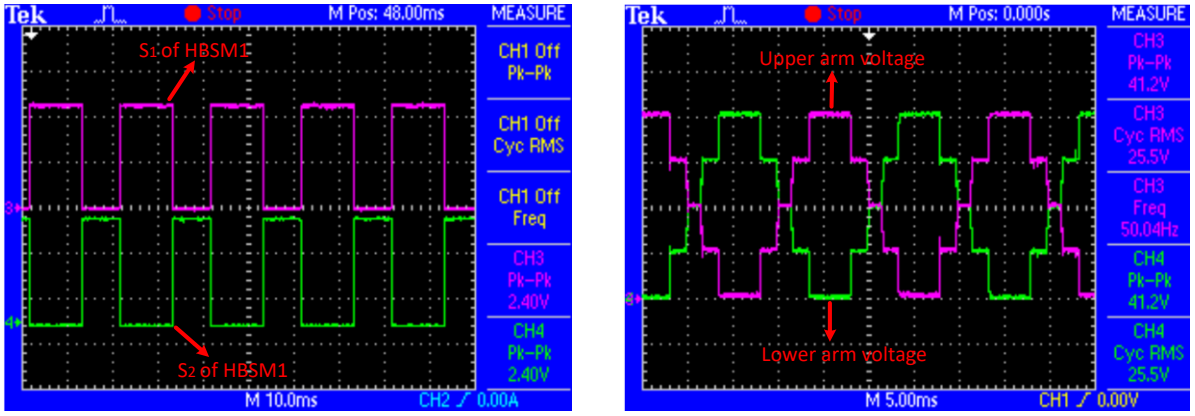


Figure 9. Experimental setup of the MMC topology

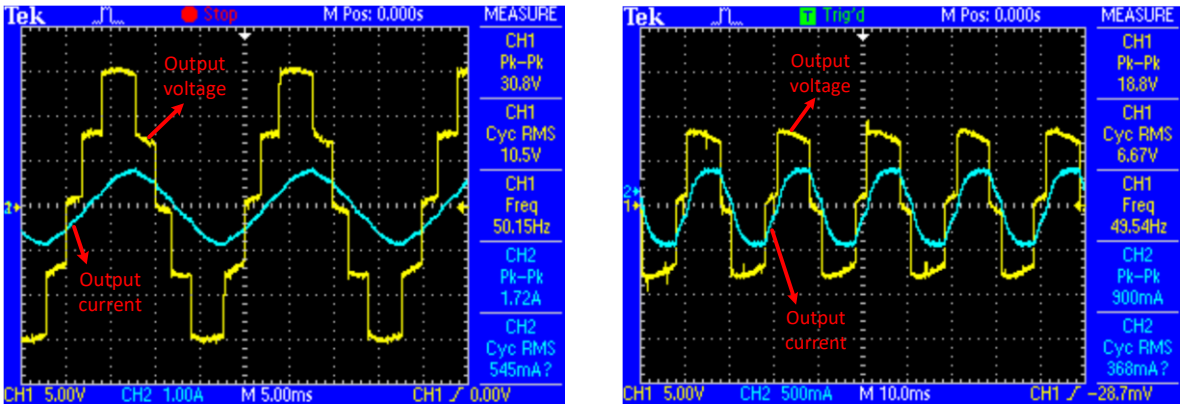
Firstly, gate signals of S_1 (channel (3)) and S_2 (channel (4)) semiconductors of HBSM1 for upper arm are presented in Figure 10(a). As seen in the screenshot of the oscilloscope, the triggering pulses are generated in the opposite manner. S_1 and S_2 semiconductors are driven by signal indicated as pink one and green one, respectively. Upper and lower arm voltages are shown in Figure 10(b), which is created as 5 levels and 50 Hz frequency for each arm.



(a) (b)

Figure 10. (a) a view of the gate signals of S_1 and S_2 semiconductors of HBSM1 for upper arm, (b) arm voltages

Secondly, output voltage and current waveforms of the MMC topology are demonstrated in Figure 11(a) and Figure 11(b), respectively. Fundamental output frequency of the waveforms is generated as 50 Hz. In the screenshots, output voltage and current are visualized when M=0.9 in Figure 11(a) and M=0.6 in Figure 11(b), respectively. As seen in Figure 11(a), output voltage is generated as 5 levels and equal to nearly 10.5 Vrms value while output current is equal to nearly 0.54 Arms. Furthermore, as indicated in Figure 11(b), output voltage is generated as 3 levels and equal to nearly 6.67 Vrms value while output current is equal to nearly 0.36 Arms.



(a) (b)

Figure 11. Output voltage and current waveforms (a) when M=0.9; (b) when M=0.6

6. Conclusions

The implementation of the NLM method on MMC using digital control methods is gaining popularity among scholars because of adaptive controllability and modular realization. In order to accomplish this aim, FPGAs are preferred due to their benefits such as high speed performance and parallel processing ability. For this reason, FPGA based control scheme of the NLM method has been proposed for single-phase five-level MMC topology. In this regard, VHDL modules have been utilized to perform the proposed architectural scheme of the NLM method by presenting each VHDL module and algorithm used in the implementation. The architectural steps of the FPGA realization of the NLM method have been presented

in detail. Gate signals of the switching devices of the MMC topology have been investigated in simulation environment. To confirm the feasibility of the NLM on MMC topology, an experimental setup has been established and experimental results have been presented. According to the obtained findings of this study, validation of the NLM method using the proposed architectural design for single-phase five-level MMC topology has been performed and its practical implementation has been shown. In addition, the outcomes including gate signals, arm voltages and output voltages with currents have been presented for various modulation index values by utilizing the RL load.

7. Author Contribution Statement

Author 1 carried out the literature review, analyzed the proposed architectural design of the NLM method and prepared the paper. Author 1 also carried out the simulation and experimental study. Author 2 contributed data collection, design of the proposed architectural design of the NLM method and evaluating the obtained results. Author 3 contributed the supervising all stages in the paper.

8. Ethics Committee Approval and Statement of Conflict of Interest

There is no need to obtain ethics committee permission for the article prepared. There is no conflict of interest with any person/institution in the prepared article.

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