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GENERALIZED THERMAL OPTIMIZATION METHOD FOR THE PLATE-FIN HEAT SINKS OF HIGH LUMEN LIGHT EMITTING DIODE ARRAYS

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Abstract: The performance of high-lumen light-emitting diode (LED) arrays is strongly affected by high temperatures. For better performance, the design of better thermal management techniques is required. In this work, an analytical thermal optimization algorithm for the passive heat sinks of high-lumen LED arrays is presented. With the aid of this algorithm, a broader range of heat sink geometry alternatives can be explored for the identification of the optimal heat sink design. This task is challenging using experimental or numerical techniques. The results demonstrate that the algorithm yields design with a reduction of more than 30% in base temperatures compared to previous heat sink design studies when minimum mass and maximum total efficiency constraints are applied. For devices with high powers, small chip spacing, and space limitations in the horizontal axis where base temperatures cannot be further reduced using these constraints, minimum temperature optimization can result in up to a 17% reduction in base temperatures. This reduction in base temperatures significantly improves the junction temperatures and the overall lighting quality of the LEDs.
Keywords: Heat sink design, Optimization, High-lumen LED array

YÜKSEK LÜMENLİ IŞIK YAYAN DİYOT DİZİLERİNİN PLAKALI ISI EMİCİLERİ İÇİN GENELLEŞTİRİLMİŞ TERMAL OPTİMİZASYON YÖNTEMİ

Özet: Yüksek lümenli ışık yayan diyot (LED) dizilerinin performansı, yüksek sıcaklıklardan büyük ölçüde etkilenir. Bu yapıların yüksek performansı için geliştirilmiş termal yönetim tekniklerinin tasarımı gereklidir. Bu çalışmada, yüksek lümenli LED dizilerinin pasif soğutucuları için analitik bir termal optimizasyon algoritması sunulmaktadır. Bu algoritmanın yardımıyla, optimum ısı emici tasarımının belirlenmesi için daha geniş bir yelpazedeki ısı emici geometri alternatifleri araştırılabilir. Kullanılan analitik yaklaşım optimizasyon için kullanımı zor olan deneysel veya sayısal tekniklere alternatif sunmaktadır. Sonuçlar, minimum kütle ve maksimum toplam verimlilik kısıtlamaları ile elde edilen taban sıcaklıklarında önceki ısı emici tasarım çalışmalarına göre %30'dan fazla bir azalma göstermektedir. Yüksek güce, küçük çip aralığına ve bu kısıtlamalar kullanılarak taban sıcaklıklarının daha fazla düşürülemeyeceği yatay eksende alan sınırlamalarına sahip cihazlar için minimum sıcaklık kısıtlaması ile gerçekleştirilen optimizasyon, taban sıcaklıklarında %17'ye kadar bir azalmaya neden olabilir. Taban sıcaklıklarındaki bu azalma, bağlantı sıcaklıklarını ve LED'lerin genel aydınlatma kalitesini önemli ölçüde artırır.
Anahtar Kelimeler: Isı emici tasarımı, Optimizasyon, Yüksek lümenli LED dizisi

INTRODUCTION

Light-emitting diodes (LEDs) have been used for several years in automotive, building, and street lighting applications. Due to their advantages such as low energy consumption, efficiency, and lifetime, they have been preferred more than other technologies such as incandescent light, fluorescent, and halogen lamps (Karlicek et al., 2017). Although LEDs have these advantages, the thermal problems of this technology still exist. LED structures produce heat and light by using electrical energy. About 80% - 90% of the total electrical energy is converted into heat (Ye et al., 2011). This often causes a single LED chip to generate 100-125 W/cm^2 heat flux (Wang et al., 2015). Generated heat leads to high chip temperatures. In high-lumen LED array systems used for high-performance applications such as outdoor and industrial lighting, hundreds of LED chips are used together. Since these chips are placed on a printed circuit board (PCB) as illustrated in Figure 1, higher temperatures can be seen because of the number of LED chips and the thermal crosstalk between them (Rammohan et al., 2021).

High chip temperatures negatively affect the chip's efficiency, light output, performance, and lifetime. To solve the thermal problems of the LED arrays, different thermal management techniques such as thermoelectric coolers (TECs) (Li et al., 2011), heat pipes (Delendik et al., 2021; Lu et al., 2011), liquid cooling methods (Deng

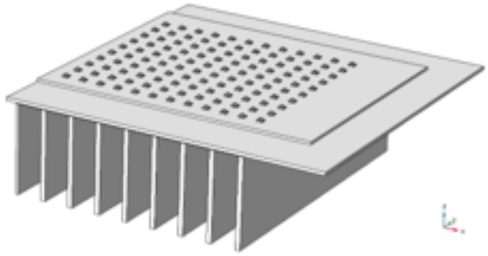

Figure 1. High-lumen LED array structure.

and Liu, 2010), and finned heat sinks (Hsu et al., 2020; Ye et al., 2011) have been suggested in the literature. (TECs) (Li et al., 2011), heat pipes (Delendik et al., 2021; Lu et al., 2011), liquid cooling methods (Deng and Liu, 2010), and finned heat sinks (Hsu et al., 2020; Ye et al., 2011) have been suggested in the literature. Among these methods, passive thermal management via finned heat sinks is preferred the most since no extra parts such as fans and/or pumps as well as cooling liquids are required (Feng et al., 2018). Although there are heat sinks with various fin cross-section geometries (triangular, pin, etc.), plate-fin heat sinks, shown in Figure 2, are the most frequently used type due to their relatively simple fabrication and easy maintenance.

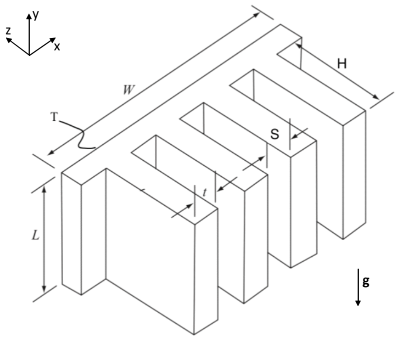

Figure 2. Fin structure.

Design and optimization of plate-fin heat sinks have been known for a long time. Countless analytical (Bar-Cohen et al., 2003; Bar-Cohen and Jelinek, 1985; Elenbaas, 1948), numerical (Ben Abdelmlek et al., 2021, 2017; Goshayeshi et al., 2011), parametric (Patel and Matawala, 2019; Walunj et al., 2013) and experimental (Abdelmlek et al., 2015; Yüncü and Anbar, 1998) work have been performed in the past for this purpose. However, most of the previous studies performed optimization using a fixed base temperature and area. For high-lumen LED arrays the heat load instead of base temperature is fixed and the base area can be varied with the different arrangements of the array elements. There are a limited number of optimization studies performed without using fixed base temperature (Hsieh and Li, 2015; Liu, 2012; Tang et al., 2015). However, the LED array powers used in these studies are relatively low and the effect of the LED configuration on optimization is not studied. Moreover, these studies involve finite element simulations with high mesh requirements due to the geometrical nature of fin elements. Therefore, previous methodologies are not sufficient to design optimized heat sinks for high-lumen LED arrays. There is a need for a fast and reliable generalized heat sink optimization algorithm for the passive thermal management of high-lumen LED arrays.

In this study, we display a generalized optimization method that allows variable base temperatures and areas. Using this algorithm, a wider group of alternatives is searched, and more suitable heat sinks for high-lumen LED arrays are achieved. The results are analyzed to observe the positive effects of more flexible design variables on the optimization performed. This task is challenging using experimental or numerical techniques. Although this study is dedicated to plate-fin heat sinks used for passive thermal management, the methodology can be modified or extended for the analysis of heat sinks with different topologies used in both passive and active thermal management.

METHOD

In this section, the details of the numerical algorithm used in the generalized optimization technique are provided. The algorithm depends on empirical natural convection correlations gathered from the literature. The calculations are performed for each configuration in MATLAB. Pure aluminum with thermal conductivity, density, and the specific heat of k_{fin}=197 W/m·K, ρ_{fin} = 2700 kg/m3, and c_p =910 J/kg·K, respectively is chosen as the heat sink material (Incropera et al., 2007a). The input parameters are the total number of LED chips (N_{chips}) and the desired heat dissipation ($\dot{Q}_{desired}$). The numerical optimization technique presented here starts with the above input variables and aims to obtain the best LED array arrangement, fin number, fin spacing, and base temperature under different constraints. The methodology is explained below in two parts: a) Database Creation and b) Structure Selection.

Database Creation

The steps of database creation summarized in Figure 4 are explained in this section.

1. The first step of the optimization is to enter the input variables: N_{chips} and $\dot{Q}_{desired}$. The desired heat dissipation can be taken as 75% of the total power consumed by the LED array since only a certain amount of power is dissipated as heat.

2. Then set N_x (number of chips in -x direction) and calculate Ny. Calculate the width (W) and length (L) of the heat sink based on the given arrangement, spacings, and size of the chips in

the array using the geometrical variables in Figure 3.

$$W = c_x \times N_x + d_x \times (N_x - 1) \quad (1)$$

$$L = c_y \times N_y + d_y \times (N_y - 1) \quad (2)$$

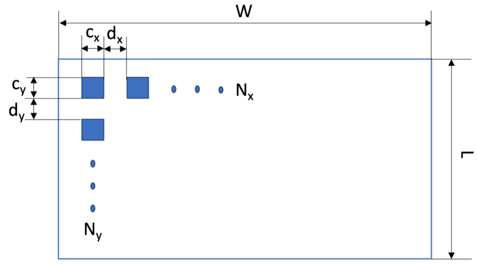

Figure 3. LED array configuration.

3. Next set the base temperature of the fins to T_{base}. Then obtain the material properties (thermal conductivity (k_{air}), dynamic viscosity (μ_{air}), and Prandtl number (Pr)) of the cooling fluid (in this case air) at the film temperature $\left(T_{film} = \frac{T_{base}+T_\infty}{2}\right)$, where $T_\infty = 300K$.

4. To find the heat transfer coefficient (h_{wall}) of the vertical walls between the fins, Rayleigh number (Ra_L) is calculated(Elenbaas, 1942):

$$Ra_L = \frac{g\beta\theta_b L^3}{\alpha v} \quad (3)$$

where g is the gravitational constant, β is the thermal expansion coefficient, θ_b=(T_{base}-T_∞) is the temperature difference between the ambient and the base, L is the length of the fin, α is the thermal diffusivity and v is the kinematic viscosity of the air at film temperature.

5. The convection coefficient of the vertical fin wall shown is calculated (Incropera et al., 2007b):

$$h_{wall} = \begin{cases} \frac{0.59Ra_Z^{0.25}k_{air}}{L}, 10^4 < Ra_L < 10^9 \\ \frac{0.1Ra_Z^{1/3}k_{air}}{L}, 10^9 < Ra_L < 10^{13} \end{cases} \quad (4)$$

6. The optimum spacing between the fins, S is calculated using the relations of Bar-Cohen and Rohsenow (Bar-Cohen and Rohsenow, 1984):

$$S = 2.714Ra_L^{-0.25}L \quad (5)$$

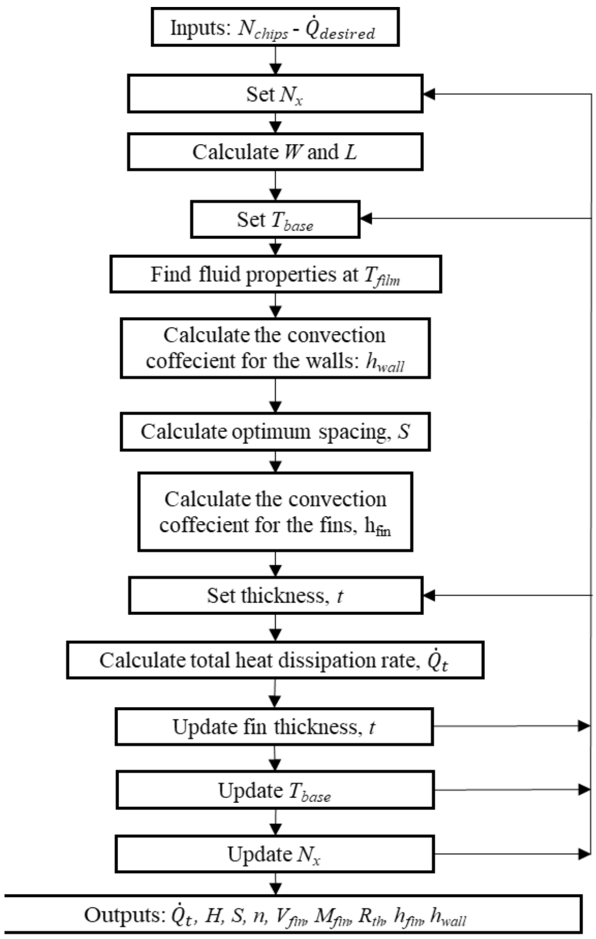

Figure 4. Optimization Algorithm.

7. To find the convection heat transfer coefficient on fin surfaces: h_{fin}, natural convection correlations obtained by Elenbaas (Elenbaas, 1942) are used. To do this first the Rayleigh number based on optimum spacing is calculated (Lee, 2010):

$$Ra_S = \frac{g\beta\theta_b S^3}{\alpha v} \quad (6)$$

Then Elenbaas number (El) is calculated with Ra_S, S_{opt}, and L with below equation (Kraus, et al., 2001):

$$El = Ra_S \frac{S}{L} \quad (7)$$

Nusselt number, Nu is calculated (Kraus, et al., 2001):

$$Nu = \left(\frac{576}{El^2} + \frac{2.873}{El^{0.5}}\right)^{-0.5} \quad (8)$$

Finally, the heat transfer coefficient of the fin is obtained from the Nu number and the optimum spacing.

$$h_{fin} = \frac{Nu \times k_{air}}{S} \quad (9)$$

8. Next to perform the optimization with varying fin thickness, set a fin thickness, t.

9. Assuming the heat loss at the fin tip is negligible, the heat transfer rate from a single fin with an adiabatic tip ($\dot{q}_f$) is calculated using (Kraus, et al., 2001):

$$\dot{q}_f = \sqrt{2h_{fin}k_{fin}t}\theta_b L tanh(mH) \quad (10)$$

where m is the performance factor and H is the height of the fin:

$$m = (\frac{2h_{fin}}{k_{fin}t})^{0.5} \quad (11)$$

To get the maximum heat transfer rate, the following fin height formula is used (Kraus, et al., 2001):

$$H(t) = \frac{1.4192\left(\frac{k_{fin}t}{2h_{wall}}\right)^{0.5}}{\left[1-1.125\left(\frac{k_{fin}t}{2h_{wall}}\right)^{0.5}\frac{h_{wall}}{k_{fin}}\right]} \quad (12)$$

Later, the total heat transfer rate from the walls of heat sink is calculated as (Kraus, et al., 2001):

$$\dot{q}_w = h_{wall}LS_{opt}\theta_b \quad (13)$$

The total heat transfer rate is the sum of the heat transfer from the walls and fin surfaces (Kraus, et al., 2001).

$$\dot{Q}_t = nL\theta_b\left[\sqrt{2h_{fin}k_{fin}t}tanh(mH) + h_{wall}(\frac{W}{n} - t)\right] \quad (14)$$

where n is the number of the fins allowed for given S, t, and W.

$$n = \frac{W}{S+t} \quad (15)$$

Finally, the total thermal resistance, fin volume and mass of the heat sink are calculated.

$$R_{th} = \theta_b/\dot{Q}_t \quad (16)$$

$$V_{fin} = L \times H \times t \times n \quad (17)$$

$$M_{fin} = V_{fin} * \rho_{fin} \quad (18)$$

where ρ_{fin} is the fin density.

10. Change thickness and repeat steps 8 and 9 until all desired thickness values are analyzed.

11. Change T_{base} and repeat steps 3 to 10 until all desired base temperature values are analyzed.

12. Change N_x and repeat steps 2 to 11 until N_x=N_{chips}.

At the end of these steps, a database given in Table 1 is obtained. $\dot{Q}_t, H, S, n, V_{fin}, M_{fin}, R_{th}, h_{fin}, h_{wall}$ values for each thickness and temperature are stored in the database.

Table 1. Optimization outputs for a given base temperature and fin thickness.

	Temperature (K)			
Thickness (mm)	**300 K**	**300.1 K**	**...**	**350 K**
1 mm	$\dot{Q}_t, H, S, n,$ $V_{fin}, M_{fin},$ $R_{th}, h_{fin}, h_{wall}$	...	...	...
1.1 mm	...	...	...	...
...	...	...	...	...
20 mm	...	...	...	$\dot{Q}_t, H, S, n,$ $V_{fin}, M_{fin},$ $R_{th}, h_{fin}, h_{wall}$

Structure Selection

After creating the database, it is filtered to find the configurations with a total heat removal rate equal to the desired heat dissipation rate $\dot{Q}_t = \dot{Q}_{desired}$. Then, the data is analyzed to find the optimum structure. As shown in Figure 5 optimization can be performed with varying motives. These are explained next.

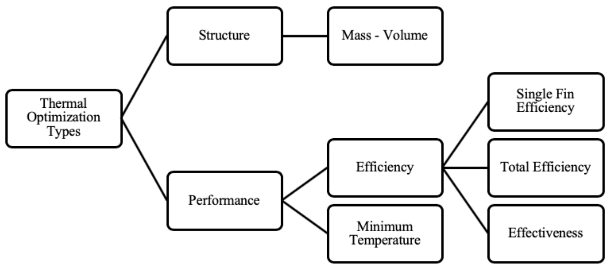

Figure 5. Optimization Types.

Minimum Fin Mass (M_{fin}): This type of optimization is generally chosen for low-cost (Feng et al., 2018) and lightweight applications. The cost of the heat sink can be reduced by decreasing the total material used. The configuration with the smallest mass is chosen.

Total Efficiency (η_{tot}):

$$\eta_{tot} = \frac{Q}{Q_{max}} \quad (19)$$

where, $\dot{Q}_{max} = \theta_b h_{fin} n(2(L + tH + LS)$ is another selection criterion. The filtered database is analyzed to obtain the configuration with the highest η_{tot}.

Maximum Single Fin Efficiency (η_{fin}): Single fin efficiency is the ratio of the heat transfer from a single fin to the maximum possible heat transfer from the fin (Ghajar et al., 1986):

$$\eta_{fin} = \frac{\tanh(mH)}{mH} \tag{20}$$

The data is analyzed to obtain the configuration with the highest η_{fin} to reduce the number of the fins.

Minimum base temperature (T_{base}): Minimum base temperature is obtained where the thermal resistance, given by Eq. (16) is smallest. The data is analyzed to obtain the configuration with the minimum thermal resistance that will give the minimum base temperature.

The optimization performed using the above steps assumes there are no geometric limitations. However, in real applications there may be some restrictions, mostly coming from fabrication limitations, such as the maximum/minimum fin thickness, fin length, or the ratio of the fin height to fin thickness. If any of these restrictions exist, then additional data filtering is needed at the beginning of structure selection. Here data that does not comply with the given limitations can be removed.

RESULTS

The above methodology is applied to optimize the heat sink of a high lumen LED array composed of N_{chips}=240 LED chips (Cree X-Lamp XP-E). The total heat generated by the chips are calculated as $\dot{Q}_{desired}$=192 W (with a single chip generating 0.8W heat). The chip dimensions and spacings are $c_x = c_y = 3.45$ mm and $d_x = d_y = 2$ mm, respectively. Using the numerical optimization algorithm described above, optimization is performed for different chip layout configurations. Table 2 summarizes these layout configurations and the resulting base area dimensions.

Table 2. Different chip layout configurations.

Configurations	N_x	N_y	W (mm)	L (mm)
1	48	5	269.6	29.25
2	24	10	138.8	56.5
3	16	15	95.2	83.75
4	12	20	73.4	111
5	10	24	62.5	132.8

The effect of optimization type on the base temperature of LED arrays with different layout configurations is plotted in Figure 6. When the number of chips along the *y*-direction (N_y) decreases, the fin length L decreases, and the fin width W increases. As a result of this, optimum spacing, S decreases, and the number of fins (n) as well as the convection coefficient at the fin surfaces (h_{fin}) increases. Thus, the heated air can leave the structure quickly and the base temperatures are reduced. However, very high masses are observed for these types of configurations.

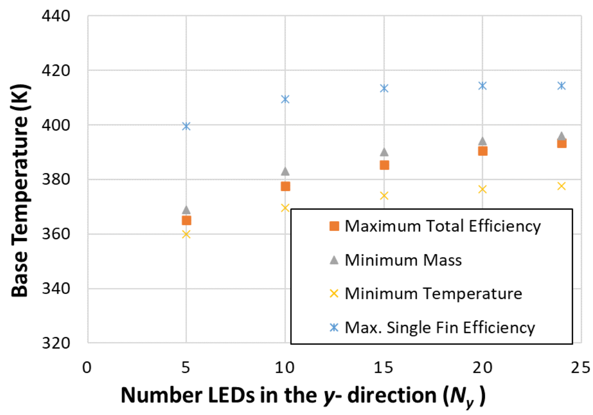

Figure 6. Base temperature vs. number of LED chips in y-direction when different optimization criteria are used.

When the number of chips along the *y*-direction increases, the heated air cannot leave the structure quickly, fin convection coefficients decrease, and the base temperature increases. However, the increase in base temperatures slows down when N_y exceeds 15. Given the tendency for vertically oriented LED arrays to experience elevated temperatures, opting for minimum temperature optimization can offer substantial advantages in terms of temperature management. Such configuration may yield a reduction in a temperature rise of up to 17%, albeit accompanied by a three-to-four-fold increase in mass. In general, total efficiency is a safe optimization type for all configurations since it provides a design with a reasonable base temperature and fin mass.

Later, the 2nd configuration with N_x=24 is chosen to have a closer look at the effects of the optimization constraints on the optimized structure. The results are summarized in Table 3. In Table 3, maximum fin height and temperatures are observed when the single fin efficiency optimization type is chosen. Although the total number of fins is low, they weigh more than 10 times the fins in other optimization types making the heat sink extremely heavy. Therefore, single-fin efficiency optimization is not recommended while designing heat sinks for high-lumen LED arrays. Minimum fin heights are observed when the minimum mass optimization type is chosen. However, the base temperatures are still higher than the ones obtained from two other optimizations. Although the minimum base temperature optimization type has the lowest temperature, it results in a heat sink design with a higher mass and length than the one obtained for maximum efficiency optimization. For this configuration, and in general, the maximum efficiency optimization type provides a reasonable mass value and a base temperature. There are a limited number of optimization studies performed without using fixed base temperature (Hsieh and Li, 2015; Liu, 2012; Tang et al., 2015).

The above results are obtained when the heat generation is kept constant at $\dot{Q}_{desired}$= 192 W. However, LED arrays can have varying heat generation values. To understand the effect of this on the optimization, the following heat generation values are used $\dot{Q}_{desired}$= 48 W, 96 W, 192 W, 216W, and 240 W. Number of chips (N_{chips} = 240), layout (N_x=24 and N_y=10), and spacings ($d_x = d_y$ = 2 mm) are kept constant. The effect of optimization type on base temperature for different LED powers is plotted in Figure 7.

According to Figure 7 optimization type does not have a strong effect on the base temperature and can be chosen freely at low powers. The difference increases at higher powers. Single-fin efficiency and minimum mass constraints should be avoided, and minimum temperature or maximum total efficiency constraints should be preferred when designing heat sinks for LED arrays at higher powers where temperatures are closer to design limitations.

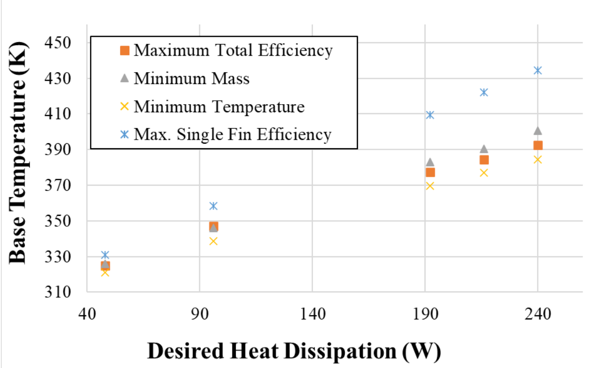

Figure 7. Base temperature vs. desired heat dissipation when different optimization criteria are used. Number of chips (N_{chips} = 240), layout (N_x=24 and N_y=10), and spacings ($d_x = d_y$ = 2 mm) are kept constant.

Finally, to observe the effect of chip spacing on base temperatures chip spacing values are varied as $d_x = d_y$= 1, 2, 3, 4, and 5 mm. The total amount of desired heat dissipation ($\dot{Q}_{desired}$= 192 W), number of chips (N_{chips} = 240), and the layout (N_x=24 and N_y=10) are kept constant. The effect of optimization type on base temperatures for different LED spacings is plotted in Figure 8. According to Figure 8, the choice of the optimization type does not have a strong effect on base temperature when chips are spread out to a wider area. For larger spacing configurations, the contribution of the base of the heat sink to convection is increased, thus the effect of the fins on heat transfer is reduced. This situation leads to lower base temperatures and reduces the significance of the choice of optimization type. However, if the spacings are small then the base temperature values may exceed the maximum junction temperatures of the LED chips present in their datasheets. If the spacings are small, then the minimum temperature optimization type can be chosen despite its other disadvantages to reduce thermal risks.

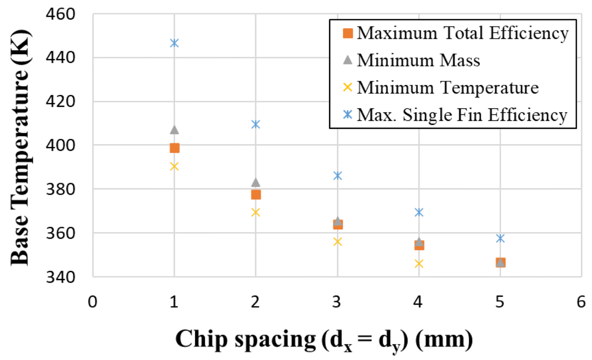

Figure 8. Base temperature vs. distance between LED chips when different optimization criteria are used. The total amount of desired heat dissipation ($\dot{Q}_{desired}$= 192 W), number of chips (N_{chips} = 240), and the layout (N_x=24 and N_y=10) are kept constant.

The base temperatures presented for the initial structure in Table 3 are compared with the base temperatures of previous analytical studies which typically begin the optimization using a fixed base temperature (Bar-Cohen et al., 2003) calculated from the maximum allowed junction temperature in LED datasheets. With the maximum total efficiency and minimum mass constraints of the proposed methodology, a reduction of more than 30% in base temperatures is achieved. Additionally, when a minimum temperature constraint is chosen, a further 5% reduction in base temperatures can be achieved. Although this option has a high mass disadvantage for devices with closely packed, vertically arranged, high-power chips where base temperatures cannot be further reduced using other constraints, the minimum temperature constraint is a viable option, resulting in a 17% reduction in base temperatures. Similar improvements have been reported in the literature but for smaller devices using lengthy numerical calculations (Ben Abdelmlek et al., 2021, 2017).

CONCLUSION

In high-lumen LED array systems extremely high temperatures are observed due to the large amount of heat

Table 3. Optimization results of the initial structure.

Optimization Type	H (mm)	t (mm)	S (mm)	T_{base} (K)	n	R_{th} (K/W)	η_{fin} (%)	η_{tot} (%)	M_{fin} (kg)	ε_{fin}	h_{fin} (W/m^{2}K)	h_{wall} (W/m^{2}K)
Maximum η_{tot}	163	1.30	5.16	378	22	0.42	38.9	65.3	0.75	202	7.37	9.01
Minimum Mass	148	1.00	5.13	383	24	0.44	34.2	65.1	0.53	229	7.48	9.17
Minimum T_{base}	268	3.20	5.23	370	17	0.37	56.4	62.2	2.22	125	7.20	8.82
Maximum η_{fin}	580	16.0	5.00	410	7	0.59	84.8	39.4	9.29	40.0	7.92	9.71

generation and the thermal crosstalk between the chips. To reduce the thermal problems of the LED arrays, proper heat sink design should be performed. In this study, we display a computationally effective analytical optimization method that allows the exploration of a wider group of base temperature and area alternatives. The proposed scheme only requires two input variables: the number of chips and the desired heat dissipation to create a database. The database is analyzed using a numerical technique to find the most suitable chip layout and heat sink geometry. The algorithm is tested on an LED chip array to discuss the heat sink base temperatures achieved by this algorithm using different optimization constraints in different scenarios. The results are summarized as follows:

- With the maximum total efficiency and minimum mass constraints of the proposed methodology, a reduction of more than 30% in base temperatures is achieved compared to previous heat sink design studies. These previous studies typically begin with optimization using a fixed base temperature calculated from the maximum allowed junction temperature in LED datasheets.
- When a minimum temperature constraint is chosen a further 5% reduction in base temperatures can be achieved, however, the heat sink mass is significantly increased.
- For devices with closely packed, vertically arranged, high-power chips where base temperatures cannot be further reduced using other constraints, minimum temperature constraint results in a 17% reduction in base temperatures. In scenarios where mass is not a constraint, minimum temperature optimization should be prioritized for such LED arrays to ensure the lowest achievable temperature.
- Maximum single-fin efficiency should not be a constraint in any optimization study since it leads to heat sink designs with extremely high mass and base temperatures.

The reduction in base temperatures will cause a similar decrease in junction temperatures and strongly affect the lighting quality of the devices. Although this study is dedicated to plate-fin heat sink optimization for passive thermal management, the methodology can be modified or extended to analyze passive and active heat sinks with different topologies.

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NOMENCLATURE

α	Thermal diffusivity of air [m^2/s]
β	Thermal expansion coefficient of air [1/m]
υ	Kinematic viscosity of air [m^2/s]
k_{air}	Thermal conductivity of air [W/m·K]
k_{fin}	Thermal conductivity of fin material [W/m·K]
El	Elenbaas Number $\left[Ra_S \frac{S}{L}\right]$
g	Gravitational constant [m/s^2]
H	Fin height [mm]
L	Fin length [mm]
W	Base plate width [mm]
T	Fin thickness [mm]
P	Fin perimeter [mm]
S	Optimum fin spacing [mm]
A	Fin base area [mm^2]
M_{fin}	Fin mass [kg]
V_{fin}	Fin volume [m^3]
Ra_s	Rayleigh number based on fin spacing $\left[\frac{g\beta\theta_b S^3}{\alpha\upsilon}\right]$
Ra_L	Rayleigh number for vertical plates $\left[\frac{g\beta\theta_b L^3}{\alpha\upsilon}\right]$
θ_b	Ambient air and base temperature difference[K]
Nu	Nusselt number $\left[\frac{h_{fin}S}{k_{air}}\right]$
h_{fin}	Fin convection coefficient [W/m^{2}K]
h_{wall}	Wall convection coefficient [W/m^{2}K]
m	Performance factor $\left[\sqrt{\frac{2h_{fin}}{k_{fin}t}}\right]$
R_{th}	Thermal Resistance [K/W]
$\dot{q}_f$	Heat transfer rate from a single fin [W]
$\dot{Q}_t$	Total heat transfer rate [W]
$\dot{Q}_{desired}$	Desired heat dissipation rate [W]

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