Black Sea Journal of Engineering and Science
doi: 10.34248/bsengineering.1515784

Open Access Journal
e-ISSN: 2619 – 8991

Research Article
Volume 7 - Issue 5: 907-916 / September 2024

# NOVEL AND LOW-COST TECHNIQUES FOR EXTENDING THE ETCH CAPABILITIES OF AN INDUCTIVELY COUPLED PLASMA ETCH TOOL THAT HAS CLAMP FINGERS FOR CLAMPING 4-INCH DIAMETER WAFERS

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**Abstract:** Widening the processing capabilities of an inductively coupled plasma (ICP) etch tool by "preventing wafer breakage" during processing of wafers, or by gaining the capability to do "through-wafer silicon etch" are important challenges that may need to be resolved with very limited resources. Resolving the undesired wafer breakage issues caused during processing of wafers is important to reduce the manufacturing costs, and increase production yield. Furthermore, considering the high prices of the state-of-the-art wafer processing tools, it is also important to prevent wafer breakage by using low-cost approaches especially if the resources for purchasing state-of-the-art processing equipment are not available. Two novel methods (method #1, and method #2) are developed to prevent wafer breakage and allow through-wafer silicon etching. With method #1, an aluminium alloy ring (AAR) and an o-ring are employed to obtain uniform load distribution (instead of point loads) on the required outer region on the surface of a wafer, and to minimize or completely remove the bending moment that may be formed on the possible cross-sections of the entire wafer, during clamping of the wafer. With method #2, through-wafer silicon etching is made possible by simultaneous application of method #1 and addition of a helium cooling gas (HCG) leakage blocking dicing tape at the back side of the wafer that is under processing for through-wafer etching. By using the explained methods, wafer breakage during ICP etch processing is eliminated, and through-wafer silicon etching is made possible. From the other side, the effective wafer area that can be used for processing is reduced by 48%. Novel and capability enabling 2 different techniques that are extremely low-cost compared to purchasing a state-of-the-art ICP etch tool are presented to extend the processing capabilities of an ICP etch tool for deep silicon etching (method #1), and through-wafer silicon etching (method #2).

**Keywords:** Low-cost, Inductively coupled plasma (ICP), Wafer breakage, Wafer breakage prevention, Wafer breakage-free, Through-wafer silicon etch

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**Received:** July 14, 2024
**Accepted:** August 12, 2024
**Published:** September 15, 2024

**Cite as:** Yilmaz M. 2024. Novel and low-cost techniques for extending the etch capabilities of an inductively coupled plasma etch tool that has clamp fingers for clamping 4-inch diameter wafers. BSJ Eng Sci, 7(5): 907-916.

## 1. Introduction

Prices of state-of-the-art inductively coupled plasma (ICP) etch tools for deep reactive ion etching (DRIE) of silicon wafer at research laboratories may easily start from 1 million USD, and go up to 1.5 million USD or even more per tool, depending on the purchased technical capabilities of the tool (SPTS, 2024), (Plasma-Therm, 2024), (Oxford Instruments, 2024), (Corial, 2024), (Sentech, 2024). However, such large amounts of money may not be easily obtained or may not be immediately available for purchasing state of the art plasma etch tools for deep reactive ion etching (DRIE) processing needs of cleanroom users. Instead, to satisfy some of the critical needs (such as wafer breakage prevention or through wafer silicon etching) of ICP etch tool users, novel techniques that are very low-cost, may be developed for a very small fraction of the total price of state-of-the-art plasma etch tools.

Over the years, wafer breakage has been identified as a critical problem that has taken attention of engineers and scientists to find solutions to prevent wafer breakage to decrease manufacturing costs, and increase production rates (McLaughlin and Willoughby, 1987), (Chen et al., 2010), (Brun and Melkote, 2009), (Chowdhury et al., 2020), (Zhou et al., 2015), (Chen et al., 2007), (Liu et al., 2022), (Saffar et al., 2015). Causes of the wafer breakage can be classified under three major branches such as:

1. Wafer breakage during manufacturing of the wafers (Wafer World Inc., 2021), (Silyb Wafer Services Inc., 2023), (Chen et al., 2010), (Liu et al., 2022),
2. Wafer breakage during transportation and handling of the wafers (Wafer World Inc., 2021), (Silyb Wafer Services Inc., 2023), (Brun and Melkote, 2009), (Chowdhury et al., 2020), (Saffar et al., 2015),
3. Wafer breakage during processing of the wafers in the relevant processing equipment (Chowdhury et al., 2020).

According to (Chowdhury et al., 2020), to minimize wafer

breakage inside a dry etch tool, "clamping force adjustment and chuck curvature control" should be optimized. Furthermore, considering that "wafer clamping" at the beginning of a process or "wafer clamping" during processing a wafer can be considered as "wafer handling", appropriate wafer handling approaches presented in (Brun and Melkote, 2009), and (Saffar et al., 2015), may be used to minimize wafer breakage events. For example, both (Brun and Melkote, 2009), and (Saffar et al., 2015), suggest that, the wafers should be handled such that the propagation of cracks or initiation of cracks should be avoided to prevent the wafers from breakage. In order to minimize crack propagation or crack initiation, it is important to minimize the stresses or stress concentrations on the wafers. This research paper aimed to minimize stresses or stress concentrations on wafers to prevent undesired crack propagation or crack initiation.

According to the available literature, there are at least three different approaches to handle a wafer during etch processing. These three approaches are listed below:

1. Using electrostatic chucks to clamp the wafers (Bonfim et al., 1993), (Izyumov, 2009),
2. Using carrier wafers to adapt the wafer under process to the clamping conditions of the etch equipment (Noori et al., 2024), and (Meyer et al., 2022),
3. As in the etch tool used in this research study, wafers can be clamped by using symmetrically arranged clamping fingers.

One of the silicon wafers that has been processed with the original wafer clamping system of the etch tool used in this study is shown in Figure 1. As can be seen in Figure, the wafer is broken during the etch processing of the wafer. Based on the experimental studies performed in this research, two optimization opportunities on the design of the original wafer clamping system of the etch tool are identified that cause wafer breakage as the depth of the features etched into silicon become deeper and deeper:

1. Point loads from equally separated 8 points (clamping fingers) are applied on the wafer. Such point loads (clamping fingers) cause stress concentrations that cause wafer breakage especially after sufficient amount of depth of silicon is etched,
2. Due to the location of the applied point loads (i.e. misaligned from the top of the "bottom o-ring (helium cooling gas (HCG) gasket)"), bending moments are formed on the wafer. These bending moments cause wafer breakage especially after sufficient amount of depth of silicon is etched.

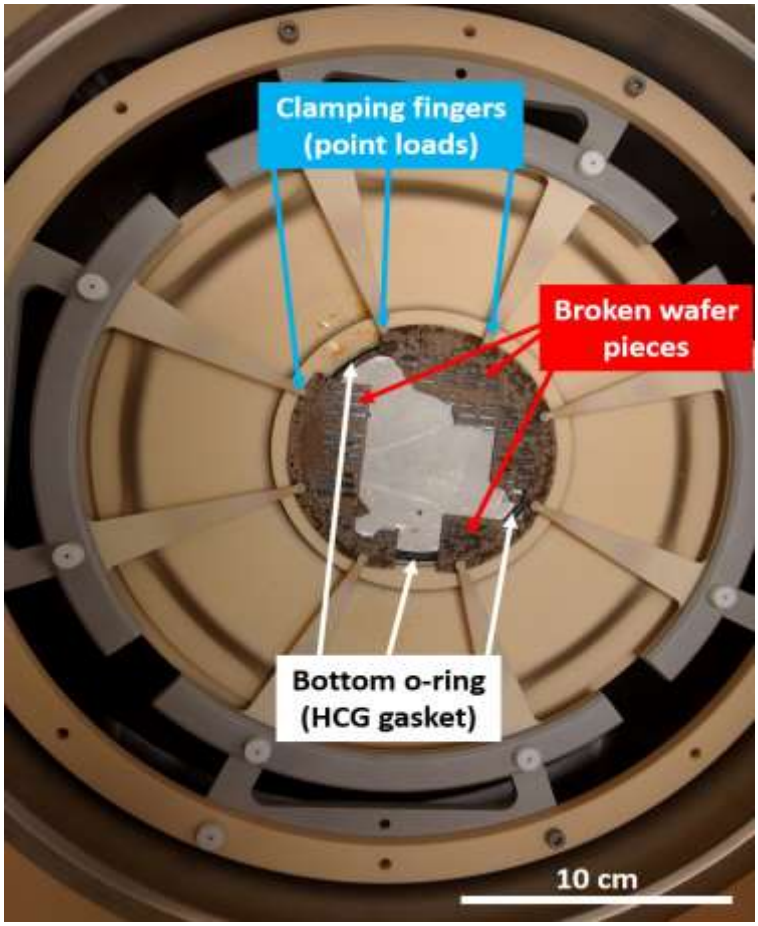


**Figure 1.** Top-down view of the inner side of the ICP etching tool process chamber that has a broken wafer. For the demonstration of the possible issues, broken wafer pieces are still clamped under the 8 clamping fingers (8 point loads) of the ICP etch tool. (HCG: helium cooling gas to cool the wafer from the back side of the wafer).

To achieve "breakage-free" wafer production approaches (explained in method #1), two modifications has been done to:

1. Uniformly distribute the clamping force that is applied on the designated region of a wafer,
2. Minimize or completely remove the bending moment that is applied on the wafer.

In this research article, two novel techniques that are aiming two different improvements to significantly extend the "without wafer breakage" processing capabilities of an inductively coupled plasma (ICP) deep silicon etch tool are presented. The first novel method is about preventing wafer breakage during "deep silicon" etching (deeper than 50 microns) using the inductively coupled plasma (ICP) tool that has 8 clamping fingers to clamp a 4-inch diameter silicon wafer during ICP etch processing. The second novel method is about achieving "through-wafer" silicon etching using the same ICP tool with 8 clamping fingers. In other words, this research paper demonstrates development of 2 novel techniques to be able to perform deep silicon etching (method #1), and through-wafer silicon etching (method #2) using wafer scale microfabrication approaches, without causing breakage of the wafers.

## 2. Materials and Methods

### 2.1. Materials

#### 2.1.1. Silicon wafers (substrates)

4-inch diameter single crystal silicon wafers with the standard crystallographic orientations and at least 500 +/- 25 micrometers wafer thickness are tested for deep silicon etching (method #1) and through-wafer silicon etching (method #2). Silicon wafers that are thinner than 500 +/- 25 micrometers may also be used with these two novel methods. However, thinner wafers have not been studied extensively while the results for silicon wafers that are at least 500 +/- 25 micrometers thick are very repeatable with the ICP etch processing tool available at our cleanroom facilities.

#### 2.1.2. Aluminium alloy ring (AAR) with an o-ring channel for uniform load distribution

Main purpose of using an aluminium alloy ring (AAR) (Figure 2) with an o-ring between the 8 clamping fingers and the wafer is to provide a mechanical element that is sufficiently rigid, that can easily receive a set of point loads coming from the 8 clamping fingers of the ICP etching tool (Figure 2 for the 8 clamping fingers that are capable of applying point load only), can easily distribute these 8 point loads as uniformly distributed load, and transfer the uniformly distributed load to the wafer with minimal bending moment on the wafer. The minimal bending moment application on the wafer would be satisfied by making sure that the bottom o-ring (HCG gasket) below the wafer is well aligned with the o-ring that is between the AAR and the top side of the wafer. This way, the wafer would be clamped on the bottom o-ring (gasket) (Figure 1) surface of the helium cooling gas (HCG) chamber with uniformly distributed force rather than the point loads applied directly by the clamping fingers of the ICP tool. Furthermore, because the o-ring above the wafer, and the bottom o-ring (gasket) below the wafer are well aligned, there would be minimized or no bending moment on the wafer. Furthermore, due to formation of native alumina ($Al_2O_3$) on the outer surface of the aluminium alloy materials when aluminium alloy surface is exposed to oxygen (Nabavi et al., 2023) in the air, the aluminium alloy ring becomes very selective to plasma etch processes that have only $SF_6$, or $SF_6$ and $O_2$ gas plasma that may be used in deep etching of silicon wafers.

#### 2.1.3. Circular cross-section o-ring to prevent scratches on the silicon wafer (substrate) surface

To make sure that there is no direct hard contact between the AAR surface and the silicon wafer (or the photoresist on the silicon wafer) surface, it is planned to have a circular cross-section o-ring material (NBR 70 SHORE) to provide soft contact between the aluminium alloy ring, and the wafer. To safely position the circular cross-section o-ring (NBR 70 SHORE), a channel is manufactured into the aluminium alloy ring that is facing the plasma exposed side of the silicon wafer and well aligned with the bottom o-ring (HCG gasket) to minimize the bending moment on the wafer while the wafer is clamped during plasma processing (Please see Figure 3 for the position of the o-ring with respect to the aluminium alloy ring and wafer surface). Hence, the purpose of the circular cross-section o-ring is twofold: First, to eliminate the possibility of direct hard contact between the AAR and the wafer surface, and second, to align the distributed force with the bottom o-ring such that the bending moment on the clamped wafer is minimized.

#### 2.1.4. Dicing tape at the back side of the wafer to prevent the helium cooling gas (HCG) from entering into the ICP process chamber

In this study, a type of dicing tape (ADWILL D-841) that is UV light sensitive and that has very strong adhesion properties before being exposed to UV light, and very weak adhesion properties after being exposed to UV light, is successfully used to prevent the helium cooling gas (HCG) from entering into the plasma process chamber (PPC) once there is a micro opening though the thickness of the wafer during through-wafer silicon etching.

According to the representative cross-sectional geometry of the ICP etching tool as shown in Figure 1 at (Yang et al., 2006), to keep the temperature of the wafer at constant temperature when the wafer is under plasma processing conditions, the wafer needs to be cooled with HCG that is continuously cooling the wafer from the back side (i.e. the side of the wafer that is not exposed to the plasma processing) of the wafer. As long as the wafer does not have any "etched holes or channels through the entire wafer thickness", between the cooling side below the wafer and the plasma processing chamber side above the wafer, the wafer under plasma processing conditions is safely cooled while the entrance of the HCG leakage into the plasma chamber is also prevented.

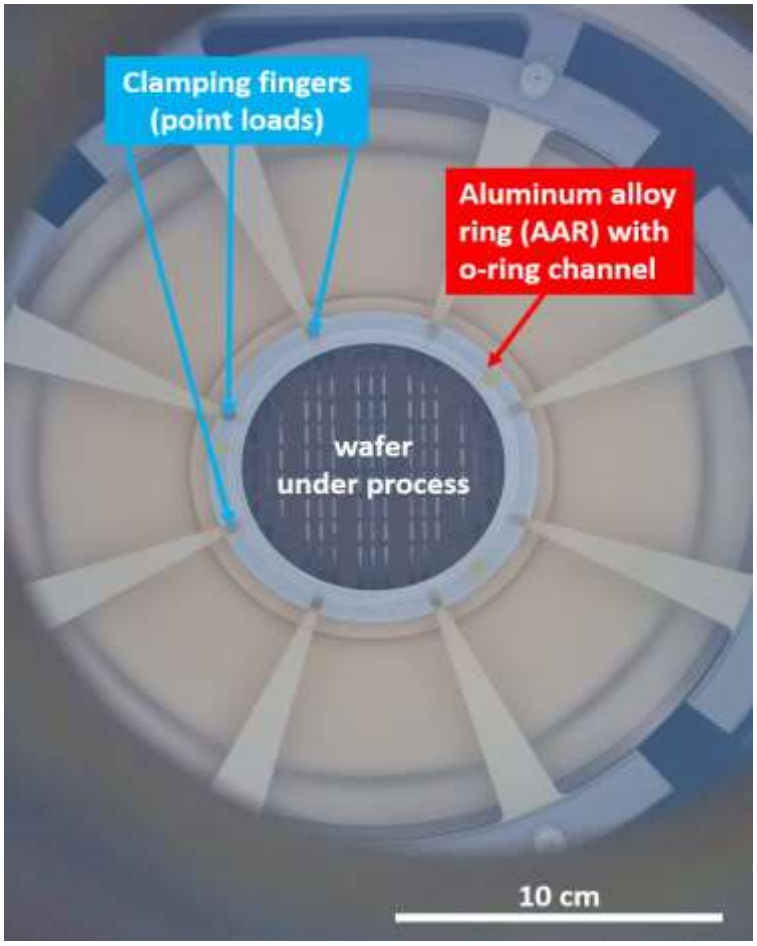


**Figure 2**. Aluminium alloy ring (AAR) with an o-ring channel. The o-ring channel (not visible in this view) is between the top surface of the wafer and back side of the AAR. O-ring channel is well aligned with the bottom o-ring (HCG gasket) shown in Figure. Well alignment between the o-ring channel and the bottom o-ring is important to minimize bending moment formation on the silicon wafer.

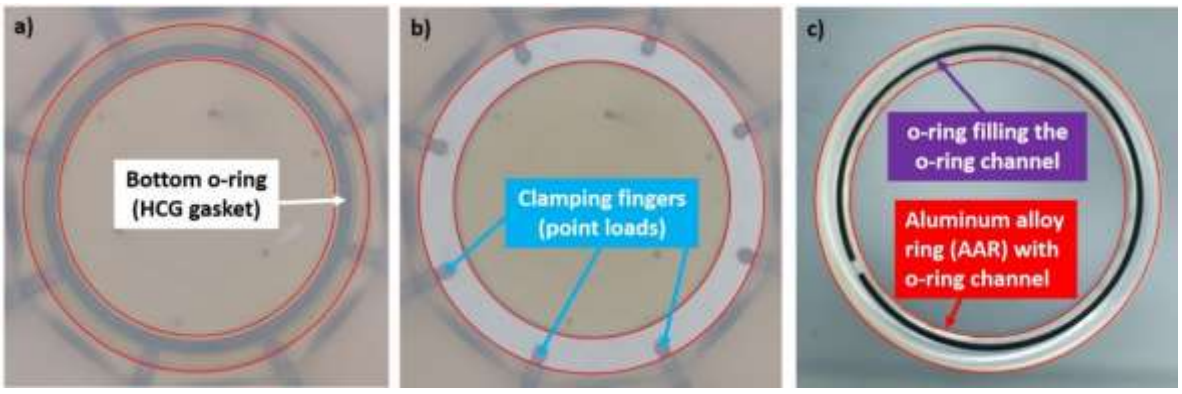


**Figure 1**. Aluminium alloy ring (AAR), and circular cross-section o-ring. The red colored circles in each image show the boundaries of AAR. a) To be able to see the position of the bottom o-ring (HCG gasket) with respect to the wafer and AAR, a transparent glass wafer is clamped with the 8 fingers of the ICP tool. b) AAR and the o-ring in the o-ring channel are positioned above the Pyrex glass wafer and below the 8 clamping fingers to uniformly distribute the point loads applied by the clamping fingers. c) At the back side of the AAR there is an o-ring channel for positioning of a circular cross-section o-ring.

However, after sufficient amount of plasma processing time of the silicon wafer, once a small through hole or a small through channel between the plasma processed (i.e. front) side and helium gas cooled (i.e. back) side of the wafer are not separated with a thickness of silicon material (Please see Figure 4 for the partially etched through wafer holes), the cooling gas can easily leak into the plasma process chamber and significantly affect the process conditions in an undesired way, if this gas leakage is not prevented. To prevent the passage of HCG

into the PPC, or to prevent the process chamber pressure from changing due to the small through holes or small through channels between the front side and back side of the wafer, a layer of material that can block the cooling gas from entering the plasma processing chamber may be prepared at the back side of the wafer. This layer of material must be strong enough to resist rupture of the layer of material. Furthermore, the layer of material must also be a reasonable conductor of heat (i.e. must have reasonably good thermal conductivity to allow the cooling of the wafer while the layer of material prevents the passage of HCG into the PPC). Good candidates for such purpose would be types of dicing tapes that can be safely removed from the wafer, after the completion of the through silicon wafer etching process. Hence, UV light sensitive dicing tapes such as ADWILL D-841 are good candidates for HCG leakage prevention.

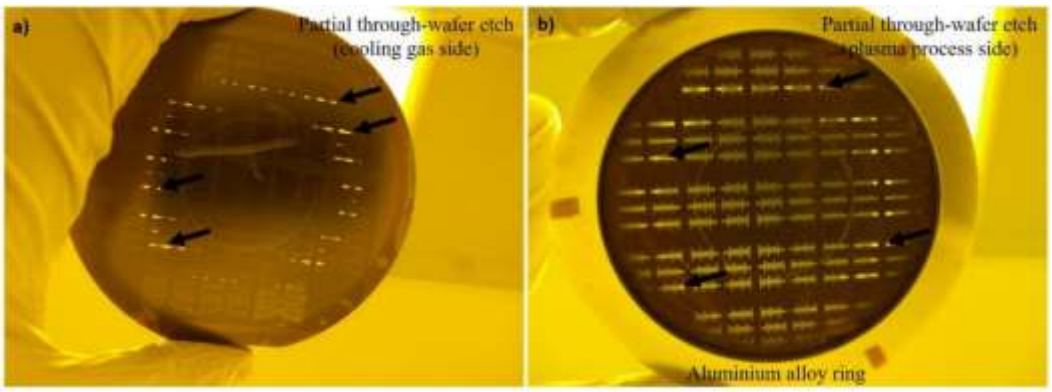


**Figure 2**. Partially completed though-wafer silicon etch. Black arrows show several of the fully etched locations. a) View from the cooling gas side (back side) of the wafer. This side of the wafer is covered with a dicing tape (UV sensitive ADWILL D-841) to prevent HCG from entering the PPC side. b) View from the PPC side (front side) of the wafer. This side of the wafer has patterned photoresist that is used to etch the plasma exposed silicon surface. AAR that is proposed in Section 2.1.2., is used to obtain minimized bending moment and uniformly distributed force on the edges of the wafer to prevent the breakage of the wafer.

**2.1.5. Photoresist and HMDS for photolithography**

Before plasma etching, for patterning of the silicon wafers various types of photoresists may be used. For example, for shallow depth silicon etching, AZ 5214E photoresist may be used, while for deep silicon etching or through wafer silicon etch processes, AZ 4562 photoresist may be used. Here it is important to emphasize that before spinning the photoresist, an adhesion layer between wafer and photoresist material, such as HMDS (hexamethyldisilazane), must be used to enhance the adhesion between photoresist and substrate surface.

**2.2. Methods**

**2.2.1. Dimension determination and manufacturing of the aluminium alloy ring (AAR) with a channel for circular cross-section o-ring**

The dimension determination approach for the dimensions of the AAR is based on the known diameter dimension of the silicon wafers that are used during the plasma etching process. It is well known that silicon wafers that are used in our research studies with the ICP etch tool in our cleanroom laboratory are either 4-inch diameter or 10 cm diameter. This wafer diameter information is used to calculate and obtain the rest of the dimensions for the AAR and the o-ring channel.

For clarity, Figure 5 a), b), and c) show the unedited versions of the images that are edited in Figure 5 d), e), and f). In Figure 5, red colored circles in d), e), and f) show the inner diameter and outer diameter on the AAR. In Figure 5, yellow colored circles in d), e), and f) show the inner diameter and outer diameter on the o-ring channel where the circular cross-section o-ring is planned to be assembled.

Starting from the diameter dimension (10 cm diameter) of a silicon wafer, the inner diameter and outer diameter of the AAR are calculated based on dimension scaling to calculate the dimensions given below:

1. Outer diameter of the AAR piece: 100 mm
2. Inner diameter of the AAR piece: 80 mm
3. Thickness of the AAR piece: 2.5 mm

Similarly, starting from the diameter dimension of a silicon wafer, the inner diameter and outer diameter of the o-ring channel inside the AAR are calculated based on dimension scaling to calculate the dimensions given below:

1. Outer diameter of o-ring between wafer and AAR piece: 88 mm
2. Inner diameter of o-ring between wafer and AAR piece: 84 mm
3. Depth of the o-ring channel: 1.3 mm

While determining the dimensions of the o-ring channel, it is paid attention to make sure that o-ring channel inside the AAR is well aligned with the bottom o-ring (gasket) that is used to seal the HCG from entering into the plasma processing chamber (Please see Figure 3 to remember where the bottom o-ring is located). To minimize the costs, it is also paid attention to make sure that the o-ring channel inside the AAR is easy to fill with

a commercially available circular cross-section o-ring which would not require customized o-ring material manufacturing. Furthermore, based on the careful measurements done of the ICP etch tool (i.e. maximum allowable wafer thickness inside the ICP process chamber is 9 mm) it is calculated that a thickness of 2.5 mm for the thickness of the AAR is sufficient to obtain uniformly distributed force distribution that is coming from the 8 point loads that are normally applied directly on the wafer surface by the alumina clamping fingers of the ICP etch tool.

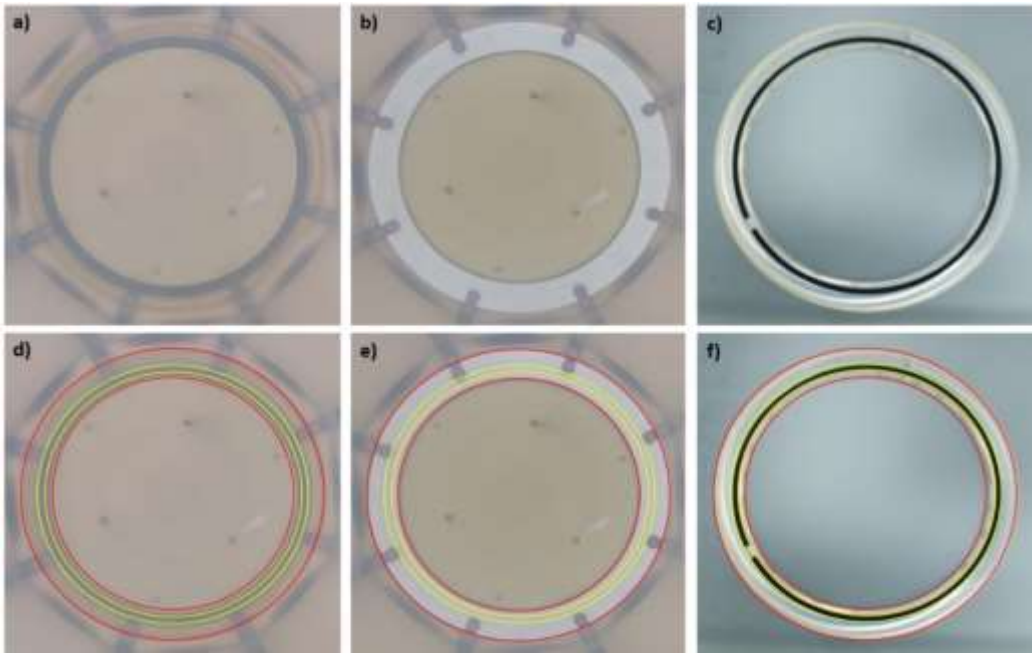


**Figure 5**. Description of the method used for the determination of the dimensions for the AAR, and o-ring channel. Sub figures a), b), and c) show the unedited versions of sub figures shown in d), e, and f). Red colored circles in sub figures d), e), and f) show the inner diameter and outer diameter on the AAR. Yellow colored circles in d), e), and f) show the inner diameter and outer diameter on the o-ring channel.

**2.2.2. Integrating the aluminium alloy ring (AAR), circular cross-section o-ring, wafer (substrate), and dicing tape**

After the preparation of the AAR with the o-ring channel, circular cross-section o-ring, wafer, and dicing tape, initially the dicing tape and the wafer are attached to each other. To attach the dicing tape to the back side of the wafer, well known protocols for the assembly of wafer and dicing tape are followed. After the assembly of wafer and dicing tape, the AAR with o-ring channel and circular cross-section o-ring are assembled as well. Next, these two assembled pairs are assembled to each other by aligning the AAR and the wafer till a good contact between the o-ring (NBR 70 SHORE) and the wafer is done. Finally, to keep the assembled components together, Kapton tape pieces are used to connect the top side of the AAR and bottom side of the wafer that has the dicing tape (Please see Figure 6 for the components assembled with Kapton tape pieces).

The o-ring (NBR 70 SHORE) with circular cross-section that is normally used for sealing purposes is used as a cushioning (i.e. spring and damper) material between the hard surfaces of the o-ring channel inside the AAR, and photoresist coated silicon wafer surface to prevent direct mechanical contact between the AAR and the photoresist coated silicon wafer surface. The o-ring inside the o-ring channel is also well aligned with the bottom o-ring (HCG gasket) to make sure that the bending moment on the clamped wafer is minimized to prevent wafer breakage. In addition, because of the manufacturing technology differences between the AAR and the very high precision manufacturing of a wafer compared to CNC milling, the o-ring is expected to help with uniform force balancing between the silicon wafer surface and the o-ring contact surface.

Furthermore, as stated before, to make sure that AAR and wafer do not move (i.e. slide) relative to each other, hence to prevent sliding of the AAR and the o-ring on the photoresist coated wafer surface, Kapton tape pieces that do not affect the plasma etch process are used to fix the AAR relative to the wafer edges (Figure 6).

Because of the manufacturing processes used for the manufacturing of the AAR and the o-ring channel at the AAR (i.e. regular CNC milling), it is assumed that there may be microscale aluminium alloy chips at the edges or milled surfaces of the AAR due to chip formation (i.e. chipping) during CNC milling. These chips are manually removed by medium grade sand paper processing of the sharp edges and surfaces of the AAR. Then, to remove any dust particles originating from sand paper processing, the AAR is washed multiple times in acetone and DI water while the AAR is kept inside a sonication bath.

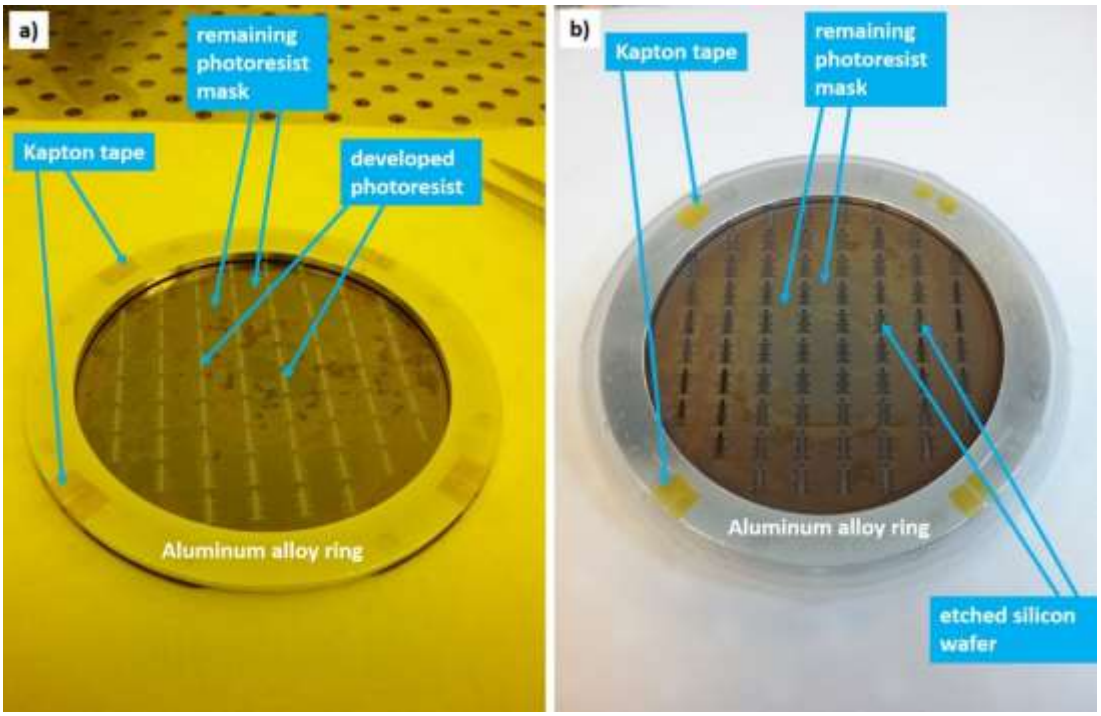


**Figure 6.** Aluminium alloy ring prevents wafer breakage during deep etch of silicon wafers. a) Using Kapton tape, the wafer, o-ring, and AAR are assembled together to prevent wafer breakage during deep silicon etching. b) Features that are significantly deeper than 50 micrometers are etched into the silicon wafer.

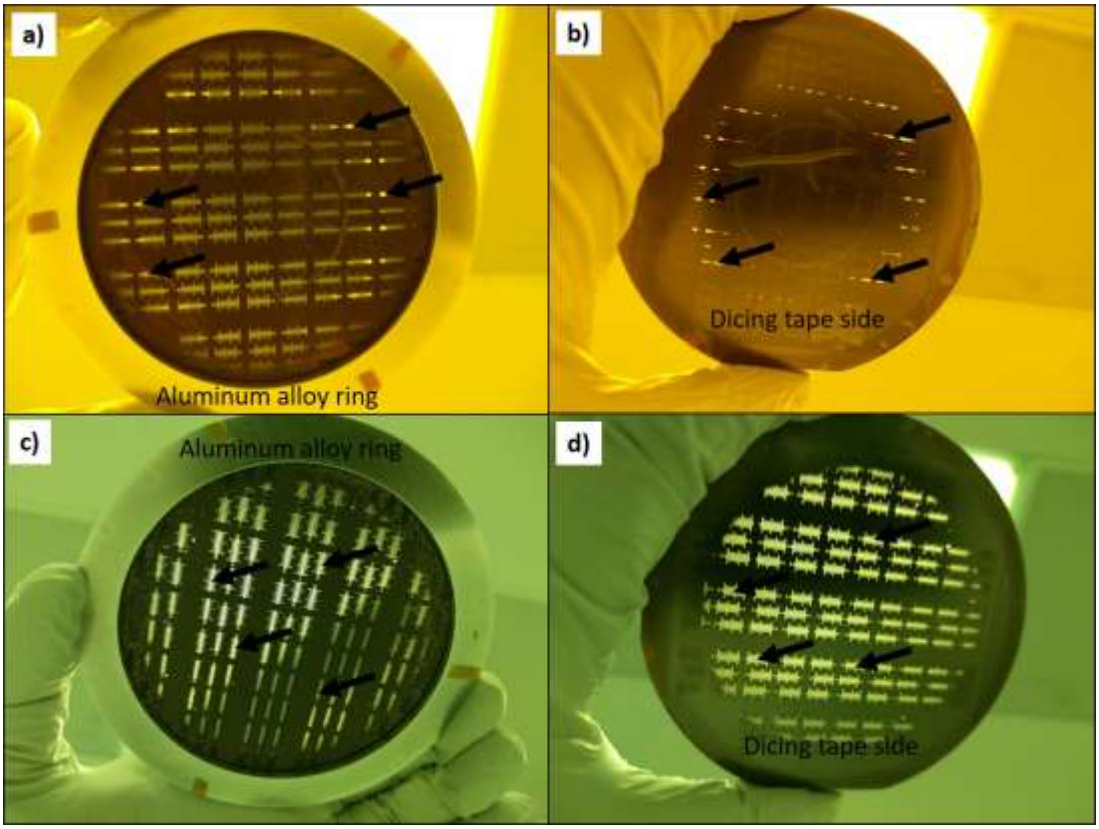


**Figure 7.** Demonstration of through-wafer silicon etch using the AAR to prevent wafer breakage and UV sensitive dicing tape to prevent HCG entrance into the process chamber side. a) black arrows show the through-wafer etched regions from the aluminium alloy side of the wafer at an early phase of the through-wafer etch process, b) black arrows show the through-wafer etched regions from the dicing tape side of the wafer, c) black arrows show the through-wafer etched regions from the aluminium alloy side of the wafer, d) black arrows show the through-wafer etched regions from the dicing tape side of the wafer.

## 3. Results

### 3.1. Applicability of the Aluminium Alloy Ring (AAR) for the Prevention of Wafer Breakage

Method #1 is successfully used to etch more than 50 micrometers deep or deeper features into silicon wafer as shown in Figure 6. With method #1, a rigid AAR that may significantly reduce the stress concentrations coming from individual clamping fingers is proposed. This way, the 8 clamping fingers from above are in direct contact with the AAR, and then the AAR is initially in contact with the o-ring and then the o-ring made from NBR 70 to prevent scratch formation and minimize bending moment is in contact with the wafer that needs to be etched.

Because the strength (i.e. bending stiffness) of a silicon wafer that is at least 500 +/- 25 micrometers thick is sufficient to withstand the point loads that are applied by the 8 clamping fingers of the original equipment manufacturer of the ICP tool, usage of the aluminium alloy ring may not be required for shallow silicon etching of about 50 micrometer deep features. However, silicon wafers with features that are etched deeper than 50 micrometer into the silicon wafers may need the usage of the aluminium alloy ring to prevent local stress formation at the sharp corners of the etched geometries on the surface and inside the wafer. Furthermore, when the etched features become deeper and deeper, the features etched into silicon start behaving as concentrated stress raiser regions. Furthermore, the 8 clamping fingers of the etch tool also behave as point-load stress inducers because the clamping force on the silicon wafer is not sufficiently uniformly distributed when only the 8 clamping fingers are used to clamp the wafers. Hence, when the stress inducers in the etched silicon wafers are combined with the point loads from the 8 clamping fingers, the wafers break prematurely inside the ICP chamber (Figure 1) hindering the completion of the microfabrication of the wafers with deep silicon etched features.

### 3.2. Applicability of the Combination of Aluminium Alloy Ring (AAR) and Back Side Dicing Tape for Prevention of Wafer Breakage and Allowing Through Wafer Etch At the Same Time

Method #2 is successfully used to etch through the thickness of a silicon wafer as shown in Figure 7. With method #2, different than what is proposed in method #1, addition of a layer of dicing tape is proposed to prevent HCG to enter into the PPC after there are features that are etched through the wafer.

While using method #2, 8 clamping fingers from above are in direct contact with the AAR, and then the AAR is initially in contact with the o-ring and then the o-ring made from NBR 70 is in contact with the wafer that needs to be etched. Additionally, the back side of the silicon wafer is coated with the dicing tape (ADWILL D-841) that prevents HCG from entering into the PPC after there are features that are etched through the wafer.

## 4. Discussion

As can be seen from the obtained results, the proposed methods that prevent wafer breakage (method #1, and method #2), and allow through-wafer etch (method #2) are very useful to extend the capabilities of an ICP tool if the resources to purchase a state-of-the-art equipment do not exist. Although, wafer breakage is prevented by adapting an AAR, using the AAR brings a limitation to be aware of: Normally, the wafer is 4-inch in diameter and this is the total workable area of a wafer if the capabilities of an ICP etch tool allows. However, because AAR also behaves as a mask during etching process, it is important to understand that not all the surface area of the wafer will be exposed to ICP etch process after adapting the AAR to the ICP etch process. Hence, there is a reduction in the total workable area of a 4-inch diameter wafer. In other words, the regions that are under the AAR would not be expected to have functional process results. According to the geometry of the AAR, the workable area of a 4-inch diameter wafer is reduced by 48%. Nevertheless, even if there is 48% reduction in the workable area of a 4-inch diameter wafer, by using the AAR, the process is safely completed on the silicon wafers to obtain the needed results or progress with the rest of the processes. So, rather than looking this 48% reduction in workable area, the researchers should be focused on available 52% workable area to obtain good process results. This 48% reduction in workable area may be unacceptable if the expected goal from the ICP tool is to increase throughput for high profit production studies. In such case, the ICP tool could be replaced with a state-of-the-art ICP etch tool that will cost extremely significant amount of money compared to the amount of money consumed to be able to use 52% workable area of a 4-inch diameter wafer with the already available ICP etch tool.

After the completion of a process that is using only AAR and o-ring (method #1) to have deep, but not through-wafer etch, features patterned into silicon wafer, AAR and o-ring are easily separated (disassembled) from the processed silicon wafer. From the other side, after the completion of a process that has the dicing tape at the back side of the wafer, it is important to do UV light exposure on the UV light sensitive dicing tape (ADWILL D-841) to be able to easily peel the dicing tape from the back side of the wafer. No wet etching process, or no other plasma processing is needed for the removal of the UV light exposed dicing tape. Simple mechanical peeling after UV light exposure is sufficient for the removal of the dicing tape from the wafer. If only mechanical peeling is not possible for reasons that may be related with the limitations of the wafer or the microfabrication process, the dicing tape may also be removed with oxygen plasma processing without exposing the wafer to wet processing conditions (A manuscript is in preparation about explaining the details of this process).

For applications where through wafer etch is performed, instead of using dicing tape types for the prevention of

HCG leakage into the PPC, a "carrier wafer" may be used instead of a dicing tape. However, using a "carrier wafer" may not be as effective as using a dicing tape unless good thermal contact between the "carrier wafer" and the wafer under through-wafer etching is satisfied. Hence, using dicing tape is advantageous compared to working with a "carrier wafer" that may serve the same purpose of preventing the leakage of HCG from the cooling chamber into the PPC.

Finite element modelling (FEM) may be done for more precise calculations. However, FEM modelling was not needed and was not performed for this study after observing that the encountered wafer breakage problems are resolved even without performing FEM modelling for the aluminium alloy ring, and o-ring structure that are used for uniform distribution of the point loads that are applied by the 8 clamping fingers of the ICP etching equipment.

## 5. Conclusion

Novel and capability enabling 2 different techniques that are extremely low-cost compared to purchasing a state-of-the-art ICP etch tool are presented to extend the processing capabilities of the ICP etch tool for deep silicon etching (method #1), and through wafer silicon etching (method #2).

These novel methods can be used, or adapted for use, with confidence on the ICP etch tools that have wafer clamping fingers to fix the position of wafers. Major advantages of the presented methods are:

1. to prevent wafer breakage by preventing crack initiation or crack propagation,
2. to enable process chamber cleanliness of ICP etch tools,
3. to allow using the already available process equipment without making significant money investment for a new process tool.

**Author Contributions**

The percentage of the author(s) contributions is presented below. The author reviewed and approved the final version of the manuscript.

| | M.Y. |
|---|---|
| C | 100 |
| D | 100 |
| S | 100 |
| DCP | 100 |
| DAI | 100 |
| L | 100 |
| W | 100 |
| CR | 100 |
| SR | 100 |
| PM | 100 |
| FA | 100 |

C=Concept, D= design, S= supervision, DCP= data collection and/or processing, DAI= data analysis and/or interpretation, L= literature search, W= writing, CR= critical review, SR= submission and revision, PM= project management, FA= funding acquisition.

**Conflict of Interest**

The author declared that there is no conflict of interest.

**Ethical Consideration**

Ethics committee approval was not required for this study because of there was no study on animals or humans.

**Acknowledgements**

TUBITAK (Scientific and Technological Research Council of Türkiye) is acknowledged for providing funds for this study under project number 115C117 of TUBITAK 2232 Program. This work was performed at National Nanotechnology Research Center (UNAM) at Bilkent University.

## References

Bonfim MJC, Swart JW, Velasco CEM, Okura JH, Verdonck PB. 1993. A low frequency remote plasma rapid thermal CVD system with face down electrostatic clamp wafer holder. In: Spring Meeting of the Materials Research Society, Symposium on Rapid Thermal and Integrated Processing II, April 12-15, San Francisco, CA, USA, 303: 407–412.

Brun XF, Melkote SN. 2009. Analysis of stresses and breakage of crystalline silicon wafers during handling and transport. Sol Energy Mater Sol Cells, 93 (8): 1238-1247.

Chen P-Y, Chen SL, Tsai MH, Jing MH, Lin T-C. 2007. Investigation of wafer strength in 12 inch bare wafer for prevent wafer breakage. In: Proceedings of IEEE Conference on Electron Devices and Solid-State Circuits, December 20-22, Tainan, Taiwan, pp: 545-548.

Chen P-Y, Tsai MH, Yeh WK, Jing MH, Chang Y. 2010. Relationship between wafer fracture reduction and controlling during the edge manufacturing process. Microelectron Eng, 87 (10): 1809-1815.

Chowdhury S, Wu Y, Shen L, McCarthy L, Parikh P, Rhodes D, Hosoda T, Kotani Y, Imanishi K, Asai Y, Ogino T, Kiuchi K. 2020. 5000+Wafers of 650 V highly reliable GaN HEMTs on Si substrates: wafer breakage and backside contamination results. In: 31st Annual SEMI Advanced Semiconductor Manufacturing Conference (ASMC), August 24-26, Saratoga Springs, NY, USA, pp: 3.

Corial. 2024. Deep reactive ion etching (DRIE). URL: https://corial.plasmatherm.com/en/technologies/drie-deep-reactive-ion-etching (accessed date: July, 09, 2024).

Izyumov M. 2009. An electrostatic clamp with temperature stabilization of semiconductor wafers under plasma treatment. Instrum Exp Tech, 52: 886-887.

Liu T, Su Y, Ge P. 2022. Breakage ratio of silicon wafer during fixed diamond wire sawing. Micromachines, 13(11): 1-13.

McLaughlin JC, Willoughby AFW. 1987. Fracture of silicon wafers. J Cryst Growth, 85(1-2): 83-90.

Meyer T, Petit-Etienne C, Pargon E. 2022. Influence of the carrier wafer during GaN etching in $Cl_2$ plasma. J Vac Sci Technol A, 40: 023202.

Nabavi R, Sarraf S, Soltanieh M. 2023. Optimization of hard anodizing process parameters on 6061-T6 aluminum alloy using response surface methodology. J Mater Eng Perform, 2023: 1-14. https://doi.org/10.1007/s11665-023-08717-4.

Noori Y, Skandalos I, Yan X, Zhelev N, Hou Y, Gardes F. 2024. Wafer bonding for processing small wafers in large wafer facilities. IEEE Trans Compon Pack Manuf Technol, 14 (2): 342-348.

Oxford Instruments. 2024. Inductively coupled plasma etching (ICP RIE). URL: https://plasma.oxinst.com/technology/icp-etching (accessed date: July, 09, 2024).

Plasma-Therm. 2024. Inductively coupled plasma (ICP) technology for etching high etch rates, process flexibility and reduced ion bombardment. URL: https://www.plasmatherm.com/process/etch/icp/ (accessed date: July, 09, 2024).

Saffar S, Gouttebroze S, Zhang ZL. 2015. Stress and fracture analyses of solar silicon wafers during suction process and handling. J Sol Energy Eng Trans-ASME, 137(3): 031010.

Sentech. 2024. Plasma etching. URL: https://www.sentech.com/products/plasma-process-technology/plasma-etching/ (accessed date: July, 09, 2024).

Silyb Wafer Services, Inc. 2023. What are the main causes of silicon wafer breakage? URL: https://www.silybwafers.com/what-are-the-main-causes-of-silicon-wafer-breakage (accessed date: July, 09, 2024).

SPTS. 2024. Plasma etch. URL: https://www.spts.com/categories/plasma-etch (accessed date: July, 09, 2024).

Wafer World Inc. 2021. Top causes of silicon wafer breakage. URL: https://www.waferworld.com/post/top-causes-of-silicon-wafer-breakage (accessed date: July, 09, 2024).

Yang Y-J, Kuo W-C, Fan K-C. 2006. Single-run single-mask inductively-coupled-plasma reactive-ion-etching process for fabricating suspended high-aspect-ratio microstructures. Jpn J Appl Phys, 45(1A): 305-310.

Zhou L, Qin F, Sun J, Chen P, Yu H, Wang Z, Tang L. 2015. Fracture strength of silicon wafer after different wafer treatment methods. In: 16th International Conference on Electronic Packaging Technology (ICEPT), August 11-14, Changsha, China, pp: 871-874.