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### Al/WO<sub>3</sub>/p-Si (MOS) Kapasitörlerde Arayüzey Durumları, Seri Direnç ve Bariyer Yüksekliğinin Frekansla Değişiminin İncelenmesi

### Ramazan LÖK

ÖZET:

#### Öne Çıkanlar:

- Elektiksel Karakterizasyon ve Frekans Etkisi: Al/WO3/p-Si (MOS) kapasitörün farklı frekanslardaki C-V ve G/w-V ölçümleri incelenmiş ve frekans arttıkça bu ölçümlerin maksimum değerlerinin azaldığı gözlemlenmiştir.
- Seri Direnç (Rs) ve Bariyer Yüksekliği: Seri direnç (R<sub>s</sub>) ve bariyer yüksekliğinin frekansla birlikte değişimi incelenmiş ve Rs'nin cihazın davranışını önemli ölçüde etkilediği gösterilmiştir.
- WO3 dielektrik sabiti 3688.75 olarak bulunmuştur.

## Anahtar Kelimeler:

- Yüksek K
- MOS
- WO<sub>3</sub>
- Bariyer Yüksekliği

## Seri Direnç Etkisi

### üzerinde sentezlenmiştir. Al/WO<sub>3</sub>/p-Si (MOS) kapasitör elektriksel karakterizasyonu, farklı frekanslarda (50 kHz'den 1 MHz'e kadar) kapasite-voltaj (C-V) ve iletkenlikvoltaj (G/w-V) ölçümleri ile gerçekleştirilmiştir. Uygulanan voltaj frekansı arttıkça, ölçülen C-V ve G/@-V karakteristiklerinin maksimum değerleri azalmıştır. Bu olgu, arayüzey durumu tuzak (Dit) yüklerinin düşük frekanslı AC voltaj sinyallerini takip etmesine bağlanmıştır. Seri direnç ( $R_s$ ) ve bariyer yüksekliğinin ( $\Phi_B$ ) frekansla değişimi incelenmiştir. $R_s$ 'in cihaz davranışını önemli ölçüde etkilediği gösterilmiştir. $\Phi_B$ de artan frekansla azalmıştır. Bu davranışın, Vo değerini doğrudan etkilerken yük taşıyıcılarının hareketliliğini dolaylı olarak etkilediği öne sürülmüştür. Sonuç olarak, WO3 malzemesi dielektrik özellikler açısından değişken sonuçlar sergilemesine rağmen, çalışmanın yüksek dielektrik sabiti (örneğin, 3688.75) bulgusu literatürdeki benzer sonuçlarla tutarlıdır. Bu yüksek dielektrik özelliği, malzemenin gelecekteki uygulamalar için önemini vurgulamaktadır.

Çalışmada, Tungsten oksit (WO3), sol-jel yöntemiyle P-tipi (100) silisyum plakası

### Investigation of Interface States, Series Resistance and Barrier Height Variation with Frequency in Al/WO<sub>3</sub>/p-Si (MOS) Capacitors

**ABSTRACT:** 

#### **Highlights:**

- Electrical Characterization and Frequency Effect: The C-V and G/ω-V measurements of the Al/WO<sub>3</sub>/p-Si (MOS) capacitor at different frequencies were examined, and it was observed that the maximum values of these measurements decreased as the frequency increased
- Series Resistance (R<sub>s</sub>) and Barrier Height: The variation of series resistance (Rs) and barrier height with frequency was examined, and it was shown that Rs significantly affects the device behaviour.
- The dielectric constant of WO3 was found to be 3688.75

## Keywords:

- High K
- MOS
- WO<sub>3</sub>
- Barrier Height
- Series Resistance Effects

In the study, Tungsten oxide (WO<sub>3</sub>) was synthesized via the sol-gel method on P-type (100) silicon wafer. Electrical characterization of the Al/WO<sub>3</sub>/p-Si (MOS) capacitor was performed through capacitance-voltage (C-V) and conductance-voltage (G/ω-V) measurements at different frequencies (from 50 kHz to 1 MHz). As the applied voltage frequency increased, the maximum values of the measured C-V and  $G/\omega$ -V characteristics decreased. This phenomenon was attributed to interface state trap (Dit) charges following low-frequency AC voltage signals. The variation of series resistance  $(R_s)$  and barrier height  $(\Phi_B)$  with frequency was examined. It was shown that Rs significantly affects the device behaviour. The  $\Phi_B$  also decreased with increasing frequency. This situation is suggested to indirectly affect the mobility of charge carriers directly through the Vo value. Ultimately, although WO<sub>3</sub> material exhibits variable results in terms of dielectric properties, the study's finding of a high dielectric constant (e.g., 3688.75) is consistent with similar results in the literature. This high dielectric property underscores the material's importance for future applications.

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Investigation of Interface States, Series Resistance and Barrier Height Variation with Frequency in Al/WO<sub>3</sub>/p-Si (MOS) Capacitors

## **INTRODUCTION**

The MOS capacitor (Metal-Oxide-Semiconductor Capacitor) is known as a fundamental building block in modern semiconductor technology and plays a decisive role, especially understanding operating principles of integrated circuits and devices such as MOSFETs (Metal-Oxide-Semiconductor Field-Effect Transistors)(Bentarzi, 2011; Ytterdal et al., 2003). This capacitor is made up of three main components: metal electrode (gate), an insulating oxide layer (usually silicon dioxide), and a semiconductor (typically p-type or n-type silicon). Key variables such as the applied voltage, semiconductor type, and doping concentration closely influence the electrical properties of MOS capacitors. This situation causes the capacitance of the device to differ in various operating regions. Under varying voltages, the MOS capacitor exhibits three main states: accumulation, depletion, and inversion. Each of these states directly affects the operation of MOSFETs and, consequently, the performance of digital and analogue electronic circuits. Furthermore, MOS capacitors are crucial tools in the optimization of semiconductor manufacturing processes, as they are used to evaluate the thickness of the gate oxide and the quality of the semiconductor surface(Lee et al., 2024; S. S. Li & Li, 1993; Malta et al., 2024; Silva et al., 2024). Additionally, an important point to add to this assessment is that ohmic and rectifying contacts are critical components that determine the operating principles of semiconductor devices. Ohmic contacts provide low-resistance conductivity, while rectifying contacts control the direction of current. These two types of contacts play a critical role in the design of electronic circuits. In order to form a rectifying contact between a P-type semiconductor and metal, the work function of the metal must be smaller than that of the semiconductor. That is, in this case, it must be  $\phi_s > \phi_m$ . When this condition is met, hole flow occurs from the metal into the semiconductor. Consequently, an electric field is created at the metal's surface, and current flows in only one direction (from the metal to the semiconductor)(Tan, 2018). For the formation of back ohmic contact in P-type semiconductors, the work function of the metal must be greater than that of the semiconductor:  $\phi_m > \phi_s$ . In this case, current can flow freely in both directions, providing a low-resistance contact. In N-type semiconductors, the formation of a rectifying contact requires that the work function of the metal is greater than that of the semiconductor:  $\phi_m > \phi_s$ . Here, free electron flow occurs from the metal into the semiconductor, allowing current to flow in only one direction (from the metal to the semiconductor). For the formation of ohmic contacts in N-type semiconductors, the work function of the metal must be smaller than that of the semiconductor:  $\phi_s > \phi_m$ . When this condition is met, current can flow freely in both directions(Rideout, 1975; Taşçıoğlu et al., 2023; Tucci et al., 2011).

(WO<sub>3</sub>), transition metal oxide, widely used in various applications. (WO<sub>3</sub>) has a band gap of 2.6-3.0 eV and a work function of 6.2 eV(Adhikari et al., 2022; Thummavichai, 2018). Recent research on WO<sub>3</sub> has attracted significant interest, particularly due to its electrochromic properties. Electrochromic materials can change colour when a voltage is applied, making them ideal for various innovative technologies. Tom Rocca and his colleagues have compared the "reversible electrochromic reduction of transparent nanostructured  $\gamma$ -WO<sub>3</sub> thin films" and suggested that their work paves "the way for the rational development of electrolytes and active materials for" various water-based devices, such as energy-saving smart windows(Rocca et al., 2024). Cong-Cong Huang and colleagues synthesized WO<sub>3</sub> using microwave irradiation and used it as an electrode material in supercapacitors. This can be considered as evidence that the WO<sub>3</sub> material has a wide range of potential applications.(Huang et al., 2009). WO<sub>3</sub> is known for its high gas sensing sensitivity, making it ideal for detecting and monitoring environmental gases. Zhang and others synthesized a gas sensor based on

monoclinic phase WO<sub>3</sub>, demonstrating that This sensor could detect NO<sub>2</sub> with higher sensitivity and selectivity under visible light at temperatures between 20 and 25 degrees (Zhang et al., 2013).

Beyond these areas, the use of  $WO_3$  continues to expand, and new application fields are being discovered. Developments in nanotechnology and materials science, in particular, further enhance the potential of  $WO_3$  and offer innovative solutions(X. Li et al., 2024; Nabeel et al., 2023; Santos et al., 2015; Zheng et al., 2011).

The main objective of the study is to determine how the electrical properties of Al/WO<sub>3</sub>/p-Si (MOS) capacitors change with frequency and to reveal the impact of these changes on the overall performance of the device. The research focuses on critical parameters such as  $R_s$ ,  $\Phi_B$ , and  $D_{it}$ , which directly affect the performance and efficiency of the device. While previous studies generally concentrated on the structural and electrochemical properties of WO<sub>3</sub>, this study emphasizes the variations in electrical performance within MOS capacitors. The analysis of Rs,  $\Phi_B$ , and  $D_{it}$  using C-V and G/ $\omega$ -V measurements distinguishes this work, highlighting the potential of WO<sub>3</sub> in high-frequency applications.

As a result, the findings demonstrate how the Al/WO<sub>3</sub>/p-Si (MOS) capacitor responds to changes in frequency and how these behaviours reflect on the device's performance. This data provides a valuable foundation for future design and optimization studies, aiding in ensuring that the device operates more efficiently and stably.

## MATERIALS AND METHODS

Solution Preparation: To prepare a pure tungsten oxide solution, 1 gram of  $WC_{16}$  (tungsten hexachloride) was incorporated into 10 ml of ethanol (C<sub>2</sub>H<sub>5</sub>OH) with continuous mixing. Within the first 2-3 minutes of the reaction, the solution quickly turned from yellow to dark blue due to the reduction of  $W^{6+}$  ions to  $W^{5+}$  ions by the ethanol. After some time, the dark blue solution became homogeneous and transparent. The reaction mechanism is given equation 1:

 $WC_{16} + C_2H_5OH \rightarrow WC_{16}-x(OC_2 H_5 )x + HCl$ 

(1)

Film Production: To produce WO<sub>3</sub> thin films, p-type (100) silicon substrates with a resistivity of 1-4 $\Omega$  and a thickness of 500 $\mu$ m were cleaned using the standard Radio Corporation of America (RCA) cleaning process. The cleaned substrates were dipped into the prepared solution four times to coat them with a thin film. The coated films were then annealed at 500°C.

Formation of the MOS Structure: The annealed thin film structure was placed in a sputter system and subjected to vacuum processing at  $6x10^{-4}$  Pascal. Front and back metal contacts were made, converting to the Al/WO<sub>3</sub>/p-Si (MOS) capacitor. Investigation of Electrical Properties: To examine the electrical properties of the produced MOS capacitor, measurements were taken at different frequencies (50 kHz and 1000 kHz) using the Keithley 4200 system semiconductor characterization system.

# **RESULTS AND DISCUSSION**

Figure 1 provides a detailed view of the frequency-dependent capacitance-voltage (C-V) characteristics of the Al/WO<sub>3</sub>/p-Si (MOS) capacitor, under a voltage bias varying from -3 V to +3 V, across a frequency range of 50 kHz to 1 MHz. The data in Figure 1 provides a detailed analysis of the device's performance and electrical properties at different frequencies. The MOS device exhibits three different regimes (i.e., inversion, accumulation, and depletion) and shows p-type characteristics. It has been detected that as the frequency increases, the capacitance values decrease. The main reason for this

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is that the interface states respond more to AC signals at lower frequencies. This situation will be examined in more detail in the following sections.

Oxide capacitance ( $C_{ox}$ ) refers to the capacitance of the oxide layer in a MOS capacitor. This capacitance determines the dielectric properties and overall electrical behaviour of the capacitor. Factors such as the thickness of the oxide layer, the dielectric constant, and the surface area of the capacitor are important parameters that affect the value of  $C_{ox}$ . Based on this capacitance value, the dielectric constant of the materials can be calculated from Equation 2. (Morkoc et al., 2019)

$$\varepsilon_i = \frac{c_{ox} d}{A\varepsilon_0} \tag{2}$$

Here, A (1.7671 x 10<sup>-6</sup> m<sup>2</sup>) is the capacitor area, and  $\varepsilon_0$  (8.85 x 10<sup>-12</sup> F.m<sup>-1</sup>) is the vacuum permittivity. As can be understood from the SEM image in Figure 2, d<sub>i</sub> is approximately (1.12 µm), which is the oxide thickness between the metal and semiconductor layers, and  $\varepsilon_i$  is the dielectric permittivity of the oxide



Figure 1. The Capacitance–Voltage (C–V) curves of Al/WO<sub>3</sub>/p-Si (MOS) Capacitor for the Different Frequencies

 $C_{ox}$  value was determined from measurements taken at 1 MHz in a strong accumulation region, as shown in Figure 1, and was found to be approximately  $Cox\approx 5.13 \times 10^{-8}$  F. The calculated dielectric constant is found to be 3688,75. It is emphasized in the literature that the  $\varepsilon_i$  of WO<sub>3</sub> can vary depending on temperature, frequency, and measurement conditions. However, as in many research studies, these values are normal for WO<sub>3</sub> (Gowtham et al., 2021; Hirose & Furukawa, 2006; Nabeel et al., 2023).



Figure 2. Cross-Section Morphology of the WO3 on Si After Annealing 500 °C

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In addition to the  $C_m$ –V curves shown in Figure 1, the  $G_m/\omega$ –V curve of the Al/WO<sub>3</sub>/p-Si (MOS) capacitor increases with increasing frequency in Figure 3. The conductance-voltage curve is an important parameter used to evaluate the interface quality of MOS capacitors. Due to the application of a weak A.C. signal between the terminal ends of the MOS capacitor, the conductivity resulting from the interaction of interface states and majority carriers corresponds to the highest conductivity value for each frequency, at the minimum capacitance value. Additionally, it has been identified that the G/ $\omega$ –V values measured at different frequencies shift to more negative values on the voltage axis as the frequency increases. Under normal conditions, the  $G_m/\omega$ –V values are expected to give an imperfect Gaussian curve. However, a peak point was not observed in all measurements except at 750 kHz and 1000 kHz. While there could be many reasons for this behaviour, it can be mainly attributed to three factors. First, the series resistance effect originating from the backside contact points of the silicon layer of the MOS capacitor; second, the interface dielectric layer; and finally, the relaxation time of the interface states(Caban-Zeda, 1969; Cristoloveanu & Li, 2013; Pande et al., 2020)



Figure 3. Conductance–Voltage (G–V) Curves of the Al/WO<sub>3</sub>/p-Si (MOS) Capacitor at Various Frequencies

Figure 4 illustrates the series resistance ( $R_{smax}$ ) values of the device plotted against voltage at different frequencies. The  $R_s$  values were determined using the method proposed by Nicollian and Goetzberger, calculated from equation 3. The series resistance effect significantly impacts the device's performance and is crucial for optimizing the device's functionality in practical applications (Çetinkaya et al., 2024; Lok et al., 2016)

$$R_S = \frac{G_m}{G_m^2 + \omega^2 C_m^2} \tag{3}$$

where  $C_m$ ,  $G_m$ , and  $\omega$  are the measured capacitance, conductance, and angular frequency measured in strong accumulation regions. As illustrated in the figure, it is clear that that  $R_s$  in the device is higher at lower frequencies. The observed effect can be ascribed the response of the interface states to the AC signal.

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Figure 4. The Max Series Resistance Values Al/WO<sub>3</sub>/p-Si (MOS) Capacitor for the Different Frequencies

In other words, the presence of frequency-dependent charges trapped at the interface results in additional capacitance at low frequencies due to their easy response to the AC signal. Therefore, it is evident that the  $R_s$  effect is one of the main reasons for the changes in the  $C_m$ –V and  $G_m$ –V curves(Lok et al., 2016; Taşci, 2023).

$$C_{c} = \frac{\left(G_{m}^{2} + \omega^{2}C_{m}^{2}\right)C_{m}}{a^{2} + \omega^{2}C_{m}^{2}}$$
(4)

$$G_{c} = \frac{\left(G_{m}^{2} + \omega^{2}C_{m}^{2}\right)a}{a^{2} + \omega^{2}C_{m}^{2}}$$
(5)

$$a = (G_m) - [(G_m)^2 + (\omega C_m)^2] R_s$$
(6)

The corrected capacitance-voltage ( $C_C$ -V) and corrected conductance-voltage ( $G_C$ / $\omega$ -V curves are shown in Figures 6 and 7. These values have been calculated sequentially from equations 4 and 5. Parameters such as  $G_m$ ,  $C_m$ ,  $R_s$ , and  $\omega$  have been previously defined. When comparing the measured capacitance and conductance curves with the corrected ones, although no significant changes are observed in the conductance-voltage curve, there has not been a large change in the capacitance values.



Figure 5. Equivalent Circuit Capacitance for a Mos Capacitor (a) Low Frequency (b) High Frequency

In the accumulation region, the capacitance values for 1 MHz are  $C_m = 5.20 \times 10^{-8}$  F, while the corrected capacitance value  $C_c = 5.34 \times 10^{-8}$  F shows an increase. The literature indicates that the

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largest error in capacitance has been reported to occur in the accumulation and a portion of the depletion region (Lok et al., 2016). When comparing Figure 1 with Figure 5, the expected behaviour in both graphs is a decrease in capacitance values with increasing frequency.

Upon examining the reasons for these changes, it is evident that this is due to the series resistance effect. This behaviour can be explained by the equivalent circuit diagram presented in Figure 5. At low frequencies, interface levels do not have enough time to follow the applied AC voltage signal. This can lead to the formation of  $C_{it}$  capacitance.  $C_{it}$  can contribute to the equivalent capacitance by adding to the space charge capacitance ( $C_{sc}$ ) and oxide capacitance, thus increasing the equivalent capacitance (Güçlü et al., 2024).



Figure 6. The Corrected Capacitance–Voltage (C–V) curves of Al/WO<sub>3</sub>/p-Si (MOS) capacitor



Figure 7. The Corrected Capacitance–Voltage (G<sub>c</sub>/ $\omega$ –V) Curves of Al/WO<sub>3</sub>/p-Si (MOS) Capacitor

When compared between Figure 3 and Figure 7, it was noted that peaks were observed at frequencies of 750 kHz and 1000 kHz in the  $G_m/\omega$ -V curves, while no peaks were observed at other frequencies. After correction, as can be seen from Figure 7, peaks have been observed. Additionally, in both the measured conductance voltage and corrected conductance voltage graphs, it has been identified that that the maximum conductance value decreases as the frequency increases, as expected. The conductance curves have increased from  $3.7 \times 10^{-9}$  to  $1.6 \times 10^{-8}$  after correction at 1 MHz. As previously mentioned, conductance curves are affected more significantly than capacitance curves because conductance reflects the dynamic response of interface traps. As these traps capture and

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release charge carriers, they cause fluctuations in conductivity, which can explain the variations in the conductance curves. Additionally, as the frequency of the AC signal changes, the response time of the traps also varies, affecting the conductance values (Mutale et al., 2021). Capacitance, on the other hand, is more related to a stable charge distribution, making it less sensitive to such fluctuations. Consequently, the greater impact on conductance curves may be related to interface traps, relaxation time, and the frequency of the AC signal (Kaymak et al., 2020; Tataroğlu & Altindal, 2008) sensitive to such fluctuations. Consequently, the greater impact on conductance curves may be related to interface traps, relaxation time, and the frequency of the AC signal (Kaymak et al., 2020; Tataroğlu & Altindal, 2008) sensitive to such fluctuations. Consequently, the greater impact on conductance curves may be related to interface traps, relaxation to such fluctuations.

The interface states are a critical parameter for the performance of MOS capacitors. The frequency-dependent interface state density was calculated using the Hill-Coleman method with the following equation:

$$D_{it} = \frac{2}{Aq} \frac{G_{c,max} / \omega}{\left(G_{c,max} / \omega C_{ox}\right)^2 + \left(1 - C_c / C_{ox}\right)^2} \tag{7}$$

Here, q denotes the electronic charge, A represents the area of the capacitor,  $C_{ox}$  refers to the capacitance in the accumulation region,  $G_{c,max}/\omega$  indicates the peak value of the corrected conductance, and  $C_c$  is the capacitance value associated with this peak conductance.

The frequency-dependent interface state density was calculated for different frequencies and is shown in Figure 8. The  $D_{it}$  value is expected to decrease as the frequency increases. The calculated values decrease with increasing frequency, consistent with the literature. However, in the literature,  $D_{it}$  values range between  $10^{10}$  and  $10^{12}$  eV<sup>-1</sup>.cm<sup>-2</sup>. A value on the order of  $10^{12}$  eV<sup>-1</sup>.cm<sup>-2</sup> indicates a high interface state density. This can be attributed to a different relaxation time-dependent acceptor-/donor-like interface states and It may also be due to the manufacturing process.



Figure 8. Variations of D<sub>it</sub> as a Function Voltage Al/WO<sub>3</sub>/p-Si/Al (MOS) Capacitor

Another important parameter is the barrier height which was figure out from the linear portion of the  $C^{-2}$ -V curve shown in Figure 9. The capacitance of depletion regions calculated Equation.8 (Yeriskin, 2019)

$$c^{-2} = 2(V_0 + V)/\varepsilon_i \varepsilon_0 q A^2 N_a \tag{8}$$

Here, V is the applied voltage, Na is the carrier concentration, and  $V_0$  is the point where the linear lines in Figure 9 intersect the x-axis.  $V_0$  is expressed by the following equation

$$V_0 \quad (=V_D - k_B T/q) \tag{9}$$

Temperature in Kelvin, denoted by T, is used to define the Boltzmann constant,  $k_B$ . In MOS capacitors, the barrier height represents the magnitude of the energy barrier between the metal and the

semiconductor. This barrier can significantly affect the electrical properties and performance of the device (Ocak et al., 2010; Sevgili et al., 2022). It can be calculated using Equation 10.

$$\Phi_B = V_0 + \frac{kT}{q} + E_F - \Delta \Phi_B = V_D + \frac{kT}{q} ln \left(\frac{N_v}{N_a}\right) - \Delta \Phi_B$$
(10)



**Figure 9**. C<sup>-2</sup> –V Characteristics and Corresponding Linear Fit Function of Al/WO<sub>3</sub>/p-Si (MOS) Capacitor at Various Frequencies from 50 kHz to 1 MHz

The expression  $E_F$  denotes the energy difference between the bulk Fermi level and the valence band edge. N<sub>v</sub> refers to the effective density of states in the valence band.  $(\Delta \Phi_B = \sqrt{qE_m/(4\pi\varepsilon_i\varepsilon_0)^{-1}})$  represents the barrier potential, where  $E_m$  is the maximum electric field.

	-	-				
F(kHz)	V <sub>d</sub> (eV)	$N_A x 10^{16} (cm^{-3})$	E <sub>F</sub> (eV)	E <sub>m</sub> x10 <sup>5</sup> (V/cm)	$\Phi_{B(C-V)}(eV)$	$\Delta \Phi_{B(C-V)} (eV)$
50	1.40	8.12	0.1491	2.17	1.37	0.1882
100	1.31	7.26	0.1520	1.98	1.28	0.1800
250	1.14	6.86	0.1535	1.80	1.13	0.1714
500	1.06	6.43	0.1551	1.68	1.06	0.1656
750	0.95	6.11	0.1565	1.55	0.95	0.1591
1000	0.91	6.20	0.1561	1.53	0.91	0.1580

Table 1. Some Important Electrical Properties Calculated for the Al/WO3/p-Si (MOS) Capacitor.

As depicted in Table 1, the barrier height ( $\Phi_B$ ) shows a decreasing trend as anticipated with frequency dispersion. However, a deceleration in the rate of this change with increasing frequency has been noted. At high frequencies, the impact of the applied electric field within the dielectric material is intensified. This can enhance the movement of carriers within the dielectric material. The increased mobility of charge carriers can result in a decrease in barrier height (Fiorenza et al., 2018). Finally, an increase in frequency has resulted in a decrease in the V<sub>0</sub> value. However, this has directly contributed to the decrease in barrier height. In addition, the frequency-dependent behaviour of the trap charges in the acceptor-donor type interface states may also have had an effect (Hazell, Simmons, Evans, & Blaauw, 1998; Raymond T. Tung, 2014; R. T. Tung, 1992)

## CONCLUSION

In this study, WO<sub>3</sub> was synthesized on a P-type  $\langle 100 \rangle$  silicon wafer using the sol-gel method. Significant reductions in the capacitance values of the Al/WO<sub>3</sub>/p-Si (MOS) capacitor was observed with increasing frequency. This observation is directly related to the interface trap charges that follow the AC voltage signals. The study also examined the frequency dependence of the R<sub>s</sub> and  $\Phi_B$ . It was found that Rs significantly affects the device's behaviour. Additionally, it was noted that the  $\varphi_B$  decreases with increasing frequency. This decrease is suggested to indirectly affect the mobility of charge carriers through the V<sub>0</sub> value.

As a result, although the WO<sub>3</sub> material shows variable results in terms of dielectric properties, the finding of a high dielectric constant (e.g., 3688.75) in the study is consistent with similar results found in the literature. This high dielectric property underscores the importance of the material for future applications. The high dielectric constant of WO<sub>3</sub> highlights its potential for use in energy storage, capacitors, and other dielectric applications. Therefore, these properties make WO<sub>3</sub> a significant candidate for future technological applications.

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