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A Cost-Effective and High-Efficiency Novel 15-Level Hybrid MLI Topology for Renewable Energy Systems

Murat KARAKILIÇ[1*] Hasan HATAŞ[2]

[1] *Iğdır University, Faculty of Engineering, Department of Computer Engineering, Iğdır, Turkey*

[2] *Van Yüzüncü Yıl University, Faculty of Engineering, Department of Electrical and Electronics Engineering, Van, Turkey*

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Graphical/Tabular Abstract (Grafik Özet)

This paper introduces a new hybrid MLI structure with a single DC source, 15-level output and 96.48% efficiency. The structure provides high performance with low THD (1.41%) and a small transformer. / Bu çalışma, tek DA kaynaklı, 15 seviyeli çıkış veren ve %96,48 verimle çalışan yeni bir hibrit ÇSE yapısı sunar. Yapı, düşük THB (%1,41) ve küçük transformatörle yüksek performans sağlar.

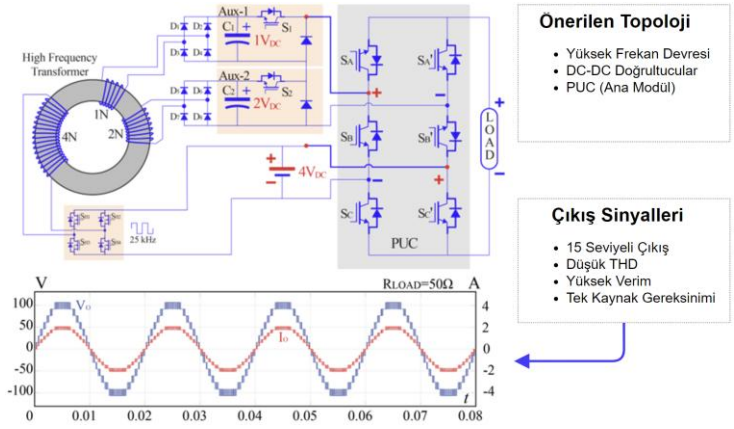

***Figure A**: Graphical representation of the proposed topology **Şekil A:** Önerilen topolojinin grafik gösterimi*

Highlights (Önemli noktalar)

- *The proposed structure introduces a hybrid inverter that generates 15-level output with a single DC source. / Önerilen yapı, tek DA kaynak ile 15 seviyeli çıkış üretebilen hibrit bir evirici sunar.*
- *Low cost and compact size are achieved through the high-frequency transformer. / Yüksek frekans transformatörü sayesinde düşük maliyet ve küçük boyut avantajı sağlar.*
- *Total harmonic distortion is reduced to a low level of 1.41%. / Toplam harmonik bozulma %1,41 gibi düşük bir seviyeye indirgenmiştir.*
- *High efficiency (96.48%) improves system performance. / Yüksek verim (%96,48) ile sistem performansı artırılmıştır.*
- *An economical solution is achieved using only 8 semiconductor devices with the PUC structure. / PUC yapısı ile sadece 8 yarı iletken cihaz kullanılarak ekonomik çözüm elde edilmiştir.*

***Aim (Amaç):** To develop a cost-effective, high-performance multilevel inverter structure using a single DC source and hybrid topology. / Tek bir DA kaynak ve hibrit topoloji kullanarak ekonomik ve yüksek performanslı çok seviyeli bir evirici yapısı geliştirmek.*

***Originality (Özgünlük):** This study introduces a novel hybrid approach combining switched diode and high-frequency link structures to feed a PUC-based inverter from a single DC source. / Bu çalışma, tek bir DA kaynaktan PUC tabanlı eviriciyi beslemek için anahtarlamalı diyot ve yüksek frekans bağlantı yapısını birleştiren özgün bir hibrit yaklaşım sunar.*

***Results (Bulgular):** The proposed inverter achieves 15-level output with 1.41% THD, 96.48% efficiency, and reduced transformer size and cost. / Önerilen evirici, %1,41 THB, %96,48 verim ile 15 seviyeli çıkış üretmiş ve transformatör boyutu ile maliyetini azaltmıştır.*

***Conclusion (Sonuç):** The presented structure provides a simplified, efficient, and scalable solution for multilevel inverter applications using minimal components. / Sunulan yapı, az sayıda bileşenle çok seviyeli evirici uygulamaları için sade, verimli ve ölçeklenebilir bir çözüm sunar.*

*Corresponding author, e-mail: murat.karakilic@igdir.edu.tr
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Abstract

This study proposes a new hybrid model for single DC source multilevel inverters (MLIs). The recommended switched diode (SD) and high frequency link (HFL) hybrid structure utilizes one single DC source voltage and supplies multiple DC voltages to the Packed U-Cell (PUC) circuit. The MLI generates 15 levels at the output signal using only 8 semiconductor devices. This simplifies the control of the system and provides an economic solution with a low cost function (CF) of 2.71. In addition, a detailed comparison with recent studies in the literature has been made. Unlike several other studies, the HFL approach is used for the voltage gain. Most of the current supplying the load is obtained directly from the DC supply source, while only a limited current element is transmitted through the high-frequency transformer. This significantly reduces transformer size and costs. In tests with inductive loads, the output is near pure sinusoidal like waveform. Under 50 Ω + 25 mH inductive load conditions, the total harmonic distortion (THD) is measured as 1.41%. Inverter efficiency is 96.48% in loss analysis with PLECS. The voltage peaks that occur during polarity transitions were eliminated by using controlled power switches instead of diodes and a stabilized output was obtained.

Yenilenebilir Enerji Sistemleri için Düşük Maliyetli ve Yüksek Verimli Yeni Bir 15 Seviyeli Hibrit MLI Topolojisi

Makale Bilgisi

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Öz

Bu makale, tek DA kaynaklı çok seviyeli evirici (ÇSE) için yeni bir hibrit model önermektedir. Önerilen anahtarlamalı diyot (AD) ve yüksek frekanslı bağlantı (YFB) hibrit yapısı, tek bir DA kaynak gerilimi kullanır ve Paketlenmiş U-Hücresi (PUH) devresine çoklu DA gerilimleri sağlar. ÇSE sadece 8 yarı iletken cihaz kullanarak çıkış sinyalinde 15 seviye üretir. Bu, sistemin kontrolünü basitleştirir ve 2,71'lik düşük maliyet fonksiyonu (MF) ile ekonomik bir çözüm sağlar. Ayrıca, literatürdeki son çalışmalarla detaylı bir karşılaştırma yapılmıştır. Diğer birçok çalışmadan farklı olarak, gerilim kazancı için HFB yaklaşımı kullanılmıştır. Yük akımı çoğunlukla doğrudan DA kaynaktan sağlanırken, sadece küçük bir kısmı yüksek frekans transformatöründen geçmektedir. Bu, transformatör boyutunu ve maliyetlerini önemli ölçüde azaltır. Endüktif yüklerle yapılan testlerde, çıkış neredeyse saf sinüzoidal benzeri dalga biçimindedir. 50Ω + 25mH endüktif yük koşulları altında, toplam harmonik bozulma (THB) %1,41 olarak ölçülmüştür. PLECS ile yapılan kayıp analizinde evirici verimi %96,48'dir. Polarite geçişleri sırasında oluşan gerilim tepe noktaları diyotlar yerine kontrollü güç anahtarları kullanılarak giderilmiş ve stabilize bir çıkış elde edilmiştir.

1. INTRODUCTION (GİRİŞ)

In recent years, significant developments in the power electronics field have highlighted the limitations of conventional two-level inverters in various applications [1], [2]. New generation applications require high power and high quality AC power [3], [4]. Some of these are electric vehicles, storage systems and renewable energy systems [5], [6]. Multilevel inverters (MLIs) offer reduced total harmonic distortion (THD) and enhanced output waveform quality in high-voltage

*Corresponding author, e-mail: murat.karakilic@igdir.edu.tr
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and high-power scenarios. These advantages have made them essential for many applications [7], [8].

Traditional MLI topologies such as cascaded neutral point clamped (NPC), flying capacitor (FC) and H-bridge (CHB) have been developed by many researchers [9]. A major limitation of these topologies is their requirement for a substantial number of power switches when scaled to achieve improved power quality and generate higher voltage levels [10]. Therefore, several strategies to improve the design of traditional MLI topologies have been developed to produce new topologies using these designs [11]. In order to reduce the cost and control complexity, the use of fewer switches in topologies has gained importance. However, using fewer switches can lead to higher voltage stress (TSV) on the switches [12]. Thus, the maximum voltage stress (MVS) increases and consequently switching losses increase. This negatively affects the performance of the inverter. These limitations have led researchers to new MLI designs and these studies, which are the focus of future research, are often referred to as next generation topologies. Some of the notable studies in the literature are presented with their major findings.

Some researchers have proposed topologies to reduce DC sources used in their proposed MLI structures. For example, in [13], a new design with two DC voltage sources is proposed. This structure is developed to achieve higher output voltage levels and aims to reduce independent DC sources compared to conventional MLIs. In [14], an extended general structure with series connection of the proposed MLI is presented. The recommended circuit has symmetrical and asymmetrical DC input source configurations.

Other researchers have developed new modules that synthesize the positive and negative levels of the topology without the need for an H-bridge structure [15]. Mostly asymmetric source configurations have been proposed to synthesize higher levels compared to the symmetric source configuration with the same number of power elements [16]. A square T-type module with 12 switches and 4 different DC sources was introduced in [17], which eliminates the need for H-bridges. In another work, the main topology generating 15 levels was extended to obtain 25 levels [18]. Switched diode (SD) circuit is frequently used in MLIs. Especially in two-stage MLI topologies, unipolar bus voltages are converted into bipolar levels with H-bridge using SD circuit [19].

Since numerous power systems, storage units, and electric vehicles (EVs) operate with a single DC-link voltage, efficient conversion of DC power into high-quality AC power becomes essential [20]. As a result, the development of suitable topologies utilizing a single DC source is crucial for such applications. Recent studies in the literature show that most single-source MLI configurations are based on switched capacitor structures. Another widely used method is to use a high frequency link (HFL) [21]. Both methods are notable for their effectiveness in achieving higher voltage levels using a single DC source. While HFL offers the advantage of reducing the cost and size of the system, it can increase the size of the transformer as all the power needs to be transmitted through the transformer. To address this limitation, some studies used the main DC source at selected output levels connected directly to the load, while the intermediate voltage levels have been generated from bus voltages generated through high-frequency link (HFL) techniques. While this method is effective in generating DC link voltages in multilevel inverters, it significantly reduces the transformer size, significantly affecting the overall efficiency [22].

In this paper, a 15-level multilevel inverter (MLI) design operating with only a single DC voltage source is presented. Two alternative structures, switched diode (SD) and switched source (SS), are proposed. The designed topology consists of three main parts: the first part is the SD or SS based structure, the second part is the high frequency link (HFL) DC-DC converter circuit and the third part is the packaged U cell (PUC) architecture. The proposed structure is compared with similar topologies in the existing literature and its advantages are highlighted. In particular, it has a very low cost function (CF) value of 2.37, which makes the topology economically favorable. In addition, the targeted output level is achieved by using only 8 power switches, which is quite low compared to similar studies.

2. PROPOSED TOPOLOGY (ÖNERİLEN TOPOLOJİ)

The hybrid MLI topology introduced in this study is illustrated in Figure 1. As depicted, the overall structure comprises three main sections: HFL, the auxiliary unit, and the main PUC circuit. HFL

transforms the voltage of DC source ($4V_{DC}$) into multiple bus voltages, specifically $1V_{DC}$ and $2V_{DC}$. In the second part, it uses Aux-1 and Aux-2 bus voltages and transfers them to the PUC circuit. The Pack-U Cell (PUC), which forms the main structure of the topology, generates a 15-level staircase waveform at the output using the DC source at the input and the intermediate level bus voltages.

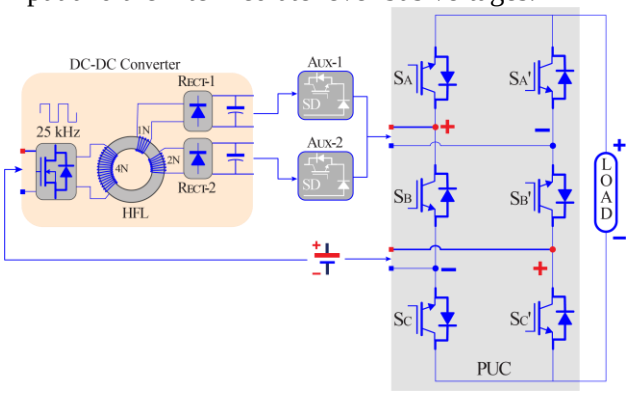


Figure 1. Proposed 15-Level hybrid MLI topology (Önerilen 15 seviyeli hibrit ÇSE topolojisi.)

In MLI circuits, the reversal of current direction at polarity transitions due to the effect of inductive components leads to peaks in the output voltage. This is due to the effect of the diodes on the current path in different operating modes, as the diodes can allow current to flow in certain directions and cut it off in case of reverse polarity. Sudden polarity changes cause a peak in the voltage wave because the diodes are reverse biased in the first instance. The most permanent solution is to replace the diodes with power switches. Power switches contain antiparallel diodes that allow the current on the switch to complete the cycle through the relevant diode in case of sudden changes in direction. Therefore, in the proposed topology, since the diodes produce peak voltages, power switches are used instead of diodes as a solution. Figure 1 shows the SC and the SS circuit which is formed by replacing the diode in this circuit with a power switch. Topology is simulated with both circuits and the results show that the problem is solved. The switching states are shown in Table 1.

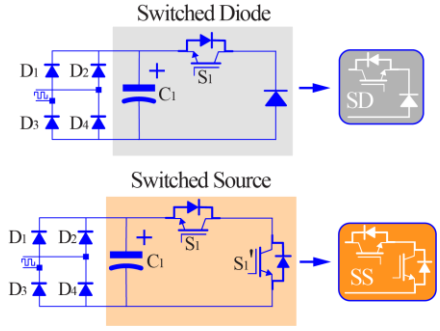


Figure 1. SC and SS circuits (AD ve AK devreleri)

Table 1. Switching Pattern Of the Proposed Topology (Önerilen Topolojinin Anahtarlama Modeli)

$S_1S_2S_AS_BS_C$	V_{out}	$S_1S_2S_AS_BS_C$	V_{out}
[00000]	+0	[01011]	-1
[01100]	+1	[10011]	-2
[10100]	+2	[11011]	-3
[11100]	+3	[00110]	-4
[00001]	+4	[01010]	-5
[01101]	+5	[10010]	-6
[10101]	+6	[11010]	-7
[11101]	+7		

As shown in Figure 2, Aux-1 applies $1V_{DC}$, Aux-2 applies $2V_{DC}$ bus voltages to the upper layer of the PUC, while the $4V_{DC}$ input source is connected to the lower layer. The HFL converts the input DC voltage into a load frequency AC wave and applies it to the transformer. The high frequency transformer has a winding ratio of 4:1:2. Thus, the $1V_{DC}$ and $2V_{DC}$ high frequency AC wave generated at its output charges the capacitors with the help of rectifiers and converts them into DC bus voltages.

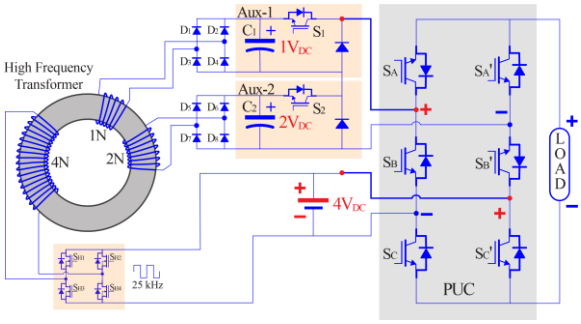


Figure 2. Circuit diagram of the proposed MLI topology (Önerilen ÇSE topolojisinin devre şeması)

Figure 3 explains the basic working principle of the proposed topology. The supply voltages are connected in reverse direction in the upper and lower layers of the PUC main circuit. This is due to the main working principle of the PUC circuit. V_u represents the upper layer supply voltage and V_b represents the lower layer voltage. The voltages synthesized by the PUC topology on the load are $\pm V_u$, $\pm V_b$, $\pm(V_u + V_b)$, respectively. In the proposed topology, multiple DC bus voltages produced by the DC-DC converter are applied instead of V_u. Thus, the PUC circuit produces voltages as ±1, ±2, ±3, ±4, ±(1+4), ±(2+4) and ±(3+4);

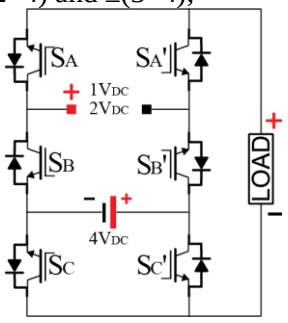


Figure 3. Voltage configuration of the main circuit. (Ana devrenin voltaj konfigürasyonu)

The proposed configuration has been thoroughly evaluated using both Sinusoidal Pulse Width Modulation (SPWM) and Nearest Level Control (NLC) strategies.The gate pulses generated by both control techniques and output voltage signals are presented in Figure 4. As seen in the figure, the upper signals are generated by SPWM and the lower ones are generated by NLC control technique. These findings are of critical importance in comparing the performance of both control techniques. In previous studies, the analyses performed on the dynamic responses and harmonic contents of these control techniques increase the reliability and applicability of the obtained results.

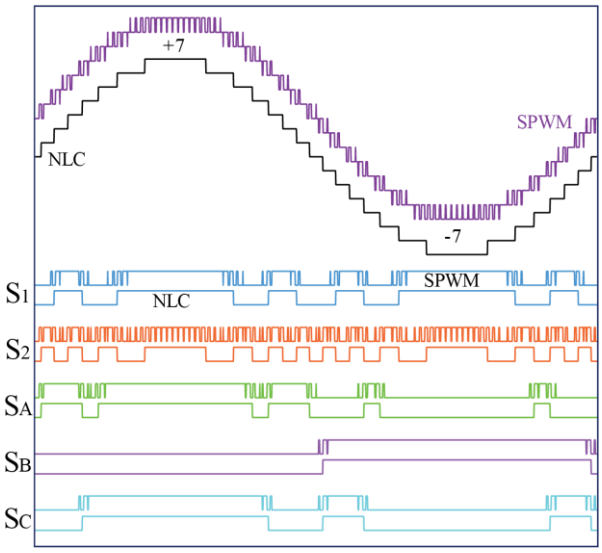


Figure 4. The output voltage waveforms and gate pulses of proposed MLI with (a) NLC and (b) SPWM control method. (Önerilen ÇSE'nin (a) NLC ve (b) SPWM kontrol yöntemi ile çıkış gerilimi dalga şekilleri ve kapı darbeleri.)

Figure illustrates the voltage stress experienced by the switches at various levels. Among all switching devices, S_B and S_B' are subjected to the largest voltage stress across the topology. The total blocking voltage, defined as the cumulative maximum voltage stress of all switches, serves as an important benchmark for evaluating MLI configurations. The maximum voltage values for each switch can be expressed as follows:

$$\begin{aligned} V_{SA'} &= V_{SA} = 3V_{DC} \\ V_{SB'} &= V_{SB} = 7V_{DC} \\ V_{SC'} &= V_{SC} = 4V_{DC} \\ V_{S1} &= 1V_{DC} \\ V_{S2} &= 2V_{DC} \end{aligned} \quad (1)$$

$$\begin{aligned} TBV &= V_{SA'} + V_{SA} + V_{SB'} + V_{SB} + V_{SC'} + V_{SC} + V_{S1} + V_{S2} \\ TBV &= 31V_{DC} \end{aligned} \quad (2)$$

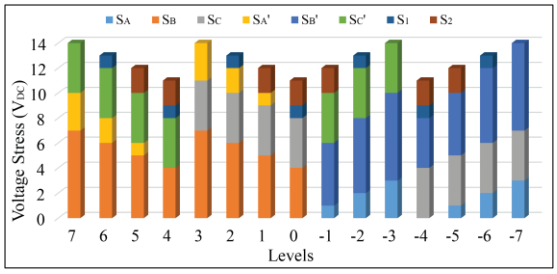


Figure 6. Voltage stress across to power switches in the proposed MLI. (Önerilen ÇSE'de güç anahtarları üzerindeki gerilim stresi.)

Figure provides a detailed representation of the power loss distribution among the power components. Thermal loss analysis using PLECS software shows that all power switches and diodes operating at the fundamental frequency exhibit an even loss distribution. Although the switches in the main module are subjected to higher voltage stresses, higher power losses occur in the switches in the Aux-1 and Aux-2 circuits. The highest individual power loss is noted at switch S_2, accounting for 10% of the total loss. Meanwhile, the high frequency switches S_{H1}-S_{H4} contribute 2% of the total power loss.

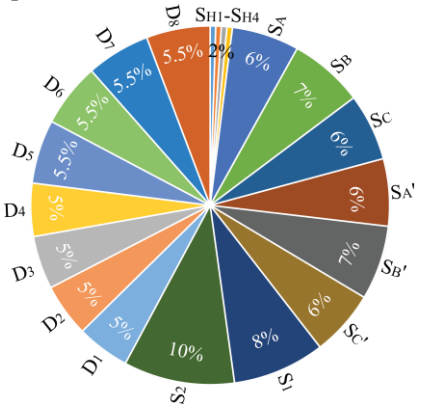


Figure 7. Power loss distribution (Güç kaybı dağılımı)

Based on the switching states provided in Table 1, the operating modes are illustrated in Figure . The figure highlights the ON-state power switches and corresponding bus voltages along the current path. Morover, the states of the S_1 and S_2 switches in the Aux-1 and Aux-2 circuits that provide multiple bus voltages to the upper layer of the PUC circuit in each operating mode are specified. As seen in the circuit diagram of the proposed topology in Figure 3, Aux-1 produces $0V_{DC}$ at its output for S_1=0 and $1V_{DC}$ for S_1=1. Similarly, Aux-2 produces 0 V_{DC} for S_2=0 and $2V_{DC}$ for S_2=1. Since the Aux-1, 2 circuits are connected in series, $3V_{DC}$ bus voltage is produced in the S_2S_1=11 switching state. All operating modes and switch states are presented in Figure 8.

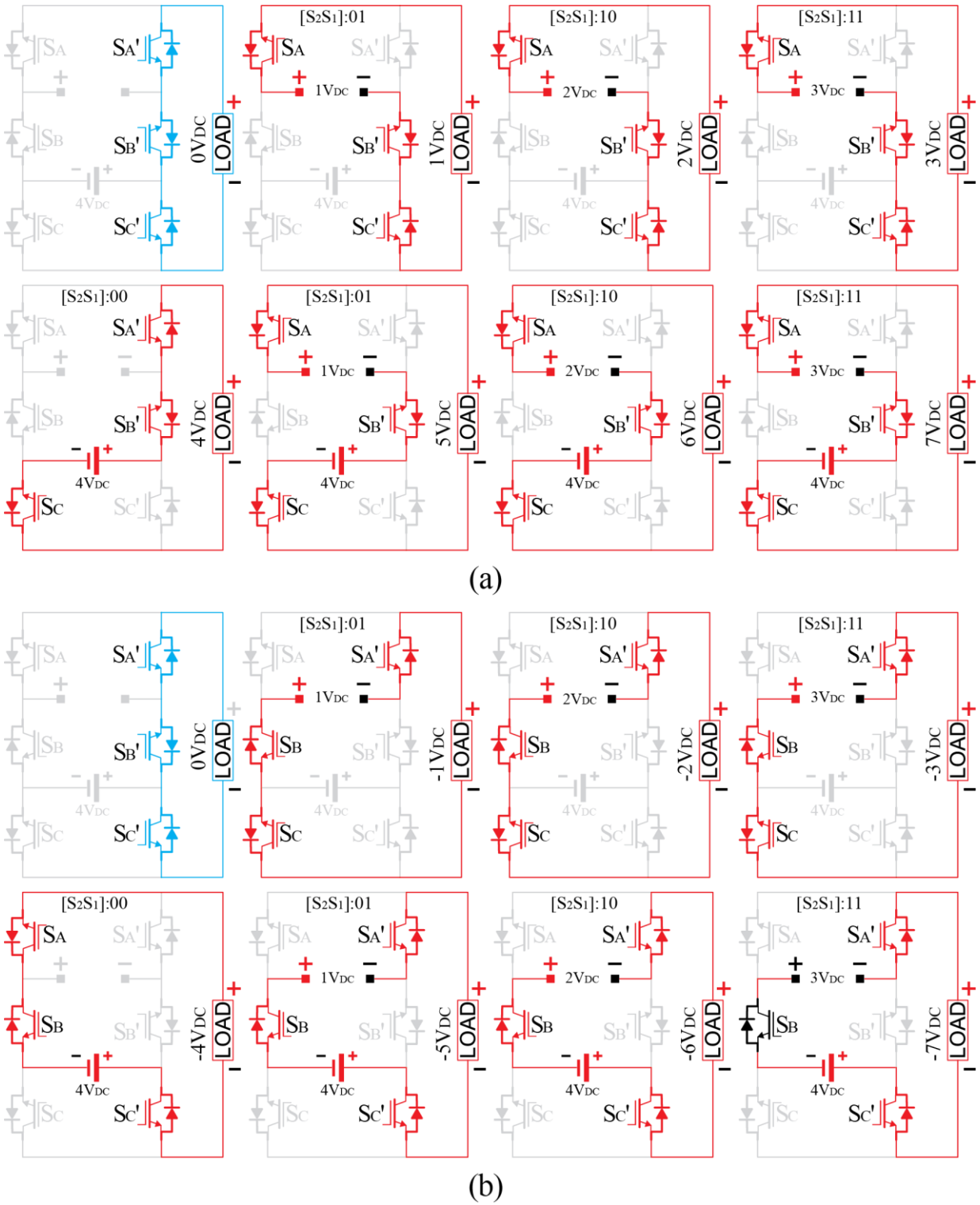


Figure 8. Operating modes of the proposed topology (Önerilen topolojinin çalışma modları)

In order to accurately determine the system efficiency in MLI structures, it is of great importance to determine the power losses in the circuit with practical methods. Although it is possible to calculate the losses under different load conditions with theoretical approaches, the electrical and thermal parameters of the circuit elements during operation vary depending on environmental factors, especially temperature. These dynamic changes reduce the accuracy of theoretical calculations and make the process complex. Therefore, in order to obtain more realistic results in power electronics systems, it is preferred to use simulation software that works with models including the thermal behavior of circuit components. In this study, the losses of power

components such as switches, diodes and capacitors are analyzed with PLECS software using thermal models of the relevant components. The simulations are carried out under output power values ranging from 0 to 1000 W and the variation of the efficiency depending on the output power is presented in Figure 5. The analysis results show that the proposed MLI topology operates with a high efficiency of 96.48%, especially at 1000 W output power. This result demonstrates that the structure not only works efficiently in high power applications but also minimizes losses with proper design and control.

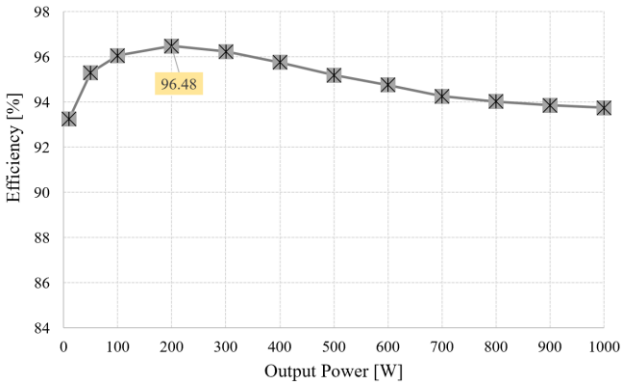


Figure 5. Inverter efficiency versus output power (Çıkış gücüne karşı invertör verimliliği)

3. COMPARATIVE STUDY (KARŞILAŞTIRMALI ÇALIŞMA)

This paper provides a detailed comparison with recent studies to show performance of proposed MLI topology. The main parameters used by many researchers to indicate the advantages of their proposed topology are the number of power elements used, the number of DC sources, the TBV and the number of levels generated by the topology. Although the cost functions (CF) determined with these parameters are partially formulated differently, they are mostly similar to each other.

The CF is determined as in Equation (3) according to the parameters specified.

$$CF = \frac{(N_{SW} + N_{GD} + N_D + N_C + \alpha TBV) \cdot N_{DC}}{N_L} \quad (3)$$

where α is defined as 0.5 and 1.5, selected based on the relative importance of the TSV.

Table 2 compares various inverter topologies in terms of the number of power components utilized and the total blocking voltage (TBV). Many studies have advantages and disadvantages. For example, the study in [23] synthesizes 9 levels at the output using 12 power devices and 3 switched capacitors. However, the same number of output levels is achieved by the topology in [11] using 10 switches. Moreover, it synthesizes 15 levels with 10 switches [24]. However, since it has a very high CF value, it is quite weak in terms of cost. The effect of 4 DC sources used at the input is significant in this. Another topology, the study in [25], synthesizes 7 levels with 10 switches and 2 capacitors, although its TBV value is very low. However, there are topologies that produce higher levels with fewer power elements [26]. The topology proposed in this study produces 15 output levels using only 8 power switches. The power switches used in the circuit reach a TBV value of 31V and attract attention with its low cost function (CF). It is seen that it has a very low cost compared to other studies in the literature. This increases the cost effectiveness of the system and brings about simplicity of design by reducing the number of components.

Table 2. Comparative analysis of proposed MLI (Önerilen ÇSE'nin karşılaştırmalı analizi)

Topology	Year	N_L	N_{DC}	N_{SW}	N_{GD}	N_D	N_C	TBV	C_F (α)	
									0.5	1.5
[11]	2023	9	1	10	9	2	3	44	5.11	10.00
[27]	2024	7	1	7	7	2	2	15	3.64	5.79
[25]	2024	7	1	10	10	1	2	17	4.50	6.93
[28]	2024	7	1	8	8	-	4	16	4.00	6.29
[23]	2022	9	1	12	11	-	3	44	5.33	10.22
[29]	2019	9	1	11	10	-	2	40	4.78	9.22
[30]	2022	13	1	14	13	-	3	33	3.58	6.12
[31]	2022	13	1	12	11	3	3	36	3.62	6.38
[32]	2019	13	2	16	16	-	4	34	8.15	13.38
[33]	2019	13	2	14	11	-	2	32	6.62	11.54
[34]	2021	13	2	14	14	2	4	34	7.85	13.08
[35]	2022	15	2	10	10	1	1	34	5.20	9.73
[24]	2017	15	4	10	10	-	-	42	10.93	22.13
[26]	2019	15	3	10	9	-	-	34	7.20	14.00
Prop.	**2024**	**15**	**1**	**8**	**8**	**2**	**2**	**31**	**2.37**	**4.43**

4. RESULTS AND DISCUSSION (BULGULAR VE TARTIŞMA)

The simulation analysis of the proposed 15-level (15L) hybrid MLI is performed using Matlab/Simulink and PLECS environments. The control and main circuit modeling of the proposed topology is performed in Matlab, while the loss evaluations are realized using PLECS. For the simulation setup, a 60 V_{DC} source is used and gate signals are generated using both NLC and SPWM techniques. Figure 6 shows the operating performance under a 50Ω pure resistive load using NLC approach. In particular, Figure 6(a) presents the output waveforms, while Figure 10(b) shows the voltage waveforms at the outputs of the Aux-1 and Aux-2 DC-DC converters. Similarly, Figure 7 shows waveforms under the same load condition using SPWM control method.

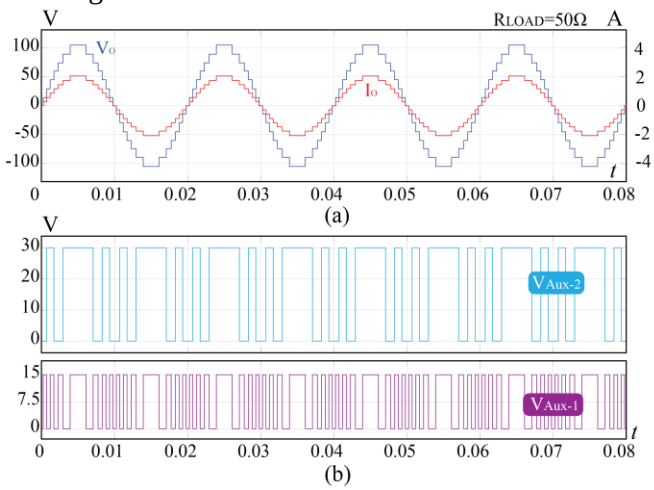


Figure 6. Voltage and current waveforms of the proposed topology (a), Aux-1 and Aux-2 voltages (b) (Önerilen topolojinin gerilim ve akım dalga şekilleri (a), Aux-1 ve Aux-2 gerilimleri (b))

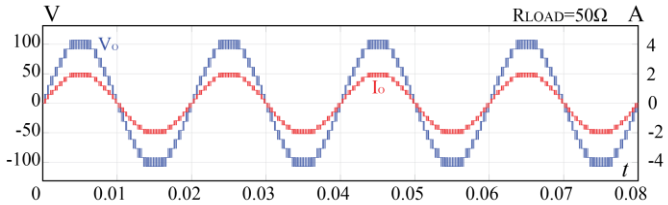


Figure 7. Voltage and current waveforms with SPWM method (SPWM yöntemi ile gerilim ve akım dalga şekilleri)

The inductive operation performance of the proposed 15L-MLI has been tested with 50Ω+25mH and 50Ω+50mH loads and the output waveforms are shown in Figure 8 (a) and (b), respectively. As can be seen, as the inductive load increases in the output waveforms, the voltage causes peaks at the polarity change moments. This will cause problems in highly inductive loads. As a solution to this problem, it is suggested to replace the Aux circuits with SS circuits instead of SD.

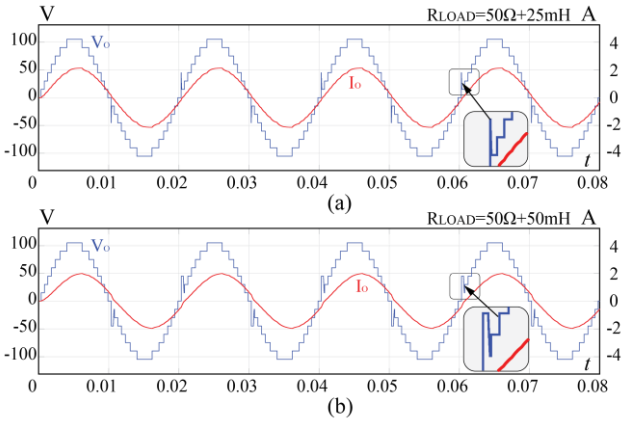


Figure 8. Inductive load response of the proposed MLI (Önerilen ÇSE'nin endüktif yük tepkisi)

It is seen in Figure 9 that the problem is eliminated by adding SS circuits. The output waveforms of the proposed circuit produced with different inductive loads are presented in the figure. In Figure 9, it is seen that there is no distortion in the output waveforms with 50Ω+25mH, 50Ω+50mH and 50Ω+200mH loads, respectively. Figure 9 (c) shows that there is no distortion despite the high inductive component. In addition, the analysis shows that the proposed solution is successful in both NLC and SPWM control techniques. THD analysis of the output current under these loads is shown in Figure 10. It is seen that very low total harmonic distortion (THD=1.53%) occurs in the current wave despite the low inductive load.

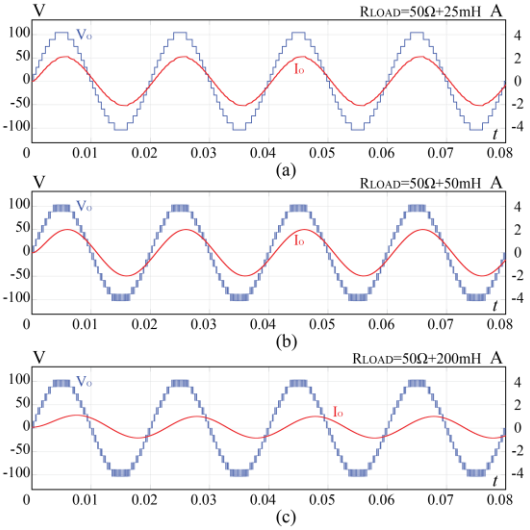


Figure 9. Output voltage and current waveforms with SS circuit (SS devresi ile çıkış gerilimi ve akım dalga şekilleri)

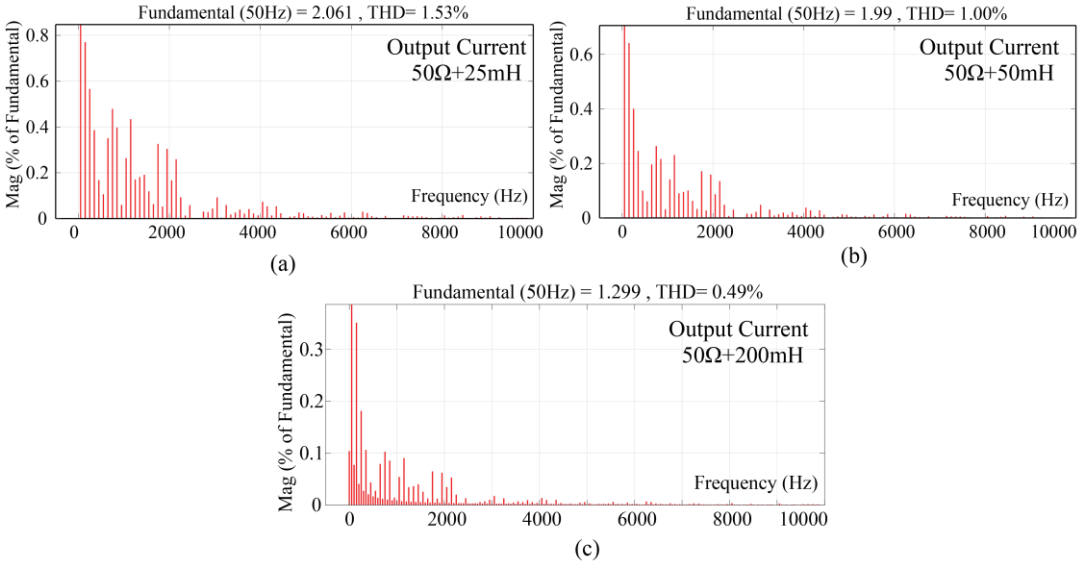


Figure 10. Harmonic analysis of the output currents with different loads (Farklı yüklerle çıkış akımlarının harmonik analizi)

Figure 10 (a) and (b) illustrate the variations in switching frequency and modulation index (MI), respectively. In Figure 15 (a), only the frequency is varied, whereas in Figure 11 (b) the frequency and MI are simultaneously varied. The corresponding frequency and MI values and the moments when these changes occur are indicated in the figures. The obtained results show that the proposed topology works stably against frequency and MI variations and no distortion is observed in the output waveforms.

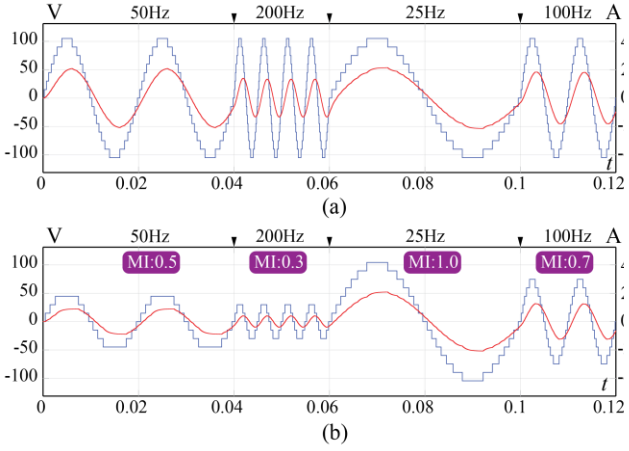


Figure 11. Response of output voltage and current to frequency (a) and modulation index changing (b) (Çıkış gerilimi ve akımının frekansa (a) ve modülasyon indeksi değişimine (b) tepkisi)

Figure 13 shows the experimental setup of the proposed MLI topology. The control signals are generated using a FPGA development board with high-performance digital signal processing capabilities. In the experimental system, the switching frequencies are set to 50 Hz (for the NLC method) and 5 kHz (for the SPWM method) to correspond to different control strategies. The tests performed on this prototype show that the designed topology can operate stably and reliably in real-time applications.

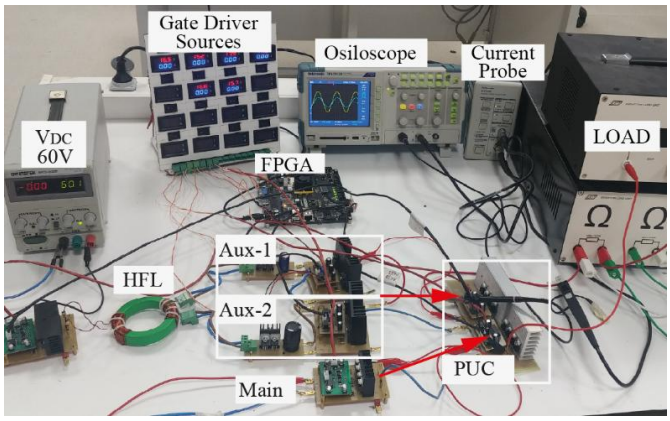
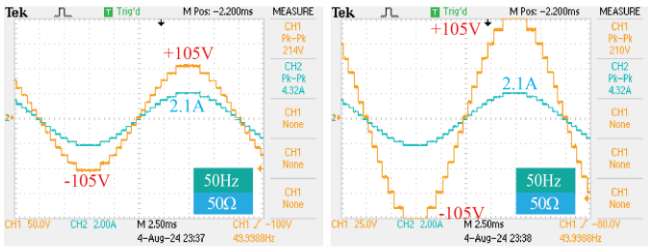


Figure 12. Experimental prototype of the proposed MLI (Önerilen ÇSE'nin deneysel prototipi)

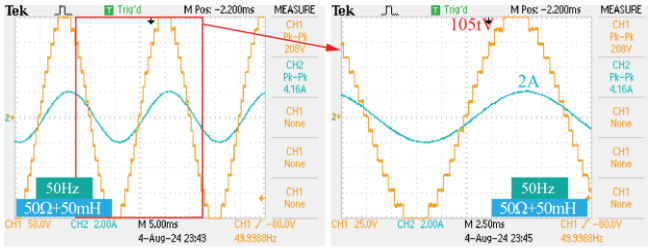
Figure 13 shows the experimental prototype test results under 60 VDC input voltage and 50Ω resistive inductive load (RL). In Figure 13 (a) and (b), it is observed that the output current and voltage are in the same phase. In addition, the output current and voltage waveforms show a 15-step staircase waveform operating at a frequency of 50 Hz. Theamplitude of the voltage waveform is measured as 105 V. These results demonstrate that the topology successfully achieves the experimentally predicted performance.



(a) (b)

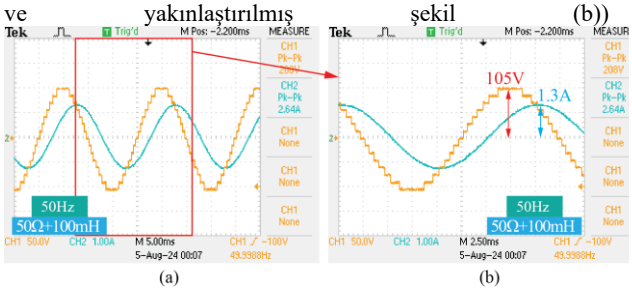
Figure 13. Experimental scopes of proposed MLI (a) output signals, (b) zoomed-in figure (Önerilen ÇSE'nin deneysel ölçekleri (a) çıkış sinyalleri, (b) yakınlaştırılmış şekil)

In order to show the inductive performance of the circuit, the experiment has been tested with different loads. First, the test is realized with a 50Ω+50mH load. Figure 14 shows no distortion occurred in the output signals. In the zoomed-in view of the waveforms in Figure 14 (b), it is seen that the current is smooth and is near to sinusoidal waveform. For high inductive performance, 200mH is connected to the load and the output waveforms are seen in Figure 15. Due to the high inductive load, the total impedance changed and the amplitude of the current wave decreased from 2A to 1.3A. In addition, the current phase shift compared to the voltage wave is noticeable.



(a) (b)

Figure 14. Inductive performance of proposed MLI with 50Ω+50mH load (a), and zoomed-in figure (b) (Önerilen ÇSE'nin 50Ω+50mH yük ile endüktif performansı (a) ve yakınlaştırılmış şekil (b))



(a) (b)

Figure 15. Inductive performance of proposed MLI with 50Ω+200mH load (a), and zoomed-in figure (b) (Önerilen ÇSE'nin 50Ω+200mH yük ile endüktif performansı (a) ve yakınlaştırılmış şekil (b))

Figure 16 shows output effect of modulation index (MI) variation. A reduction in the MI value decreases the number of levels and consequently negatively affects the quality of the output waveform. This figure presents the output waveforms corresponding to modulation index (MI) variations between 0.35 and 1.0. It is evident that the number of generated output levels varies with the MI value. For instance, an MI of 0.75 results in 10 output levels, whereas an MI of 0.35 produces only 5 levels. However, the output stability and voltage uniformity of the system are maintained despite the MI variations. Figure 17 shows the response of the experimental prototype to frequency variations. The circuit responded smoothly to frequency variations between 200 Hz and 25 Hz and no distortion was observed in the output signals. Figure 18 shows the dynamic system response when MI and frequency are varied simultaneously. The obtained results show that the proposed 15-level MLI topology exhibits high stability for different modulation indices and frequency variations.

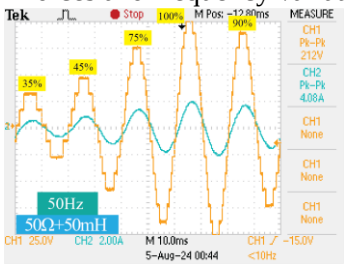
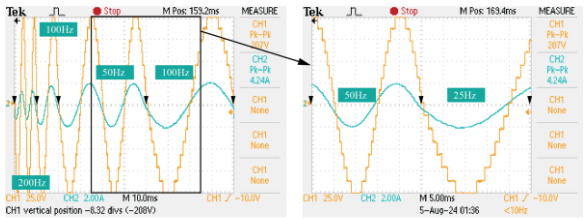
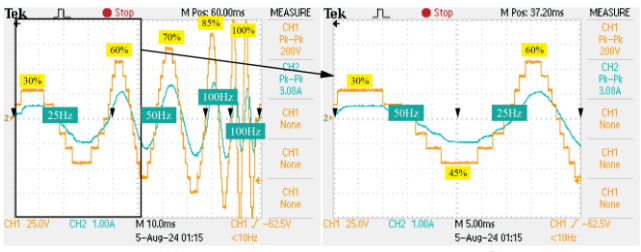


Figure 16. Dynamic performance of the proposed MLI under MI variation (Önerilen ÇSE'nin MI değişimi altında dinamik performansı)



(a) (b)

Figure 17. Dynamic performance of the proposed MLI under frequency variation (Önerilen ÇSE'nin frekans değişimi altında dinamik performansı)



(a) (b)

Figure 18. Dynamic performance of the proposed MLI under MI and frequency variation (Önerilen ÇSE'nin MI ve frekans değişimi altında dinamik performansı)

5. CONCLUSIONS (SONUÇLAR)

In this paper, a novel hybrid MLI topology is proposed that operates using only a single DC source. The most remarkable feature of the topology is its ability to generate 15 level at the output signal without additional DC voltage source. This performance is achieved using only eight power switches, simplifying the control structure of the system considerably. Compared to similar structures in the literature, this topology has a lower cost function (CF) value of 2.71, making it an economically prominent solution. Moreover, one of the most unique contributions of this work is the utilization of a HFL structure for voltage boosting. While most of the current is supplied directly from the input source, a small portion of the current is drawn from the HFL to generate the intermediate voltage levels, thus reducing transformer size and cost. For a low inductive load of 50Ω + 25mH, the output of the system is nearly ideal sinusoidal current, which is supported by a total harmonic distortion (THD) value of 1.41%. The inverter efficiency analysis is performed with PLECS software and the findings indicate that the proposed topology operates with 96.48% efficiency. On the other hand, the switched diode (SD) element used in the circuit caused unwanted peaks in the output voltage during polarity transitions. In order to overcome this problem, a switched source (SS) circuit with controlled switches is proposed instead of the SD circuit, thus stabilizing the output waveform.

As a result, the prominent findings of the study are summarized below:

- The proposed structure produces high-level output with low number of switches and offers a cost advantage with a CF of 2.71.
- Under low inductive load, almost sinusoidal output current is obtained with a THD value of 1.41%.
- According to the simulation results, the efficiency of the system is 96.48%.

Disturbing voltage peaks at polarity transitions are successfully eliminated by the SS circuit and output stability is achieved.

DECLARATION OF ETHICAL STANDARDS (ETİK STANDARTLARIN BEYANI)

The author of this article declares that the materials and methods they use in their work do not require ethical committee approval and/or legal-specific permission.

Bu makalenin yazarı çalışmalarında kullandıkları materyal ve yöntemlerin etik kurul izni ve/veya yasal-özel bir izin gerektirmediğini beyan ederler.

AUTHORS' CONTRIBUTIONS (YAZARLARIN KATKILARI)

***Murat KARAKILIÇ*:** Theoretical calculations, simulation studies, experimental setup and analysis of the proposed topology and writing and editing of the paper.

Önerilen topolojinin teorik hesaplamaları, benzetim çalışmaları, deney düzeneği kurulumu ve analiz süreçlerini yürütülmesi ile makalenin yazımı ve düzenlenmesi.

***Hasan HATAŞ*:** Evaluation of experimental and simulation results, preparation of graphs and illustrations.

Deneysel ve benzetim sonuçlarının değerlendirilmesi, grafik ve illustrasyonların hazırlanması.

CONFLICT OF INTEREST (ÇIKAR ÇATIŞMASI)

There is no conflict of interest in this study.

Bu çalışmada herhangi bir çıkar çatışması yoktur.

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