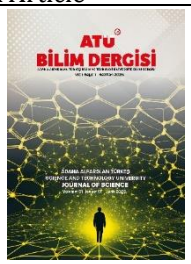
ADANA ALPARSLAN TÜRKEŞ BİLİM VE TEKNOLOJİ ÜNİVERSİTESİ BİLİM DERGİSİ

ADANA ALPARSLAN TÜRKEŞ SCIENCE AND TECHNOLOGY UNIVERSITY JOURNAL OF SCIENCE

Research Article www.dergipark.com/atujscience



Design and Simulations of a Stable Oscillator Circuit in 90 nm CMOS Technology

Emre Baysal[1,#], Ulaş Reyhan[2], Berke Ersöz[3], Emre Berkan Sungur[4], Yılmaz Zini[5], Mahmud Yusuf Tanrıkulu[6]

[1,2,3,4,5,6]Adana Alparslan Türkeş Science and Technology University, Faculty of Engineering, Department of Electrical-Electronics Engineering, Postcode, 01250, Adana, Türkiye

ORCID[1]: 0009-0009-9220-1910

ORCID[2]: 0009-0004-8248-3348

ORCID[3]: 0009-0002-8742-0632

ORCID[4]: 0009-0003-2831-6867

ORCID[5]: 0009-0006-9732-3667

ORCID[6]: 0000-0001-7956-1289

[#]Corresponding Author:
byslemre2380@gmail.com

Abstract

In the realm of modern integrated circuit design, the need for efficient, low-power, and high-accuracy systems has led to the development of advanced circuit components. This study focuses on the design and integration of Bandgap Reference (BGR) circuits, Low-Dropout (LDO) regulators, and Voltage-Controlled Oscillators (VCOs) to enhance the performance of low-power integrated systems. These circuits address critical challenges, including temperature stability, power efficiency, and frequency accuracy, making them indispensable for applications in mobile devices, communication systems, and embedded electronics. The proposed designs have been developed using 90 nm CMOS technology and validated through extensive simulations. Key performance metrics such as temperature coefficient, power consumption, phase noise, and output stability have been optimized to demonstrate the practical applicability of the circuits. The findings highlight the potential for combining BGR, LDO, and VCO circuits to achieve a unified solution that meets the demands of modern low-power electronic systems. This work not only contributes to the advancement of circuit design methodologies but also sets the stage for future innovations in mixed-signal and low-power integrated circuits. By addressing the interplay between these components, the study provides a foundation for developing more efficient, reliable, and versatile electronic systems.

Keywords: Bandgap Reference; Low-Dropout; Voltage-Controlled Oscillator; Complementary Metal-Oxide-Semiconductor; Temperature coefficient

Bir Kararlı Salınıcı Devresinin 90 nm CMOS Teknolojisinde Tasarımı ve Simülasyonları

Öz

Modern entegre devre tasarımında, verimli, düşük güç tüketimli ve yüksek doğruluklu sistemlere olan ihtiyaç, gelişmiş devre bileşenlerinin geliştirilmesine yol açmıştır. Bu çalışma, düşük güçlü entegre sistemlerin performansını arttırmak amacıyla Bant Aralığı Referansı (BGR) devreleri, Düşük kayıplı (LDO) Regülatörleri ve Gerilim Kontrollü Salınıcılar (VCO) tasarımına ve entegrasyonuna odaklanmaktadır. Bu devreler, sıcaklık kararlılığı, güç verimliliği ve frekans doğruluğu gibi kritik zorlukları ele alarak mobil cihazlar, haberleşme ve gömülü sistemler gibi uygulamalar için vazgeçilmez hale gelmektedir. Önerilen tasarımlar CMOS teknolojisi kullanılarak geliştirilmiş ve kapsamlı simülasyonlar ile doğrulanmıştır. Sıcaklık katsayısı, güç tüketimi, faz gürültüsü ve çıkış kararlılığı gibi temel performans metrikleri optimize edilerek devrelerin pratik uygulanabilirliği gösterilmiştir. Bulgular, BGR, LDO ve VCO devrelerinin birleştirilerek modern düşük güçlü elektronik sistemlerin gereksinimlerini karşılayan bütünleşik bir çözüm elde edilebileceğini ortaya koymaktadır. Bu çalışma, yalnızca devre tasarım metodolojilerinin ilerlemesine katkıda bulunmakla kalmayıp, aynı zamanda karma sinyal ve düşük güçlü entegre devrelerde gelecekteki yenilikler için bir temel oluşturmaktadır. Bu bileşenler arasındaki etkileşimi ele alarak daha verimli, güvenilir ve çok yönlü elektronik sistemlerin geliştirilmesine zemin hazırlamaktadır.

Anahtar Kelimeler: Bant Aralığı Referansı; Düşük Kayıplı; Gerilim Kontrollü Salınıcı; Tümleyici Metal Oksit Yarı İletken; Sıcaklık katsayısı

Received: 16/05/2025

Accepted: 21/08/2025

Online Published: 25/12/2025

How to Cite: Baysal E., Reyhan U., Ersöz B., Sungur E. B., Zini Y., Tanrıkulu M. Y. "*Design and Simulations of a Stable Oscillator Circuit in 90 nm CMOS Technology*" Adana Alparslan Türkeş Science and Technology University Journal of Science, **1** (2): 50-61 (2025).

1. Introduction

In today's rapidly evolving technological landscape, the demand for low-power, high-accuracy, and reliable integrated circuits (ICs) has grown significantly. The proliferation of electronic devices, ranging from portable gadgets to advanced communication networks, has amplified the need for efficient power management and robust frequency stability to ensure optimal system performance. At the core of these advancements lie critical circuit components such as Bandgap Reference (BGR) circuits, Low Dropout (LDO) regulators, and Voltage-Controlled Oscillators (VCOs). These components form the backbone of modern integrated systems, enabling stability, precision, and efficiency in applications where minimizing power consumption and enhancing reliability are paramount [1].

1.1 Bandgap Reference (BGR) Circuit

BGR circuits are indispensable in providing a stable reference voltage that remains unaffected by temperature variations and power supply fluctuations. This stability is crucial for maintaining the accuracy and functionality of ICs across a myriad of applications [2], including mobile devices, industrial control systems, and medical equipment [3]. By leveraging the principles of proportional to absolute temperature coefficient (PTAT) and complementary to absolute temperature (CTAT) currents, BGR circuits achieve temperature compensation, ensuring consistent performance under varying environmental conditions [1]. These circuits typically incorporate an intricate combination of transistors, resistors, and operational amplifiers to balance these currents and generate a highly stable reference voltage. Innovations in BGR design now focus on minimizing power consumption while maintaining exceptional accuracy, making them ideal for energy-efficient and portable systems where every milliwatt of power savings matters [4] [5].

1.2 Low-Dropout (LDO) Regulator

LDO regulators play a pivotal role in power management by delivering a stable and precise output voltage with minimal input-to-output voltage difference. These circuits are widely deployed in applications demanding low noise, high efficiency, and compact design. The integration of LDO regulators into ICs facilitates effective power distribution, mitigates thermal challenges, and prolongs the operational life of electronic systems by shielding sensitive components from voltage irregularities [6]. Modern LDO designs incorporate advanced techniques, including dynamic feedback control, adaptive biasing, and transient response optimization, to address challenges posed by varying load conditions [7]. The inclusion of sophisticated elements such as error amplifiers and current mirrors has further enhanced their performance, offering robust solutions for stability and efficiency under fluctuating power demands [8] [9].

1.3 Voltage Controlled Oscillator (VCO)

VCOs are essential for frequency generation and synchronization in a wide range of applications, including communication systems, phase-locked loops (PLLs), and clock generation circuits [10]. By providing a voltage-controlled mechanism for frequency tuning, VCOs offer the flexibility required for diverse applications, from wireless communication to high-speed signal processing [11]. The performance of VCOs is often evaluated based on key parameters such as tuning range, phase noise, and power consumption. Current-starved VCO architectures have gained prominence for their ability to balance power efficiency with a wide frequency tuning range, meeting the stringent requirements of modern communication systems [12]. Furthermore, state-of-the-art VCO designs now incorporate innovative noise reduction techniques and enhanced linearity, ensuring minimal phase noise and improved signal integrity, even in high-frequency scenarios [13] [14].

In this study the design and the integration of Bandgap Reference (BGR) circuits, Low-Dropout (LDO) regulators, and Voltage-Controlled Oscillators (VCOs) are performed to enhance the performance of low-power integrated systems. The proposed designs have been designed using 90 nm CMOS technology and validated through extensive simulations [15]. Key performance metrics such as temperature coefficient, power consumption, phase noise, and output stability have been obtained to demonstrate the practical applicability of the circuits.

2. Material and Methods

In this study, Bandgap Reference (BGR), Low-Dropout (LDO) Regulator, and Voltage-Controlled Oscillator (VCO) circuits are designed, simulated, and analyzed to enhance the performance of low-power integrated systems. The study consists of three main stages, which are circuit design, simulation, and performance analysis. The design of the BGR, LDO, and VCO circuits are carried out using 90nm CMOS technology. Each circuit is optimized to ensure temperature stability, low power consumption, and high accuracy. Figure 1 shows the system created using this technology.

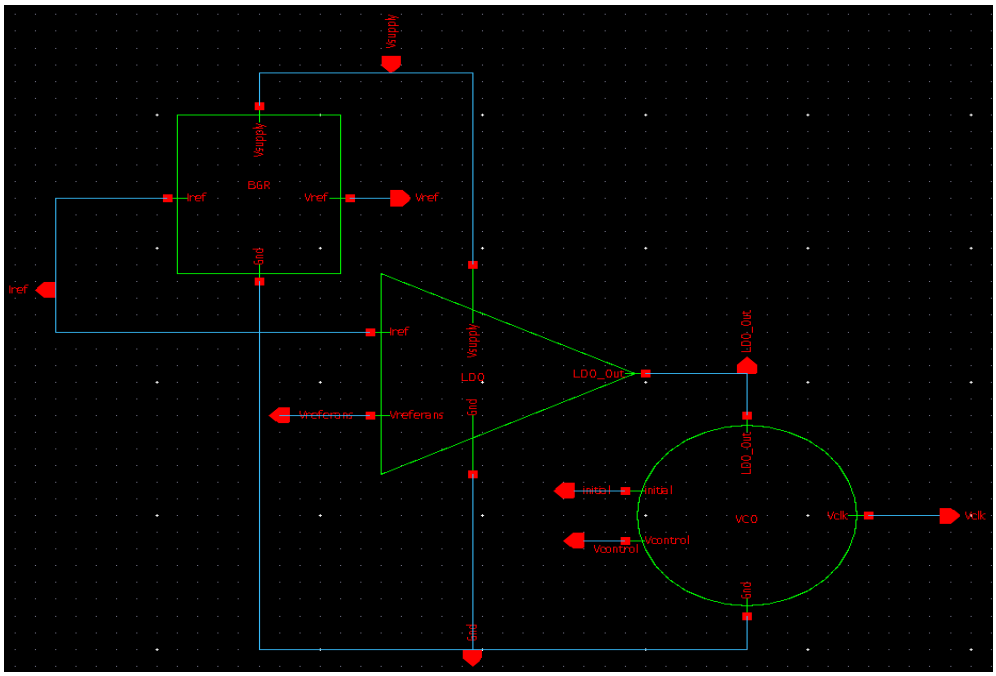


Figure 1. System architecture.

2.1 BGR

In the BGR circuit, a CMOS-based bandgap reference architecture was chosen to provide a stable reference current against temperature variations. During the design process, temperature coefficient minimization is considered to improve the accuracy of the reference current.

Figure 2 shows the BGR circuit which consists of transistors and resistors to generate a stable reference current against temperature variations. These components produce two opposing currents, which counteract temperature changes within the circuit.

The **core structure** shown in Figure 2 is designed using **M1**, **M2**, **R1**, **R2**, and **R4** components. Also, the operational amplifier (op-amp) structure consists of **M3**, **M4**, **M5**, **M6**, and **M7** MOSFETs [16]. **M9**, **M10**, **M11**, **M12**, and **M14** PMOS transistors are used as current mirrors in the circuit, transmitting a constant reference current to various points of the circuit. Thus, a stable current is ensured in the relevant circuit components. Additionally, **M13** and **M15** PMOS transistors are used as source followers. These structures ensure impedance matching between the BGR circuit and the load connected to the circuit. Consequently, it allows the BGR circuit to deliver a stable reference current to the load.

The node voltage V_a is set equal to the node voltage V_b by the input voltage definition of op-amp [4].

$$V_a = V_b \tag{1}$$

The temperature coefficient value of the thermal voltage (V_T) can be calculated from Equation 2 as having a positive temperature coefficient [14].

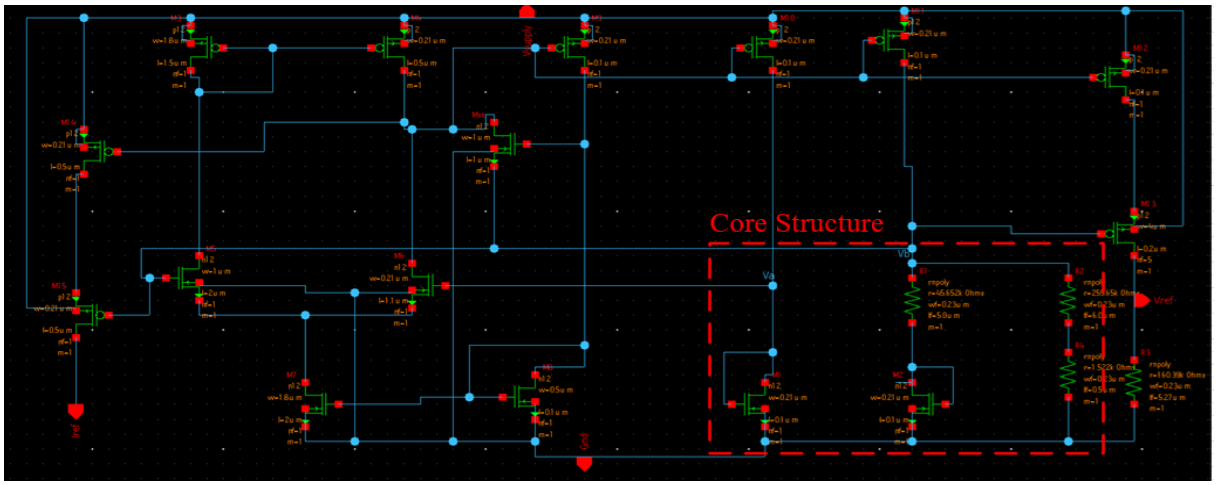


Figure 2. Bandgap reference circuit schematic and its core structure.

$$\frac{\partial V_T}{\partial T} = \frac{k}{q} \tag{2}$$

A positive temperature coefficient of current (PTAT) is generated across resistor R_1 due to the difference in the gate-source voltages of M1 and M2 NMOS transistors according to Equation 3 [4].

$$I_{R1} = \frac{\Delta V_{gs}}{\mathrm{R_1}} \tag{3}$$

$I_{R2,4}$ is proportional to the V_{gs1}, which is set equal to V_b. Thus, we can obtain the current with a negative temperature coefficient (CTAT) from Equation 4.

$$I_{R2,4} = \frac{V_{gs1}}{R_2+R_4} = \frac{V_a}{R_2+R_4} = \frac{V_b}{R_2+R_4} \tag{4}$$

The current I_{R1} with a positive temperature coefficient and the current $I_{R2,4}$ with a negative temperature coefficient together create the temperature-compensated current I_b.

$$I_b = I_{R1} + I_{R2,4} \tag{5}$$

Thus, the I_b current from the Equation 5 can be used as I_{ref} at any point in the circuit using the specified PMOS transistors. Figure 3 shows the layout of the designed BGR circuit occupying an area of 346 μm^2.

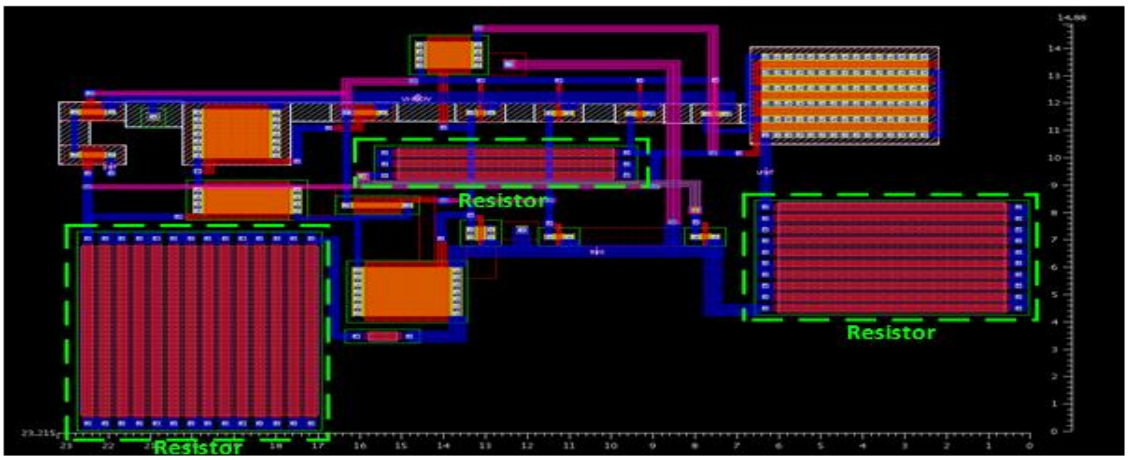


Figure 3. BGR layout design.

2.2 LDO Regulator

The LDO regulator circuit is designed to operate efficiently even when the difference between the input voltage and output voltage is low [17]. In the circuit, a PMOS-based output transistor is used to guarantee a low dropout

voltage and to enhance the stability of the output load. In Figure 4, which shows the general structure of the LDO voltage regulator, the PMOS transistor is connected to the input voltage and controls the output voltage. The PMOS transistor enters cut-off mode under high input voltage conditions, thereby reducing the output voltage. The output voltage of the error amplifier provides the control voltage for the PMOS transistor. This voltage makes certain that the desired output voltage is achieved. The error amplifier in the LDO circuit regulates the output voltage when the supply voltage is higher than the output.

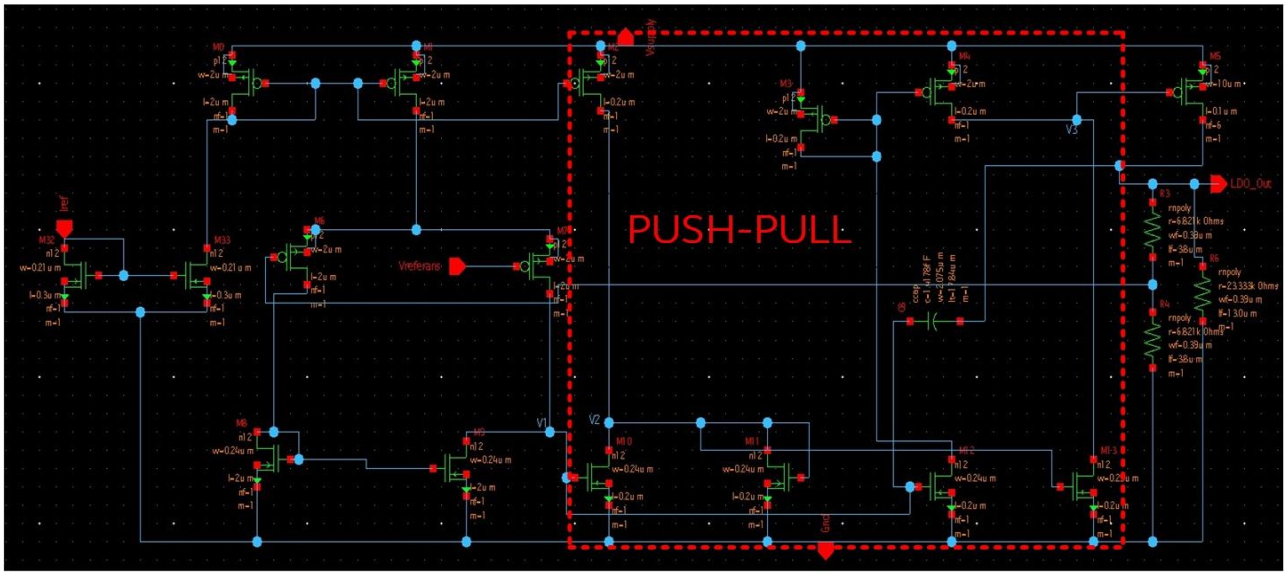


Figure 4. LDO circuit and PUSH-PULL structure.

In the circuit shown in Figure 4, the **M0**-**M13** MOSFETs are used as switching elements to control the current. The reference current provided by the BGR circuit to the LDO circuit is defined in the LDO circuit with a current source called I_{ref}. The resistors **R1**, **R2,** and **R3** with values of $6.82k\Omega$, $6.82k\Omega$ and $23.33k\Omega$ respectively regulate the output voltage. Additionally, a capacitor with a value of $1.41fF$ confirms system stability and improves the transient response of the system. V_1 and V_2 are fixed reference voltages, while V_3 determines the output voltage. **M0** and **M1** operate in a current mirror configuration providing a constant current. The reference current (I_{ref}) flows through M0 and is mirrored by M1, making the current passing through M1 equal to I_{ref}.

In addition to these MOSFETs, **M6**-**M9** compare the reference voltage (V_2) with the output voltage and create a feedback loop. The MOSFETs **M2**, **M3**, and **M4** together function as an error amplifier to carry on the **M5** MOSFET.

The M5 MOSFET supplies the current of load and regulates the output voltage. This voltage is fed back to the reference voltage through resistors. The circuit offers a stable and accurate output voltage even at low input-output voltage differences [8].

Figure 4 also shows the push-pull configuration used to increase the gate drive current dynamically when the load changes. This structure reduces power consumption and affords low forward gain and low output resistance [8].

$$V_{LDO\_Out} = \left(\frac{R_1}{R_2} + 1\right).V_{reference} \tag{6}$$

The output voltage obtained in the LDO voltage regulator circuit can be derived from Equation 6. This output voltage, which is 1.2V DC, serves as the supply source for the VCO circuit. The connection ensures that the VCO operates with a stable and regulated DC voltage source. Figure 5 shows the layout of the designed LDO regulator occupying an area of 783 μm^2.

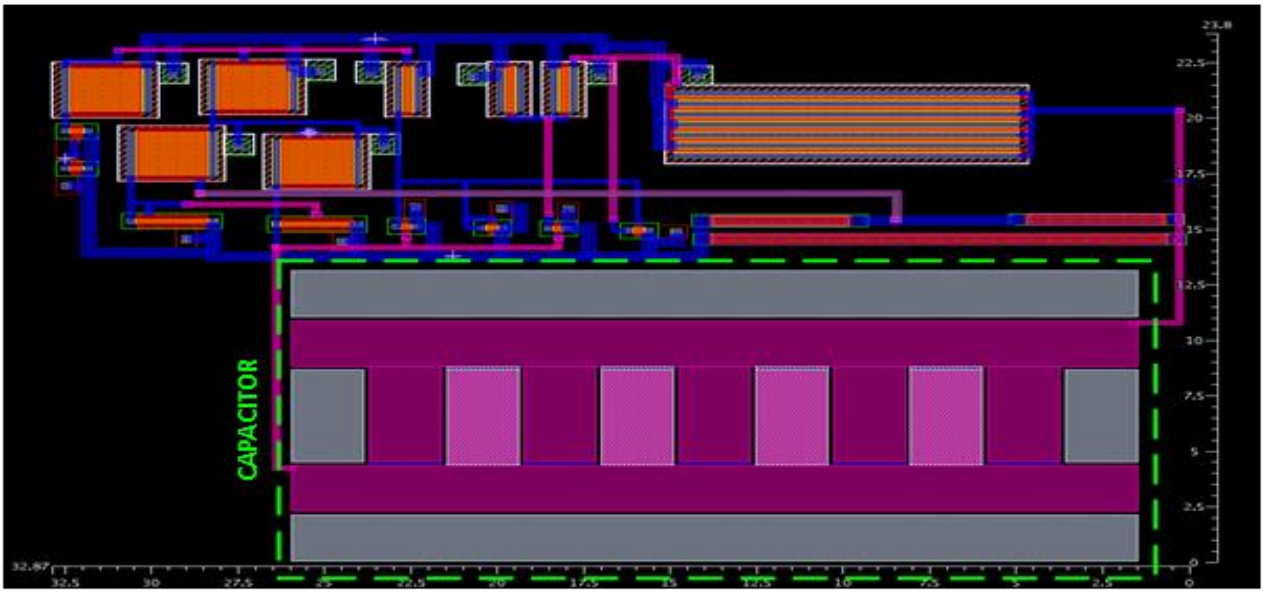


Figure 5. LDO layout design.

2.3 VCO

In this study, a CSVCO (Current Steering Voltage-Controlled Oscillator) is preferred as an oscillator structure that offers a wide tuning range and meets various performance requirements. The primary reason for using the CSVCO is that it supports a balanced solution among power consumption, area, and phase noise due to its wide tuning range [18].

Figure 6 shows the schematic view of the VCO circuit. The circuit consists of five differential delay cells and two buffer cells. The differential delay cells increase the oscillation frequency and decrease phase noise, while the buffer cells convert the oscillations into square waves.

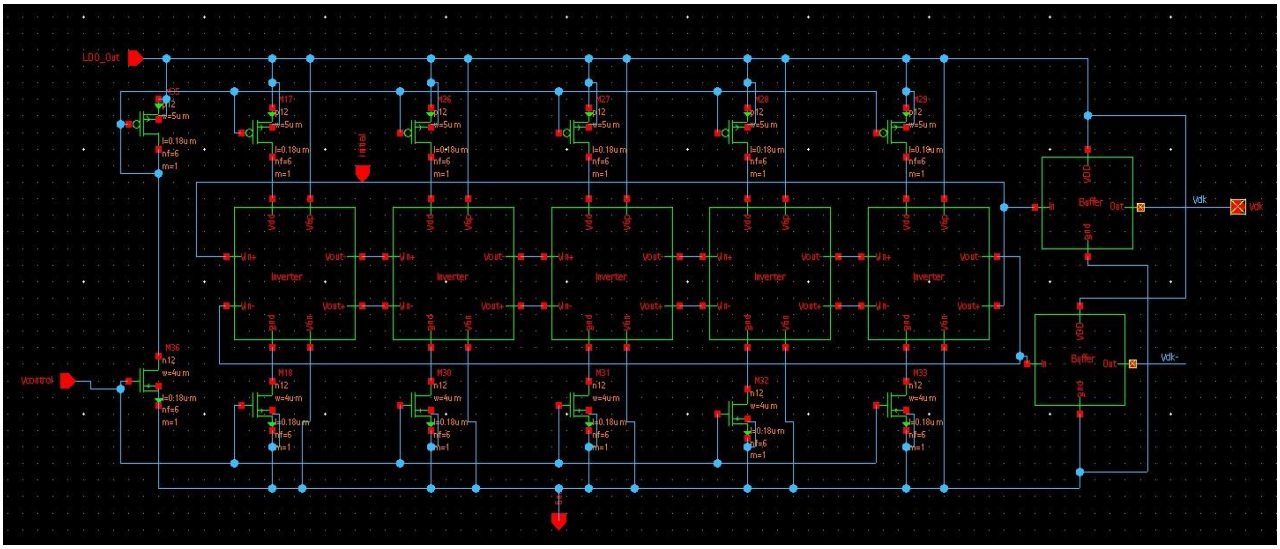


Figure 6. The schematic view of the VCO circuit together with the node voltages of the differential pairs.

Figure 7 shows the differential delay cell, which serves as a building block for the CSVCO. This circuit increases the oscillation frequency and keeps down the leakage power loss caused by phase noise. To maximize these benefits, five differential delay cells are used in the circuit.

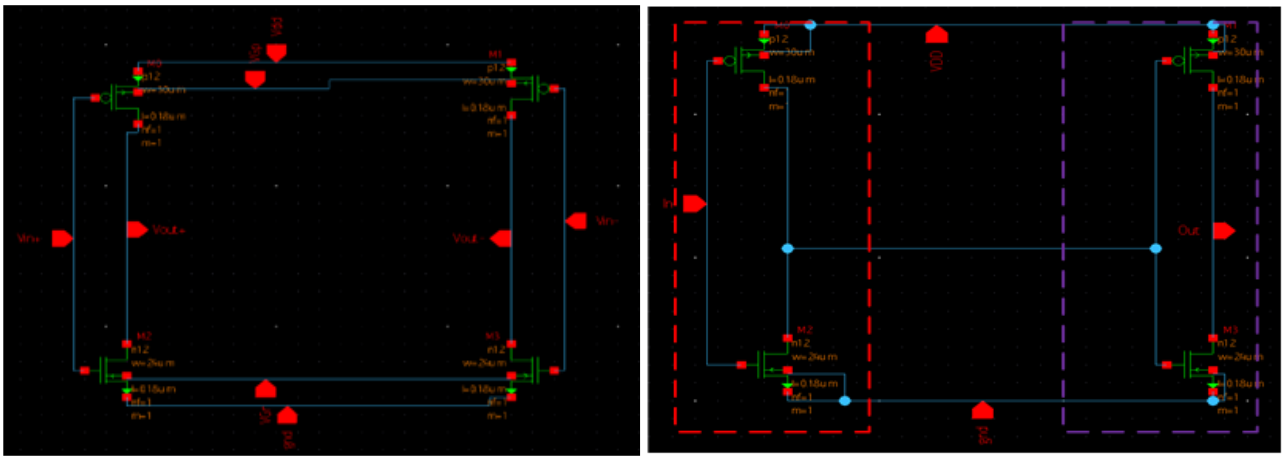


Figure 7. Differential delay cell and buffer circuit.

When the control voltage ($V_{control}$) of the current-starved VCO exceeds the threshold voltage, the M36 MOSFET turns on, and the current mirror MOSFETs **M36**, **M35**, **M17**, **M26**, **M27**, **M28**, and **M29** enter the active region. In the differential delay cell, the **M2** and **M3** (n-type) MOSFETs form the pulling network. The differential inverter switches on since the MOSFETs **M0**, **M1**, **M2**, and **M3** become active. The connection of the five differential delay cells in the CSVCO is made in series, with the $out+$ and $in-$ labels connected in series, while the $out-$ and $in+$ labels are also connected in the same manner. The output of the fifth inverter is fed back to the input of the first inverter, creating a continuous signal loop. As a result of this loop, the control voltage is inverted between each delay cell, and the CSVCO begins to produce oscillations.

In addition to all the processes, as the control voltage increases, the frequency of the oscillations also increases linearly, just like in a traditional VCO situation [13]. Figure 7 also shows the buffer circuit, formed by the series connection of the inverters shown in red and purple, which converts the sinusoidal oscillations produced by the differential cells in the CSVCO circuit into square pulses. Figure 8 shows the layout of the designed VCO circuit occupying an area of 1531 μm^2.

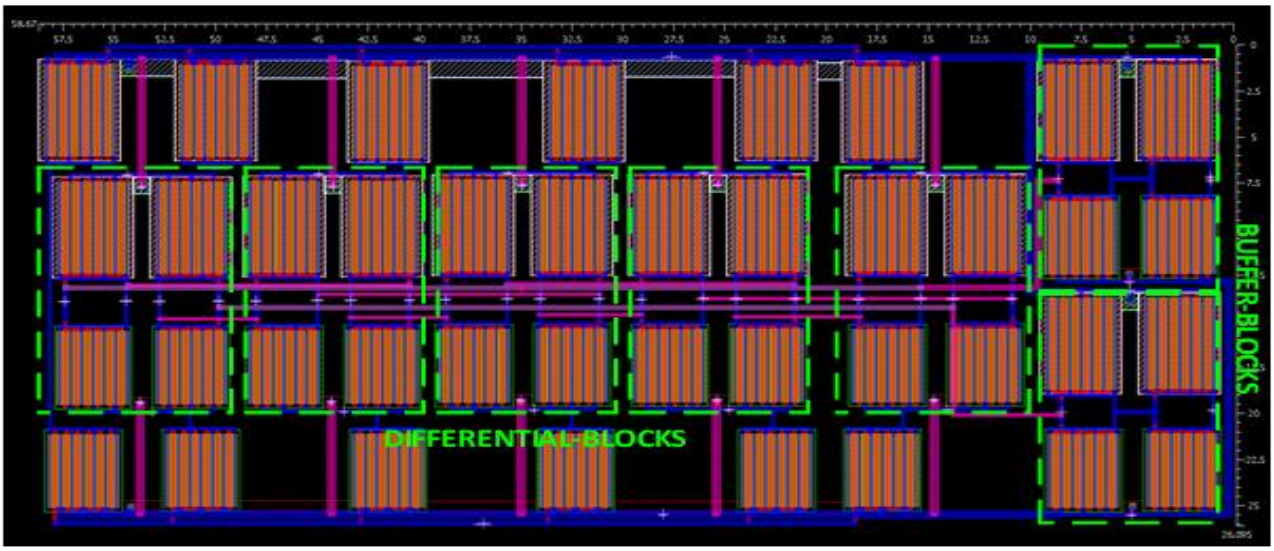


Figure 8. VCO layout design.

3. Results and Discussion

In this section, simulation results which are conducted using the Synopsys application to evaluate the functionality of the designs are presented. The layouts formed for the post-layout simulations of all designs have successfully passed the DRC and LVS checks.

3.1. BGR Simulations

In the BGR test environment, dc, tran, and xf analyses are used to meet the requirements. Among these analyses, the dc analysis is executed to determine the values of the reference voltage (V_{ref}) and the node voltages. By utilizing the sweep feature within the dc analysis, voltage variations dependent on temperature are observed, and the resulting voltage values are used to calculate the ppm value. The tran analysis was applied to obtain a time-dependent graph. This allows for the observation of both the reference voltage and its variations when the supply voltage (V_{supply}) decreases and increases by 10%. The xf analysis enabled us to determine the PSRR value. During this analysis, an 1V AC voltage was applied to the circuit's supply voltage.

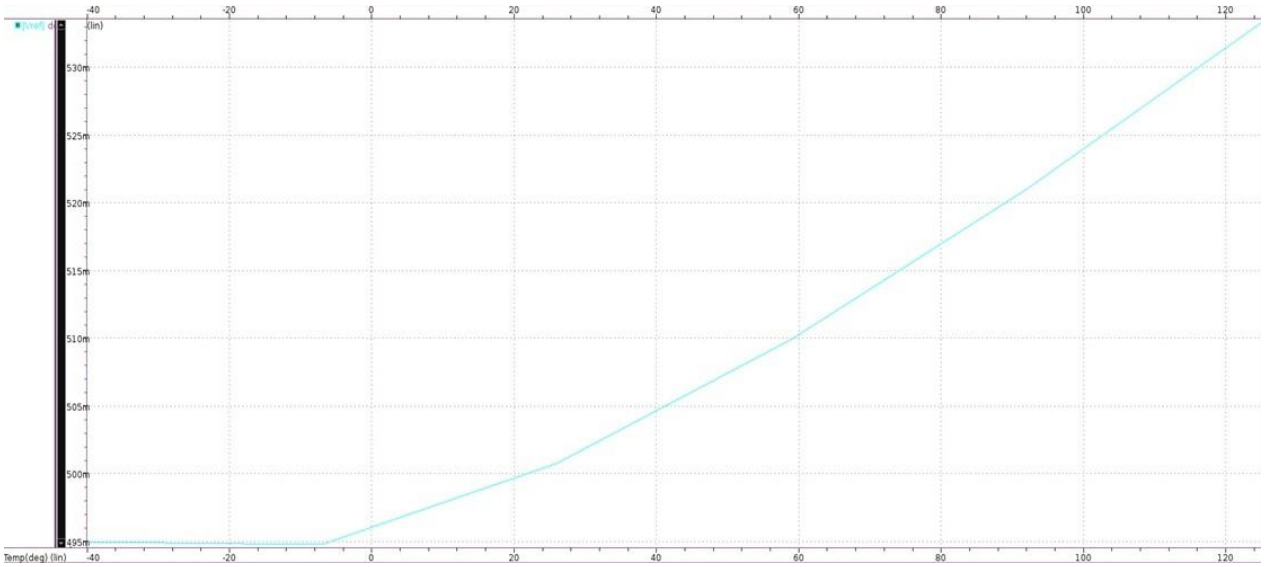


Figure 9. Temperature variation graph in the schematic design.

Figure 9 shows the temperature variation of the BGR schematic circuit between -40°C and 125°C for a 500 mV reference voltage. The reference voltage in this range remains between 495 mV and 533 mV.

$$TCV_o = \frac{V_{max} - V_{min}}{V_{nominal}(T_{max} - T_{min})} \cdot 10^6 \tag{7}$$

Based on the ppm calculation formula provided in Equation 7, the temperature variation of the circuit is estimated approximately as 460 $ppm/°C$. The same simulation is also carried out for the layout of the BGR circuit, which is close to the schematic results.

Table 1. BGR simulation results.

	Schematic Simulation Results	**Post-Layout Simulation Results**
Reference Voltage	501 mV	488 mV
PSRR	-2.4 dB	-2.9 dB
Temperature Coefficient	460 ppm/℃	509 ppm/℃
Power Consumption	0.185 mW	0.167 mW
Reference Voltage in Supply 1.8V±10%	In 1.8V+10%, 498 mV In 1.8V-10%, 503 mV	In 1.8V+10%, 485 mV In 1.8V-10%, 491 mV
Start-up Circuit	Added	Added

3.2. LDO Simulations

In the LDO test environment, dc, tran, and lstb analyses have been used to simulate important parameters of the circuit. Among these analyses, the dc analysis has been run to evaluate the output voltage and node voltages. The tran analysis has been applied to obtain graphical outputs. The lstb analysis has determined the loop gain and

phase margin. During this analysis, a supply voltage of 1V (AC) was applied to the circuit. By using the **dc** and **tran** analyses together, the power consumption, line regulation, and load regulation of the circuit is examined.

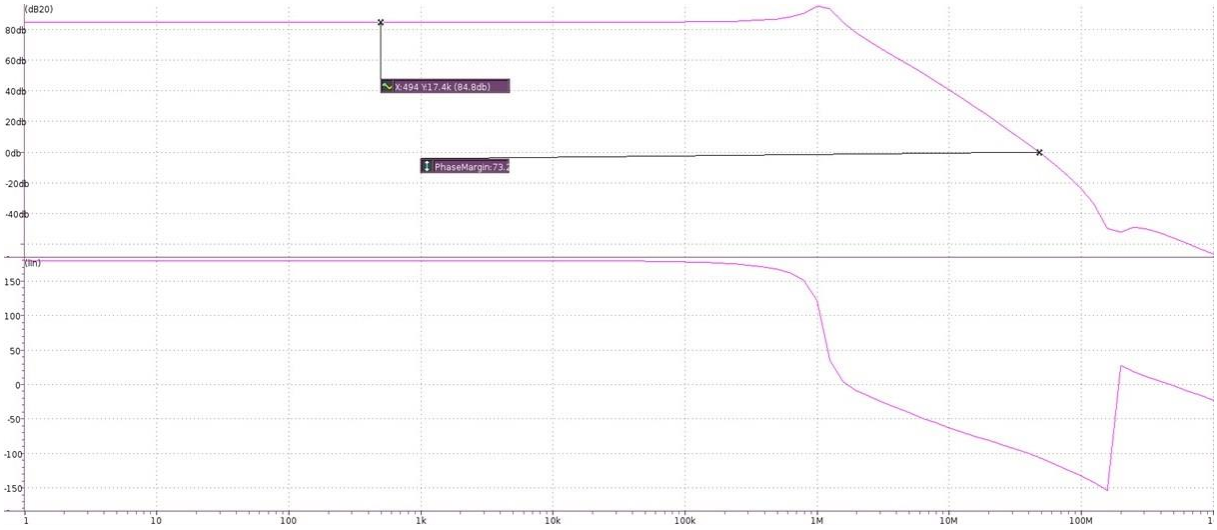


Figure 10. Loop gain and phase margin graph in the schematic design.

To get the loop gain and phase margin, a capacitor with a value of 500 pF was connected to the output of the LDO circuit, and a constant current of 1 mA was drawn using a current source from the output. Figure 10 shows the lstb analysis graph, where the loop gain of the LDO circuit is 84.8 dB, and the phase margin is 73.2°. When the LDO circuit has no output load, a maximum power consumption of 1.69 mW has been achieved.

Table 2. LDO simulation results.

	Schematic Simulation Results	**Post-Layout Simulation Results**
Output Voltage	1.2 V	1.2 V
Loop Gain and Phase Margin	84.8 dB and 73.2°	74.5 dB and 110°
Power Consumption	1.69 mW	1.67 mW
Output Voltage Against Current Pulses	1.56 V deviation	2.52 V deviation
Line Regulation	Constant Output Voltage	Constant Output Voltage
Load Regulation	Constant Output Voltage	Constant Output Voltage

3.3. VCO

In the VCO test environment, dc, tran, sn, and snnoise analyses have been used to simulate the circuit. The dc analysis was employed to observe the output voltage (V_{clk}) and the node voltages. The tran analysis aimed to visualize the time-dependent variation of the square pulse and its frequency value. To achieve this waveform, an 'initial condition' was provided to the circuit. The given initial condition was applied between the V_{in+} terminal of the first inverter and the V_{out+} terminal of the fifth inverter. Additionally, the rise and fall times were calculated and observed using this analysis. The sn and snnoise analyses were utilized to assess the phase noise values. Finally, a sweep analysis was performed to calculate the KVCO value.

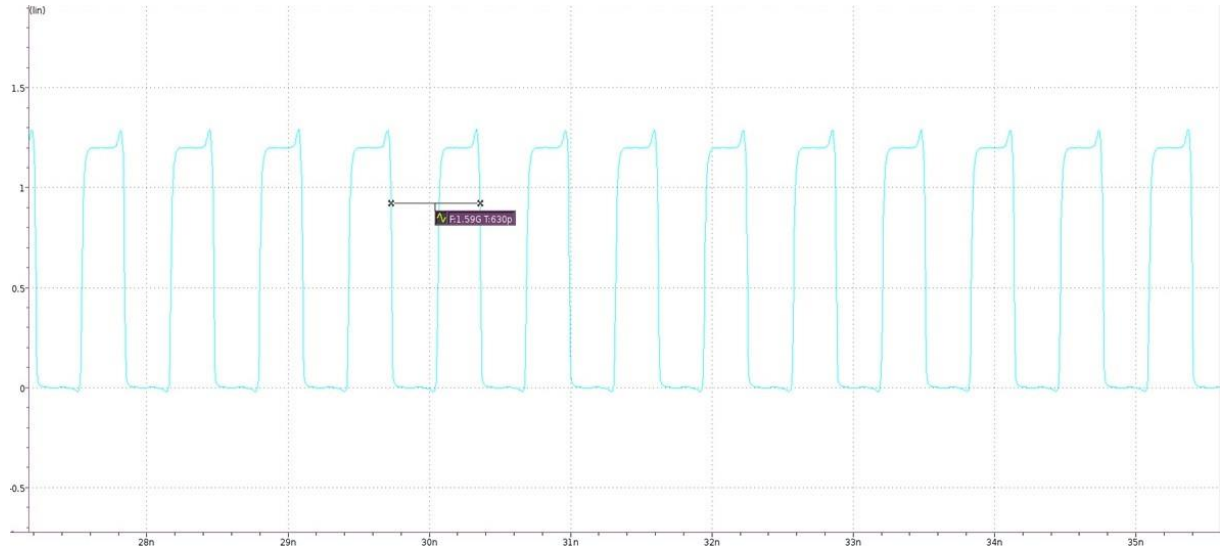


Figure 11. The operating frequency of the VCO schematic circuit.

Figure 11 shows the waveform produced by the VCO schematic circuit when it operates without a load. The frequency of the generated waveform has been observed to be 1.59 GHz. The output voltage (V_{clk}) of the circuit varies between 0 V and 1.2 V.

Table 3. VCO simulation results.

	Schematic Simulation Results	**Post-Layout Simulation Results**
Operating Frequency	1.59 GHz	1.26 GHz
Duty Cycle	43.7%	44.1%
Power Consumption	Max 13 mW	Max 12 mW
Range of Square Wave	0-1.2 V	0-1.23 V
Control Voltage	0.77 V	0.77 V
KVCO	733 MHz/V	567 MHz/V
Phase Noise	-97.1 dBc	-99.9 dBc
Rise and Fall Time at 1600MHz	0.195 ns	-

3.4. Entire System

The designed circuits are combined to get a stable oscillator structure as given in Fig.1. The simulations of the entire system are also performed to understand the performance. Figure 12 shows the layout of the entire system occupying an area of 3645 μm². This area represents the overall physical footprint of the system, including all components and interconnections.

Figure 12. Entire system layout design.

The total power consumption of the schematic of the entire circuit is simulated to be 21.5 mW while this value is 18.2 mW for the post-layout simulations. These values represent the total energy consumption of the system, considering all components and their activities during operation.

Table 4. Entire system simulation results.

	Schematic Simulation Results	**Post-Layout Simulation Results**
BGR Reference Current	-1.74 µA	Between -1.4 µA and-1.62 µA
LDO Output Voltage	0.361-1.57 V	1.11-1.25 V
VCO Operation Frequency	1.8 GHz	1.2 GHz
Power Consumption	Max 21.5 mW	Max 18.2 mW

4. Conclusions

This study presents the design and performance analyses of Bandgap Reference (BGR), Low Dropout Regulator (LDO), and Voltage Controlled Oscillator (VCO) circuits for low-power integrated systems. Our work presents an approach that simultaneously addresses the requirements of low power consumption, temperature stability, and frequency accuracy by integrating these three circuits. These features are particularly important in areas where power efficiency is critical, such as mobile devices and embedded systems, and our research expands upon the limited studies in the literature regarding the combined use of these circuits. The BGR circuit provides a stable reference current against temperature variations. These results validate that the BGR circuit offers temperature stability in line with previous studies, supporting its applicability in mobile and industrial applications. The LDO circuit delivers efficient power regulation with a low dropout voltage and possesses the ability to respond quickly to changes in load conditions, thus giving solutions for various power management requirements. This feature enhances the stability of the LDO circuit in integrated systems, ensuring long-lasting and reliable power management. The VCO circuit operates with low phase noise across a wide frequency range, offering a critical solution for communication systems. Its capability to generate a frequency with sufficient accuracy to meet signal synchronization requirements demonstrates that the VCO is suitable for applications in the field of communications. These findings demonstrate that the study serves as a fundamental work for temperature stability, power efficiency, and frequency accuracy in low-power systems. This work presents a new perspective on the combined use of BGR, LDO, and VCO circuits to improve the performance of integrated circuits, representing a significant step toward achieving more efficient and reliable performance in low-power systems. For future work, process variation analyses, advanced reliability studies, and actual silicon testing should be performed to validate the practical implementation and ensure robust performance under real-world conditions. These works will fill the gap between simulation results and commercial viability of the proposed integrated system.

Authors' Contributions

EB, UR, BE, EBS, YZ: Conceptualization, Methodology, Validation, Formal analysis, Investigation, Resources, Writing - Original Draft, Visualization (Authors contributed equally). **MYT**: Writing - Review & Editing, Validation, Supervision.

Declaration of Ethical Standards

The author(s) of this article declare that the materials and methods used in this study do not require ethical committee permission and/or legal-special permission.

Conflict of Interest

There is no conflict of interest in this study.

Funding Institution

Teknofest Chip Design Competition

References

[1] Razavi, B. (2021). The design of a low-voltage bandgap reference, IEEE Solid-State Circuits Magazine 13(3), 6-16.

[2] Banba, H., Shiga, H., Umezawa, A., Miyaba, T., Tanzawa, T., Atsumi, S., Sakui, K. (1999). A CMOS bandgap reference circuit with sub-1-V operation, IEEE Journal of Solid-State Circuits 34(5), 670-674.

[3] Pakravan, E., Mojarad, M., Mashoufi, B. (2023). A low-power bandgap voltage reference circuit with ultra-low temperature coefficient. In Proceedings of the 5th Iranian International Conference on Microelectronics (IICM2023), 16-20.

[4] Hongprasit, S., Sa-ngiamvibool, W., Aurasopon, A. (2012). Design of bandgap core and startup circuits for all CMOS bandgap voltage reference, Przegląd Elektrotechniczny (Electrical Review) 88(4a), 277-280.

[5] Lee, C.-L., Sidek, R. M., Rokhani, F. Z., Sulaiman, N. (2015). A low power bandgap voltage reference for low-dropout regulator. In Proceedings of RSM 2015.

[6] Khan, D., Basim, M., Qurrat-ul-Ain, Q., Shah, S. A. A., Shehzad, K., Verma, D., Lee, K. Y. (2022). Design of a power regulated circuit with multiple LDOs for SoC applications, Electronics 11(17), 2774.

[7] Bhuiyan, M. A. S., Hossain, M. R., Minhad, K. N., Haque, F., Hemel, M. S. K., Dawi, O. M., Reaz, M. B. I., Ooi, K. J. A. (2022). CMOS low-dropout voltage regulator design trends: An overview, Electronics 11(2), 193.

[8] Zhang, R., Liu, Z., Wang, X. (2021). A capacitor-less LDO with nested Miller compensation and bulk-driven techniques in 90 nm CMOS. In Proceedings of the 4th International Conference on Circuits, Systems and Simulation (ICCSS), 51-55.

[9] Magod, R., Suda, N., Ivanov, V., Balasingam, R., Bakkaloglu, B. (2017). A low-noise output capacitorless low-dropout regulator with a switched-RC bandgap reference, IEEE Transactions on Power Electronics 32(4), 2856-2864.

[10] Hajimiri, A., Lee, T. H. (1998). A general theory for phase noise in electrical oscillators, IEEE Journal of Solid-State Circuits 33(2), 179-194.

[11] Chang, Y.-H., Luo, Y.-L. (2024). CMOS voltage-controlled oscillator with complementary and adaptive overdrive voltage control structures, Electronics 13(2), 440.

[12] Anjum, N., Yadav, V. K. S., Nath, V. (2023). Design and analysis of a low power current starved VCO for ISM band application, International Journal of Microsystems and IoT 1(2), 82-98.

[13] Rahul, R., Thilagavathy, R. (2014). A low phase noise CMOS voltage-controlled differential ring oscillator. In Proceedings of the International Conference on Control, Instrumentation, Communication and Computational Technologies (ICCICCT), 1025-1028.

[14] Razavi, B. (2017). Design of analog CMOS integrated circuits (2nd ed.). McGraw-Hill.

[15] Ito, T. (2003). Research and development of advanced CMOS technologies, FUJITSU Scientific & Technical Journal 39(1), 3-8.

[16] Sangolli, S. S., Rohini, S. H. (2015). Design of low voltage bandgap reference circuit using subthreshold MOSFET. In Proceedings of the 5th Nirma University International Conference on Engineering (NUiCONE).

[17] Huang, C. H., Liao, W. C. (2020). A high-performance LDO regulator enabling low-power SoC with voltage scaling approaches, IEEE Transactions on Very Large Scale Integration (VLSI) Systems 28(5), 1141-1149.

[18] Dinesh, S., Bharadwaj, S. (2017). New modified current starved ring voltage controlled oscillator and frequency to voltage rectifier for noise suppression from 1–6 GHz in 180 nm technology, Procedia Computer Science 115, 756-763.