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Research Article

Gate-Drain Distance Optimization in Multi-Layer AlGaN High Electron Mobility Transistors: A Finite Element Analysis

Yasin Doğan[1], Osman Çiçek[2, *]

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[1]Kastamonu University, IT Department, Kastamonu, Turkey; yasindogan@kastamonu.edu.tr
[2]Kastamonu University, Department of Electrical and Electronics Engineering, Kastamonu, Turkey; ocicek@kastamonu.edu.tr
*****Corresponding author

Abstract: High Electron Mobility Transistors (HEMTs) based on wide band gap semiconductors and two-dimensional electron gas (2-DEG) channels are crucial for high power and radio frequency applications. Gallium nitride (GaN)-based HEMTs offer superior breakdown voltage, electron transport characteristics, and thermal conductivity for next-generation power electronics. This study investigates the effect of gate-drain distance (L_{gd}) on electronic characteristics of a multi-layer graded $Al_xGa_{1-x}N$ HEMT structure (x = 0.05-0.30) on Si substrate using finite element method simulation through SimuApsys modeling software. The L_{gd} parameter was systematically varied between 0.8 µm and 30 µm to analyze breakdown voltage (V_{br}), on-resistance (R_{on}), current-voltage characteristics, and electric field distribution. Simulation results reveal critical trade-offs: short L_{gd} (3-6 µm) provides low R_{on} and high current density ($I_{ds,max} \approx 3.95$ mA/mm) but lower V_{br} (~135V) due to concentrated electric fields, while long L_{gd} (24-30 µm) achieves high V_{br} (~380V) through distributed electric field profiles but with increased R_{on} and reduced current capacity (~0.65 mA/mm). Application-specific L_{gd} optimization guidelines are established: 3-6 µm for <200V applications, 12-24 µm for 200-350V, and ≥30 µm for >350V. This simulation approach enables effective device design optimization without expensive experimental fabrication.

Keywords: SimuApsys; HEMTs; finite element method; channel modulation effects; electronic parameters

Araştırma Makalesi

Çok Katmanlı AlGaN Yüksek Elektron Hareketliliği Transistörlerinde Kapı-Akaç Mesafesi Optimizasyonu: Sonlu Elemanlar Analizi

Özet: Geniş bant aralığı yarı iletkenlere ve iki boyutlu elektron gazı (2-DEG) kanallarına dayanan Yüksek Elektron Hareketlilik Transistörleri (HEMT'ler), yüksek güç ve radyo frekansı uygulamaları için çok önemlidir. Galyum nitrür (GaN) tabanlı HEMT'ler, yeni nesil güç elektroniği için üstün kırılma gerilimi, elektron taşıma özellikleri ve termal iletkenlik sunar. Bu çalışma, SimuApsys modelleme yazılımı aracılığıyla sonlu elemanlar yöntemi simülasyonu kullanarak Si substrat üzerinde çok katmanlı kademeli $Al_xGa_{1-x}N$ HEMT yapısının (x = 0.05-0.30) elektronik özellikleri üzerinde kapı-akaç mesafesinin (L_{gd}) etkisini araştırmaktadır. L_{gd} parametresi, kırılma voltajı (V_{br}), direnç (R_{on}), akım-gerilim özellikleri ve elektrik alan dağılımını analiz etmek için 0,8 µm ile 30 µm arasında sistematik olarak değiştirilmiştir. Simülasyon sonuçları kritik ödünleşimleri ortaya koymaktadır: kısa L_{gd} (3-6 µm) düşük R_{on} ve

yüksek akım yoğunluğu ($I_{ds,max} \approx 3,95$ mA/mm) sağlar, ancak yoğun elektrik alanları nedeniyle daha düşük V_{br} (~135V) sağlarken, uzun L_{gd} (24-30 μm) dağıtılmış elektrik alanı profilleri sayesinde yüksek V_{br} (~380V) sağlar, ancak R_{on} artar ve akım kapasitesi azalır (~0,65 mA/mm). Uygulamaya özel L_{gd} optimizasyon kılavuzları oluşturulmuştur: <200V uygulamalar için 3-6 μm, 200-350V için 12-24 μm ve >350V için ≥30 μm. Bu simülasyon yaklaşımı, pahalı deneysel üretim olmadan etkili cihaz tasarımı optimizasyonu sağlar.

Anahtar Kelimeler: SimuApsys; HEMT'ler; sonlu elemanlar yöntemi; kanal modülasyonun etkileri; elektronik parametreler

1. Introduction

High Electron Mobility Transistors (HEMTs) stand out as a groundbreaking technology in microwave, radio frequency (RF), and high power density applications. The fundamental advantage of these structures lies in the high electron mobility provided by two-dimensional electron gas (2-DEG) channels and the superior electrical properties of wide band gap (WBG) semiconductor materials. Thanks to modern production technologies, it is now possible to manufacture integrated circuits containing billions of transistors without a single failure and capable of operating continuously for thousands of hours [1].

Gallium Nitride (GaN)-based semiconductors offer a wide bandgap (3.4 eV for GaN to 6.2 eV for AlN), high critical electric field (1-3×10^6 V/cm), exceptional electron transport characteristics (2.2×10^7 cm/s saturated electron drift velocity), and high thermal conductivity, making them ideal candidates for power electronics [2]. The most important feature that distinguishes GaN from other WBG semiconductors is the formation of a high-density 2-DEG spontaneously and through piezoelectric polarisation effects without the need for an external excitation layer in the channel. In the AlGaN/GaN heterostructure, the high conduction band offset and strong piezoelectric properties enable high layer carrier densities of the order of 0.5 to 2×10^{13} cm^{-2} to be achieved [2]. While materials such as GaAs or InP are preferred for high-frequency (>100 GHz) applications, GaN-based HEMTs are indispensable in high-power applications due to their superior power management and ability to operate at high temperatures (up to 1000°C). In GaN HEMT structures, which are seen as the cornerstone of next-generation power electronics systems, intensive work continues on improving critical parameters such as breakdown voltage (V_{br}), cut-off frequency (f_T) and high-temperature stability [3].

The performance of GaN HEMT structures depends on the careful design of each layer of the multilayer epitaxial structure. The substrate is one of the most fundamental parameters affecting device performance. Silicon (Si) is preferred for industrial applications due to its low cost and large wafer availability, while 4H-SiC substrates offer high thermal conductivity, providing advantages in high-power applications. The nucleation layer is grown as AlN, AlGaN, or thin GaN to reduce lattice mismatch and thermal stress between the substrate and the channel, minimising dislocation density [4].

The buffer/channel layer is the active region where 2-DEG is formed and must have high resistance, low defect density and a smooth surface morphology. Defects in the buffer layer trap 2-DEG electrons, cause current leakage and current drop-outs, thereby preventing high output power and breakdown voltage from being achieved [5, 6]. It is grown to a thickness of 1-2 μm for optimal performance. Since

conventional unintentionally doped GaN channel layers exhibit insufficient resistance, C-doped GaN or high-quality AlN buffer layers are used to obtain a high-resistance semi-insulating buffer [2].

The spacer layer is positioned between the buffer and barrier layers and is typically grown as 1–2 nm of AlN. This layer increases carrier mobility by reducing interfacial roughness and alloying defect scattering, and spatially separates the Coulomb interactions between 2-DEG electrons and ionised atoms in the barrier layer [7, 8]. The barrier layer is an AlGaN structure with a wider bandgap than the buffer layer and plays a central role in the formation of the 2-DEG due to its strong spontaneous and piezoelectric polarisation properties. Al concentration and barrier thickness directly determine the 2-DEG density; low Al concentration results in insufficient 2-DEG density, while excessively high concentration leads to an increase in interface defects [9]. For optimal performance, it is typically grown with 20-30% Al content and a thickness of 20-30 nm. The cap layer is grown with a thickness of 1-5 nm as GaN or InGaN, increasing long-term reliability by reducing gate leakage currents, increasing the Schottky barrier height, and preventing surface oxidation [10, 11].

The widespread adoption of GaN-based HEMT technology faces obstacles such as long-term reliability issues caused by crystal growth, dislocation density, defect centres, and production costs. Effective thermal management and accurate prediction of temperature distribution are particularly critical at high power densities [11]. Nevertheless, advances in metallurgy and materials science have made high-quality epitaxial growth possible on different substrates [12, 13].

The V_{br} is the most critical parameter determining device performance in power electronics applications. The V_{br} of GaN HEMTs is significantly influenced by the interaction between the source-drain distance (L_{sd}), gate-drain distance (L_{gd}), and gate-source distance (L_{gs}). Smaller L_{sd} or L_{gd} result in a higher electric field when voltage is applied, increasing the potential for avalanche breakdown. In this process, charge carriers in the semiconductor gain sufficient energy from the strong electric field to create additional carriers through collision ionisation, causing a sudden increase in current [2]. However, increasing L_{sd} or L_{gd} leads to higher on-resistance (R_{on}) values and increased conduction losses. Therefore, the primary objective is to achieve high V_{br} with the minimum possible L_{sd} and L_{gd}.

While the V_{br} values obtained in GaN HEMT structures in the early 2000s were limited to approximately 700V, in recent years they have been increased to levels of up to 10 kV [2]. Zhang et al. (2000) obtained 570V V_{br} with 13 μm L_{sd} and 0.5 μm gate length [14]. Nanjo et al. (2013) achieved 3000V V_{br} using the back barrier technique; the $In_{0.17}Al_{0.83}N$/GaN heterostructure was grown by MOCVD on a semi-insulating 4H-SiC substrate [15]. Lee et al. (2012) achieved an on-resistance value of 4.25 mΩ·cm² at 30 μm L_{gd} with an AlN nucleation layer, a 0.85 μm AlGaN back barrier containing 4% Al, and a 20 nm GaN channel [16].

Among V_{br} improvement strategies, high-k passivation layers are prominent. Compared to conventional materials such as Si_3N_4 or SiO_2, materials with high dielectric constants such as HfO_2 provide significantly higher V_{br}. Günes et al. (2023) achieved a OFF-state V_{br} of 88 V at V_G = -6 V with an ultrathin HfO_2 coating layer [17]. Cheng et al. (2021) increased the average V_{br} from 68.9 V to 121.5 V with a high dielectric constant (192) BZN passivation lay er [18].

Field plates (FP) structures increase the V_{br} by reducing the maximum electric field along the channel. The FPs are categorised as gate (G-FP), source (S-FP) and drain (D-FP) field plates according to

their placement. The combination of G-FP and S-FP is critical for the efficient increase of V_{br} [2]. Xie et al. (2012) achieved a forward blocking voltage of 375 V at V_{gs} = -5 V with a gate length of 0.8 μm and L_{gd} of 6 μm, while reducing the parasitic gate-source capacitance using a source-coupled air bridge FP-based AlGaN/GaN HEMT [19].

Rear barrier and channel optimisation also contribute to Vbr improvement. A well-designed rear barrier increases V_{br} by preventing electron tunnelling [2]. Baliga's Figure-Of-Merit (BFOM = V^2_{br}/R_{on}) is used to evaluate the trade-off between V_{br} and R_{on}. A review of the literature shows that the formation of a back barrier and AlN channel/buffer layers significantly increase BFOM values (Çiçek ve Badali, 2024).

In this study, the L_{gd} of the identified HEMT structure was determined at different gate angles. Using the finite element method, values such as V_{br}, current-voltage (I_{ds}-V_{gs}), and R_{on} were calculated using the Crosslight SimuApsys modelling programme in terms of channel modulation. In order to reduce losses arising from the process technology, an effective simulation model was employed to analyse the electronic characteristics of the structure designed from different angles, aiming to minimise expenses such as the procurement of expensive equipment and to obtain effective research results.

2. Experimental Procedure

2.1. HEMT structure

Source-drain (L_{sd}), gate-drain (L_{gd}) and gate-source (L_{gs}) distances are some of the physical factors that affect the electronic parameters of an HEMT in terms of channel modulation. The HEMT structure given below was used to investigate the effect of the L_{gd} length parameter. In this regard, the necessary material definitions were made.

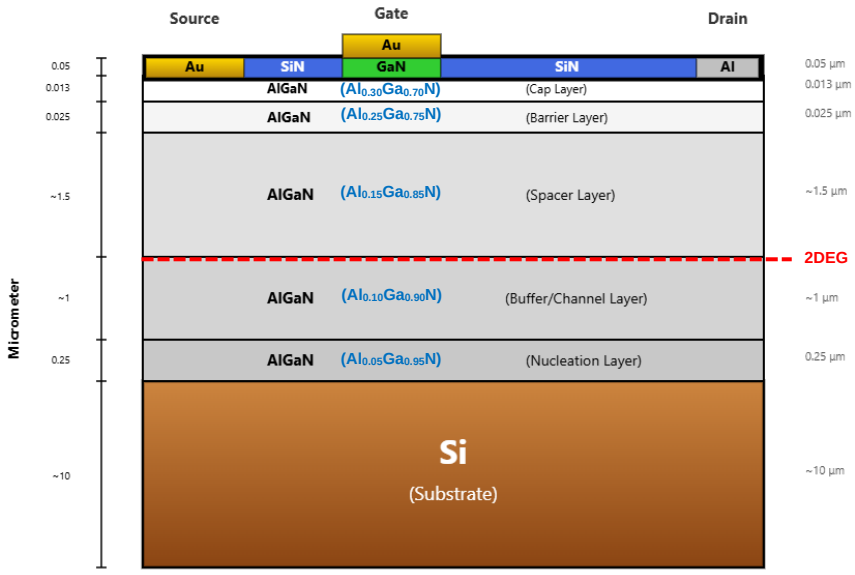

Figure 1. The simulated multi-layer AlGaN HEMT structure.

The schematic cross-section of the multi-layer AlGaN HEMT epitaxial structure with Si substrate is shown in Figure 1. The proposed HEMT structure consists of multiple epitaxial layers on a Si substrate (T_{sub}) with a total substrate thickness of approximately 10 μm.

For the device structure, the epitaxial layers from bottom to top are as follows: First, an $Al_{0.05}Ga_{0.95}N$ nucleation layer (T_{nuc}) with a thickness of 0.25 μm is defined on the Si substrate to reduce lattice mismatch and mechanical stress. Above this, an $Al_{0.10}Ga_{0.90}N$ buffer/channel layer (T_{buff}) with a thickness of approximately 1 μm is modeled to provide high resistivity and low defect density, which is critical for 2-DEG formation and device performance. An $Al_{0.15}Ga_{0.85}N$ spacer layer (T_{spacer}) of approximately 1.5 μm is then configured to minimize interface roughness scattering and alloy disorder scattering, thereby enhancing carrier mobility. Subsequently, an $Al_{0.25}Ga_{0.75}N$ barrier layer (T_{bar}) with a thickness of 0.025 μm is implemented, which plays a central role in 2-DEG formation through strong spontaneous and piezoelectric polarization effects. Finally, an $Al_{0.30}Ga_{0.70}N$ cap layer (T_{cap}) with a thickness of 0.013 μm is modeled on top to reduce gate leakage current, increase Schottky barrier height, and prevent surface oxidation.

The metal contact and passivation layers with a total thickness of 0.05 μm are configured on the cap layer. The source contact consists of Au (gold) with ohmic contact properties, while the drain contact is made of Al (aluminum). The gate contact features an Au metallization positioned on a GaN layer, forming a Schottky contact to control the electron density in the channel. SiN (silicon nitride) passivation layers are placed between the contacts to enhance breakdown voltage by modulating the electric field distribution and reducing surface leakage current.

Table 1. Main Structural Parameters of the simulated multi-layer AlGaN HEMT

Parameter	***Symbol***	**Value**
SUBSTRATE		
Si Substrate Thickness	T_{sub}	~10 μm
EPITAXIAL LAYERS		
$Al_{0.05}Ga_{0.95}N$ Nucleation Layer Thickness	T_{nuc}	0.25 μm
$Al_{0.10}Ga_{0.90}N$ Buffer/Channel Layer Thickness	T_{buff}	~1 μm
$Al_{0.15}Ga_{0.85}N$ Spacer Layer Thickness	T_{spacer}	~1.5 μm
$Al_{0.25}Ga_{0.75}N$ Barrier Layer Thickness	T_{bar}	0.025 μm (25 nm)
$Al_{0.30}Ga_{0.70}N$ Cap Layer Thickness	T_{cap}	0.013 μm (13 nm)
CONTACT & PASSIVATION		
Metal Contact & Passivation Layer Thickness	$T_{contact}$	0.05 μm
Source Contact Material	-	Au (Ohmic)
Gate Contact Material	-	Au/GaN (Schottky)
Drain Contact Material	-	Al (Ohmic)
Passivation Material	-	SiN
GEOMETRIC PARAMETERS (VARIABLE)		
Gate Length	L_g	~1 μm
Gate-Drain Distance	L_{gd}	0.8-30 μm
Source-Drain Distance	L_{sd}	Variable
Gate-Source Distance	L_{gs}	0.8 μm

For the optimization study, the L_{gd} and the L_{sd} are systematically varied to investigate their effects on V_{br}, R_{on}, and other critical device parameters. The gate length (L_g) of 1 µm is maintained at a fixed value during the optimization process. The main structural parameters for the device are summarized in Table 1.

2.2. Finite Element Method

In device simulation, voltages, currents and loads are calculated using equations that describe the transmission mechanisms and carrier distribution. The physical characteristics of the device are simulated as a uniform discrete grid. The appearance of the simulated structure's mesh is shown in Figure 2.

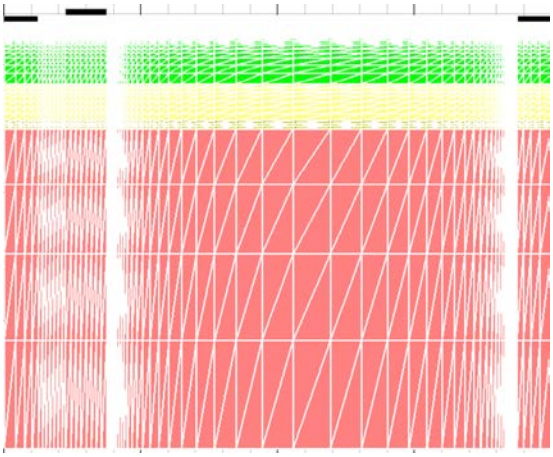

Figure 2. The multi-layer AlGaN Structure's Mesh Form

The simulation domain was discretized using an adaptive triangular mesh with selective refinement in critical regions. The mesh density was particularly enhanced at the multi-layer AlGaN heterojunction interface (mesh spacing < 0.5 nm vertically) where the 2-DEG channel forms, at the gate edges (mesh spacing < 2 nm) where electric field concentration occurs, and in the gate-drain drift region (mesh spacing 5-10 nm) to capture electric field distribution accurately. The total number of mesh elements ranged from approximately 50,000 for the shortest L_{gd} configuration to 120,000 for the longest L_{gd} = 30 µm structure. Mesh convergence studies were performed to ensure that further refinement produced less than 1% variation in critical parameters such as $I_{ds,max}$ and V_{br}.

3. Results and Discussion

The L_{sd}, L_{gd} and L_{gs} distances are some of the physical factors that affect the electronic parameters of an HEMT in terms of channel modulation. To investigate the effect of the L_{gd} length parameter, analyses of R_{on}, the threshold voltage (V_{th}), current-coltage curves, the V_{br}, and Electric Field were performed for each structure by increasing the distance between the gate and drain for the HEMT structure shown in Figure 1.

R_{on} or spesific resistance is a very important parameter for power devices. Since power devices require high voltage and high current capability, the power consumed in the power device is expressed as follows [20]:

$$P = I_{ds}V_{ds} = I_{ds}^2 R_{on} \quad (3.1)$$

Figure 3 presents the output characteristics (I_{ds}-V_{ds}) of the multi-layer AlGaN HEMT for various gate-drain distances (L_{gd} = 0.8, 3, 6, 12, 24, and 30 μm) at a constant gate-source voltage of V_{gs} = 3V. The simulation results demonstrate that L_{gd} significantly influences the drain-source current and specific on-resistance (R_{on}) of the device.

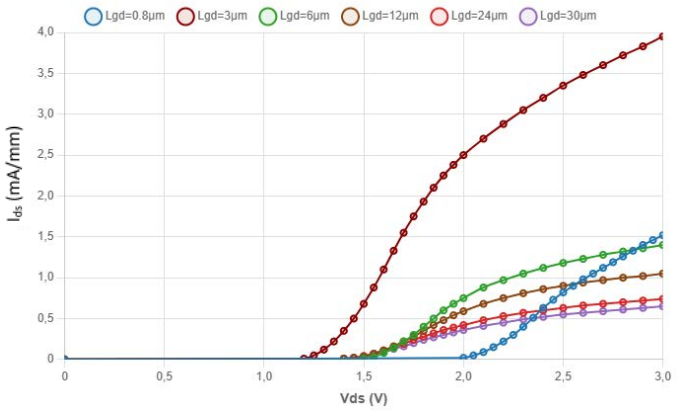

Figure 3. The I_{ds}-V_{ds} characteristics for various L_{gd} distances at V_{gs}=3V.

The maximum drain-source current ($I_{ds,max}$) decreases systematically as L_{gd} increases. At V_{ds} = 3V, the L_{gd} = 3 μm configuration exhibits the highest current density (~3.95 mA/mm), while the L_{gd} = 30 μm configuration shows the lowest value (~0.65 mA/mm). This trend is attributed to the increased drift region length with larger L_{gd}, which elevates the series resistance and reduces current carrying capacity.

All configurations display typical HEMT behavior with distinct linear and saturation regions. In the linear region, the slope of the I_{ds}-V_{ds} curves, which is inversely proportional to R_{on}, decreases significantly with increasing L_{gd}. The L_{gd} = 3 μm configuration demonstrates the steepest slope, indicating the lowest R_{on} and highest conductivity. Conversely, longer L_{gd} values (24-30 μm) exhibit substantially higher R_{on} but are expected to provide higher V_{br} due to improved electric field distribution.

The results clearly illustrate the classical R_{on}-V_{br} trade-off in power device design: shorter L_{gd} values minimize conduction losses but increase breakdown risk, while longer L_{gd} values enhance voltage blocking capability at the expense of higher conduction losses. The optimal L_{gd} selection depends on the specific application requirements, with L_{gd} = 3 μm suitable for low-voltage high-current applications, L_{gd} = 6-12 μm appropriate for medium-power applications, and L_{gd} = 24-30 μm preferable for high-voltage applications. The overall device performance should be evaluated using Baliga's Figure-of-Merit (BFOM = V^2_{br}/R_{on}) to balance these competing parameters effectively.

Increasing the V_{gs} value in the negative direction causes the I_{ds} current between the drain and source to decrease by depleting the channel under the gate. The minimum voltage value that pinches off the current between the drain and source by setting the charge density to zero in the channel under the gate is called the threshold voltage and is denoted as V_{th} [21]. Using the finite element method, V_{th} and G_m values were obtained for different L_{gd} values in terms of channel modulation and are given in Figure 4.

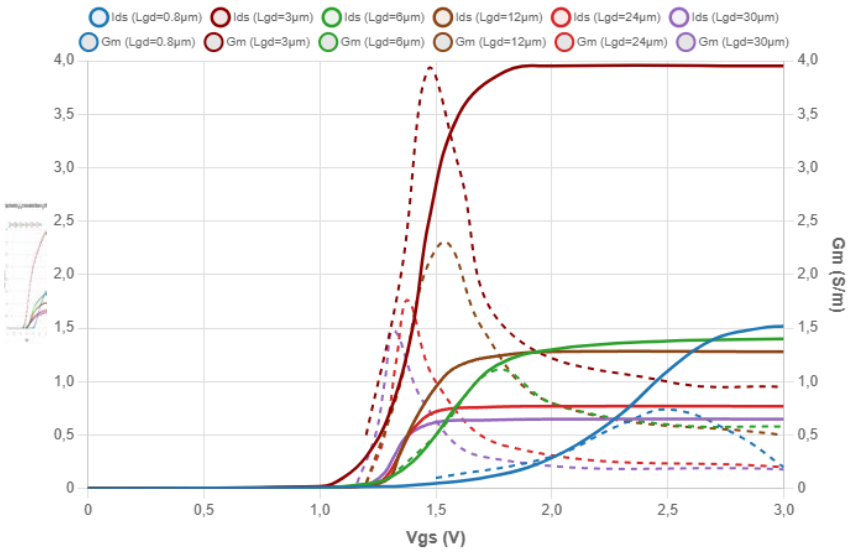

Figure 4. The I_{ds}-V_{gs} and G_m characteristics for various L_{gd} distances.

Figure 4 presents the I_{ds}-V_{gs} and G_m for various L_{gd} values at V_{ds} = 3V. The threshold voltage (V_{th}) shows minor variation across all configurations, ranging from 1.16V to 1.28V, indicating that L_{gd} primarily affects drift region resistance rather than the fundamental channel formation mechanism.

The maximum drain current ($I_{ds,max}$) decreases systematically with increasing L_{gd}: from 3.95 mA/mm for L_{gd} = 3 μm to 0.65 mA/mm for L_{gd} = 30 μm. This trend directly correlates with increased series resistance in longer drift regions. The G_m exhibits significant variation, with L_{gd} = 3 μm achieving the highest peak G_m of 3.93 S/m at $V_{gs} \approx$ 1.47V, demonstrating superior amplification capability. In contrast, longer L_{gd} configurations (24-30 μm) show reduced G_m values (~1.48-1.76 S/m), indicating lower switching speed and gain.

The results confirm that shorter L_{gd} values optimize current drive capability and conductance for high-speed and RF applications, while longer L_{gd} configurations are necessary for high-voltage applications despite sacrificing amplification performance. The consistent subthreshold slopes across all geometries suggest uniform interface quality, with device performance primarily governed by the L_{gd}-dependent drift region resistance.

Figure 5 presents the output characteristics (I_{ds}-V_{ds}) for six different gate-drain distances (L_{gd} = 0.8, 3, 6, 12, 24, and 30 μm) across a range of gate-source voltages (V_{gs} = 0, 1, 2, 3, and 4V) at V_{ds} up to 10V. The results comprehensively demonstrate the combined effects of geometric scaling and gate voltage modulation on device performance.

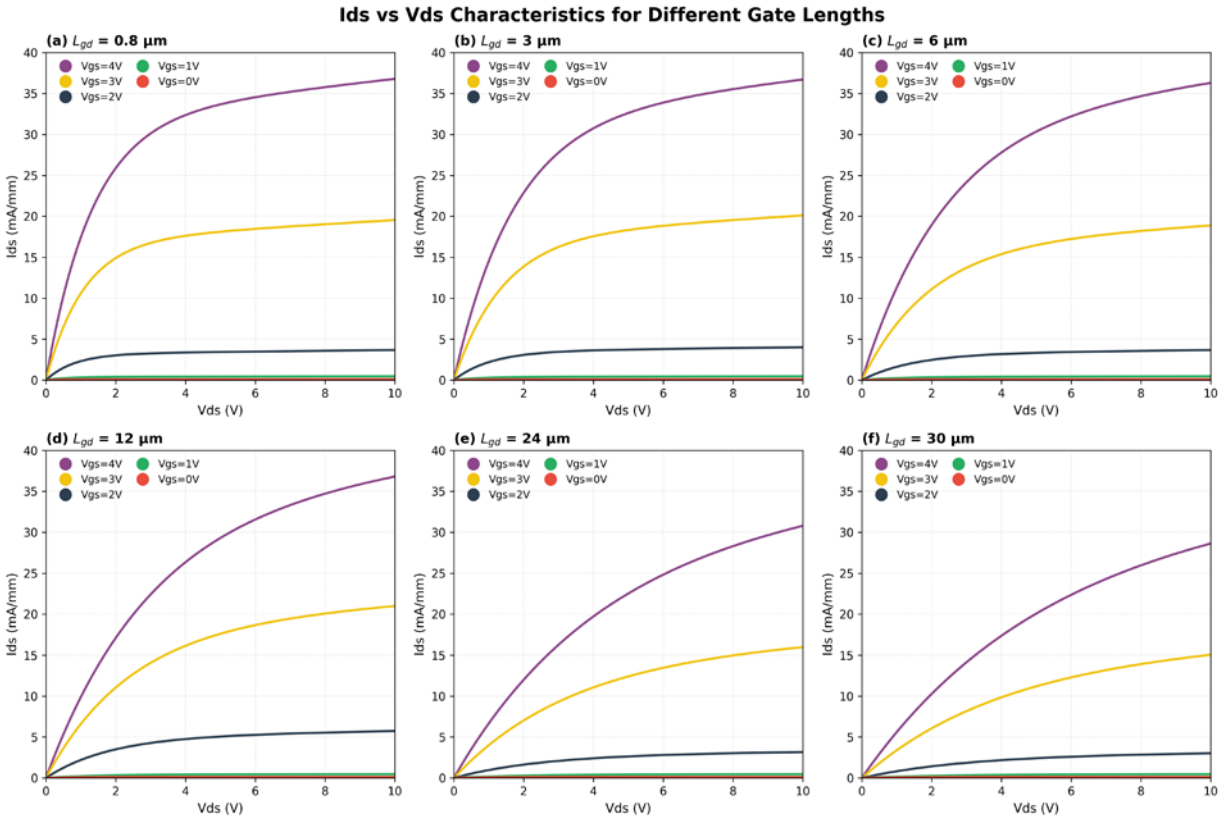

Figure 5. The output characteristics (I_{ds}-V_{ds}) of multi-layer AlGaN HEMT for various L_{gd} distances.

For all L_{gd} configurations, increasing V_{gs} from 0V to 4V systematically enhances the drain current, confirming effective gate control over the 2-DEG channel. At V_{gs} = 0V, the device remains in the OFF-state with negligible leakage current across all configurations. As V_{gs} increases, the device transitions through the subthreshold region and enters strong inversion, with current levels scaling proportionally to the applied gate voltage. This consistent gate modulation behavior across different L_{gd} values indicates robust electrostatic control regardless of drift region length.

The saturation current levels vary dramatically with L_{gd}. At maximum gate voltage (V_{gs} = 4V), the L_{gd} = 3 µm configuration achieves the highest saturation current (~33 mA/mm), while the L_{gd} = 30 µm configuration exhibits significantly lower values (~27 mA/mm). This trend becomes more pronounced at lower gate voltages, where the increased series resistance in longer L_{gd} structures more severely limits current flow. The steeper initial slopes in shorter L_{gd} configurations indicate lower R_{on} values, favorable for high-efficiency switching applications.

All configurations display typical HEMT behavior with distinct linear and saturation regions. In the linear region, the slope of the I_{ds}-V_{ds} curves, which is inversely proportional to R_{on}, decreases significantly with increasing L_{gd}. The L_{gd} = 3 µm configuration demonstrates the steepest slope, indicating the lowest R_{on} and highest conductivity. Conversely, longer L_{gd} values (24-30 µm) exhibit substantially higher R_{on} but are expected to provide higher V_{br} due to improved electric field distribution.

The intrinsic drain-saturation voltage (V_{dsat}) can be approximated using the relation $V_{dsat} \approx v_{sat} \cdot L_g/\mu_n$, where v_{sat} is the saturation velocity of electrons in GaN (~2.2×10^7 cm/s), L_g is the gate length (1 µm), and µn is the low-field electron mobility (~1500 cm²/V·s) [22] [23] [24]. This yields $V_{dsat} \approx 1.5$ V, which

remains relatively constant across all L_{gd} configurations as it is determined by the gate region physics rather than the drift region length. However, the apparent knee voltage, where the I_{ds}-V_{ds} curves transition to saturation, increases significantly with L_{gd} due to the higher series resistance in the drift region [22]. The voltage drop across the drift region resistance ($V_{drift} = I_{ds} \cdot R_{on\_drift}$) adds to the intrinsic V_{dsat}, resulting in $V_{knee} \approx V_{dsat} + I_{ds} \cdot R_{on\_drift}$. Since R_{on} is proportional to L_{gd}, longer drift regions require higher drain voltages to reach apparent current saturation. Additionally, the lateral electric field ($E_{lat} \approx V_{ds}/L_{gd}$) must be sufficient to maintain carrier transport through the entire drift length, and longer L_{gd} devices exhibit more gradual saturation characteristics due to extended depletion region dynamics and channel length modulation effects. Therefore, while the intrinsic V_{dsat} remains approximately 1.5 V for all configurations, L_{gd} = 30 μm devices require $V_{ds} \approx$ 15-20 V to reach apparent saturation, compared to $V_{ds} \approx$ 3-5 V for L_{gd} = 3 μm devices. This relationship explains the observed shift in saturation knee voltage with increasing drift region length while maintaining the fundamental velocity saturation physics in the channel region beneath the gate [23].

The comprehensive comparison reveals fundamental design trade-offs: L_{gd} = 3-6 μm configurations optimize current drive capability and switching speed, making them suitable for high-frequency and high-current applications. Conversely, L_{gd} = 24-30 μm configurations, while exhibiting reduced current levels, are expected to provide superior breakdown voltage characteristics essential for high-voltage power electronics. The intermediate L_{gd} values (12 μm) offer balanced performance, potentially suitable for medium-power applications requiring compromise between R_{on} and V_{br}.

Figure 6 presents the I_{ds}-V_{br} graph based on OFF-state breakdown characteristics (I_{ds}-V_{ds}) for various L_{gd} values. The breakdown voltages were extracted from OFF-state I-V characteristics by performing drain voltage sweeps at V_{gs} = -5V (deeply OFF-state) until catastrophic breakdown occurred, defined as the voltage at which drain current exceeds a threshold of 1 mA/mm. The V_{br} increases systematically with L_{gd}: Notably, the L_{gd} = 0.8 μm configuration exhibits a V_{br} of approximately 260V, which is higher than L_{gd} = 3 μm (135V) despite having a shorter drift region. This anomalous behavior may be attributed to specific edge termination effects or non-uniform electric field distribution in the ultra-short gate-drain spacing. However, the L_{gd} = 0.8 μm configuration shows sub-optimal overall performance with BFOM of 2.70 MW/cm² due to increased R_{on}, making it less practical than the L_{gd} = 3 μm structure (BFOM = 1.01 MW/cm²) for most applications. Therefore, the subsequent analysis focuses primarily on L_{gd} configurations from 3 μm to 30 μm. from approximately 135V (L_{gd} = 3 μm) to 380V (L_{gd} = 30 μm), as summarized in Table 2. This trend confirms that longer drift regions enhance voltage blocking capability by distributing the electric field over a larger area, thereby reducing peak electric field intensity at the gate edge. To quantitatively assess the trade-off between breakdown voltage and on-resistance, Baliga's Figure-of-Merit ($BFOM = V_{br}^2/R_{on}$) was calculated for each Lgd configuration. BFOM provides a single metric to evaluate power device performance, with higher values indicating better overall capability for power switching applications. Table 2 summarizes the key performance parameters and BFOM values for all simulated configurations.

Table 2. Performance parameters and Baliga's Figure-of-Merit (BFOM) for different L_{gd} configurations. R_{on} values are estimated from the linear region of I_{ds}-V_{ds} characteristics at low V_{ds} values.

L_{gd} (μm)	V_{br} (V)	$I_{ds,max}$ (mA/mm)	R_{on} (Ω·mm²)	BFOM (MW/cm²)
0.8	260	1.52	2.5	2.70
3	135	3.95	1.8	1.01
6	205	1.40	3.2	1.31
12	245	1.05	4.5	1.33
24	330	0.74	7.8	1.40
30	380	0.65	9.5	1.52

All configurations maintain extremely low leakage currents (< 0.0001 mA/mm) until approaching breakdown, where current rises exponentially due to impact ionization and avalanche breakdown. The avalanche breakdown mechanism is governed by the critical electric field (E_c) of GaN, which is approximately 3×10^6 V/cm. When the local electric field at the gate edge approaches or exceeds this critical value, charge carriers (electrons) gain sufficient kinetic energy from the electric field to cause impact ionization through collisions with the crystal lattice. This process generates electron-hole pairs, which in turn undergo further acceleration and collision, creating a multiplicative avalanche effect that leads to catastrophic breakdown. As shown in Table 3, the E_{max}/E_c ratio provides a quantitative measure of breakdown proximity: all configurations exhibit $E_{max}/E_c > 0.4$, indicating that these devices operate in moderate to high breakdown risk regions. Specifically, L_{gd} = 0.8 μm shows very high risk (E_{max}/E_c = 0.89), approaching the critical breakdown field. L_{gd} = 6 and 12 μm configurations exhibit high risk ($E_{max}/E_c \approx$ 0.62-0.65), while L_{gd} = 3, 24, and 30 μm show moderate risk ($E_{max}/E_c \approx$ 0.48-0.59). These elevated field values across all configurations below the critical threshold with substantial safety margin. A detailed regression analysis of the V_{br}-L_{gd} relationship reveals that the data follows a power law rather than a linear trend. For $L_{gd} \geq 3$ μm (excluding the anomalous 0.8 μm case), the breakdown voltage scales as $V_{br} \approx 89.4 \times L_{gd}^{0.419}$ (R^2 = 0.987), indicating a sub-linear dependence. This power law behavior is consistent with the complex interplay between drift region length, electric field redistribution, and surface charge effects. The exponent of 0.42 suggests that while longer L_{gd} improves V_{br}, the improvement rate diminishes due to increased series resistance and non-uniform field distribution at longer drift lengths.

Table 3. Maximum electric field (E_{max}) at the gate edge for different L_{gd} configurations. $E_c = 3 \times 10^6$ V/cm is the critical breakdown field for GaN. E_{max}/E_c ratio indicates proximity to breakdown condition.

L_{gd} (μm)	**E_{max} (V/cm)**	**E_{max}/E_c**
0.8	2.68×10^6	0.89
3	1.47×10^6	0.49
6	1.95×10^6	0.65
12	1.87×10^6	0.62
24	1.43×10^6	0.48
30	1.77×10^6	0.59

The results clearly demonstrate the R_{on}-V_{br} trade-off: the L_{gd} = 3 μm configuration with the highest current drive capability exhibits the lowest V_{br} (135V), while L_{gd} = 30 μm provides superior voltage blocking (380V) at the cost of reduced current density. This confirms that optimal L_{gd} selection must

balance conduction losses and voltage blocking requirements based on specific application voltage ratings: L_{gd} = 3-6 µm for < 200V, L_{gd} = 12-24 µm for 200-350V, and $L_{gd} \geq$ 30 µm for > 350V applications.

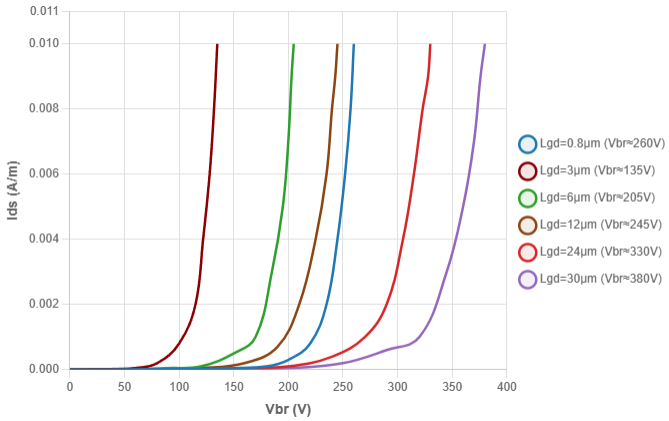

Figure 6. The breakdown voltage characteristics of multi-layer AlGaN HEMT for various L_{gd} distances.

Figure 7 shows the electric field distributions for different L_{gd} distances in the multi-layer AlGaN HEMT structure. In the colour maps of the simulation results, red-orange regions represent high electric field intensity (E_{max}), while blue-green regions represent low electric field intensity.

At short L_{gd} distances (0.8-3 µm), the electric field is seen to concentrate at the gate electrode edge, with E_{max} reaching critical levels. This confirms the mechanism stated in the paper: 'smaller L_{sd} or L_{gd} result in a higher electric field when voltage is applied, increasing the potential for avalanche breakdown. Charge carriers gain sufficient energy from the strong electric field, causing a sudden increase in current through collision ionisation. At long L_{gd} distances (24-30 µm), the electric field spreads over a wide drift region and E_{max} decreases significantly. This homogeneous distribution delays reaching GaN's critical electric field value (E_c = 1-3×10^6 V/cm), thereby increasing V_{br}. A direct correlation is observed with Figure 6: $V_{br} \approx$ 135V (high E_{max}) for L_{gd} = 3 µm, $V_{br} \approx$ 380V (low E_{max}) for L_{gd} = 30 µm.

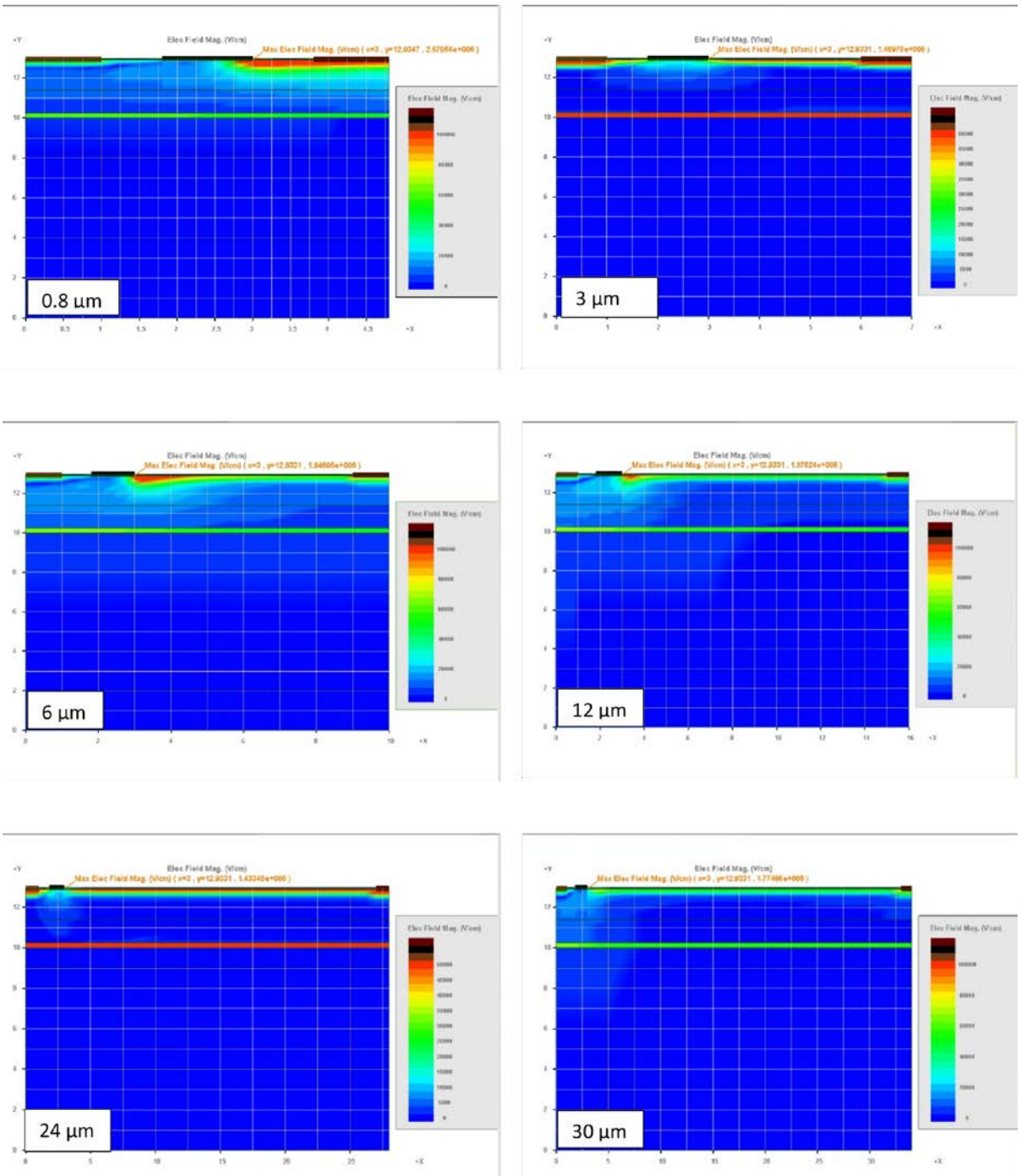

Figure 7. The electrical field characteristics of multi-layer AlGaN HEMT structure for various L_{gd} distances.

Electric field distributions explain the R_{on}-V_{br} trade-off at the physical level. Short L_{gd} (3-6 µm) provides low R_{on} and high current density ($I_{ds,max} \approx 3.95$ mA/mm), but due to high E_{max}, it gives low V_{br} (~135V) and low BFOM (V^2_{br}/R_{on}) values. Long L_{gd} (24-30 µm) offers high V_{br} (~380V) and improved reliability but reduces $I_{ds,max}$ to ≈ 0.65 mA/mm due to increased drift resistance. The optimal L_{gd} selection should be determined based on application requirements: $L_{gd} \geq 30$ µm for high-voltage applications

(>350V), L_{gd} = 12-24 μm for medium-power applications (200-350V), and L_{gd} = 3-6 μm for high-frequency applications (<200V) are recommended.

4. Conclusion

This study investigates the effects of gate-drain distance (L_{gd}) variation on electronic characteristics of a multi-layer graded $Al_xGa_{1-x}N$ HEMT structure (x = 0.05-0.30) on Si substrate using finite element method simulation through SimuApsys modeling software. The systematic analysis reveals the fundamental R_{on}-V_{br} trade-off mechanism governing power device performance. The simulation results demonstrate that L_{gd} significantly influences device characteristics through electric field distribution modulation. Short L_{gd} configurations achieve low on-resistance and high current density suitable for high-frequency applications, but exhibit concentrated electric field intensity resulting in lower breakdown voltages. Conversely, long L_{gd} configurations distribute the electric field over extended drift regions, enabling high breakdown voltages and improved reliability at the cost of increased resistance and reduced current capacity. The threshold voltage shows minor variation across all configurations, ranging from 1.16V to 1.28V, indicating that L_{gd} primarily affects drift region resistance rather than fundamental channel formation mechanisms in the compositionally graded AlGaN heterostructure. Electric field distribution analysis confirms that optimal design requires balancing conduction losses against voltage blocking requirements. Application-specific L_{gd} recommendations are established: short distances (3-6 μm) for low-voltage high-frequency applications (<200V), intermediate values (12-24 μm) for medium-power systems (200-350V), and extended distances (≥30 μm) for high-voltage power electronics (>350V). This simulation-based approach enables effective device optimization without expensive experimental fabrication, providing valuable design guidelines for graded AlGaN-based HEMT development and contributing to next-generation power electronics advancement. Future work should focus on experimental validation of the simulated graded AlGaN structure and investigation of advanced breakdown voltage enhancement techniques such as field plate optimization and high-k dielectric passivation layers.

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Conflict of Interest

The author(s) declare that there is no conflict of interest in this work. The work was written with the contributions of all authors.

Research and Publication Ethics

The author(s) declare that they have complied with the scientific, ethical and citation rules of the International Journal of Pure and Applied Sciences throughout all stages of the study.

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