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Research Article

An Efficient Layout Design of Fredkin Gate in Quantum-dot Cellular Automata (QCA)

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ABSTRACT

Quantum-dot Cellular Automata (QCA) has been considered one of the alternative technologies used in Nanoscale logic design and a promising replacement for conventional Complementary Metal Oxide Semiconductor (CMOS) due to express speed, ultra low power consumption, higher scale integration and higher switching frequency. In this paper, an efficient design of the Fredkin gate based on QCA logic gates: the QCA wire, 3-input majority gate and QCA inverter gate has been presented. Furthermore, compared with the previous design, the number of cells, covered area and latency time of the proposed design has reduced by 62.20%, 76.70%, and 25% respectively and also obviates coplanar wire-crossing. Functional correctness of the presented layout has proved by employing QCADesigner tools. The proposed circuit is suitable for constructing in low power consuming fault-tolerance system and can stimulate higher degree of integrated applications in QCA.

Keywords: *Quantum-dot Cellular Automata (QCA), QCA logic gates, Fredkin gate and QCADesigner*

Kuantum-noktası Hücresel Otomasyonda (KHO) Fredkin Geçitinin Etkili Bir Tasarım Deseni

ÖZET

Kuantum-noktası Hücresel Otomasyon (KHO), nano ölçekteki mantık dizaynlarında kullanılan ve süratli hız, ultra düşük güç tüketimi ve yüksek skalada entegrasyon ve yüksek anahtarlama frekansı yüzünden geleneksel Tümler Metal Oksit Yarıiletkenlerin yerini almada gelecek vadeden alternatif teknolojilerden biri olarak kabul edilmektedir. Bu çalışmada, KHO mantık geçitlerine; KHO kablosu, 3-girdi çoğunluk ve KHO dönüştürücü geçitlerine, dayanan Fredkin geçitinin etkili bir dizaynı sunulmuştur. Dahası, önceki dizaynla kıyaslandığında önerilen dizaynın hücrelerinin sayısı, kaplanan alan ve gecikme zamanı sırasıyla %62,20, %76,70 ve %25 azalmıştır ve aynı zamanda eş düzlemli kablo çaprazlamasını önlemiştir. Sunulan tasarımın işlevsel doğruluğu QCADesigner araçları kullanılarak kanıtlanmıştır. Önerilen devre düşük güç tüketen hata-toleranslı system oluşturmaya uygundur ve KHO'da yüksek dereceli entegrasyon uygulamalarını arttırabilir.

Anahtar Kelimeler: Kuantum-noktası Hücresel Otomasyon (KHO), *KHO mantık geçitleri, Fredkin geçiti ve QCADesigner*

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I. INTRODUCTION

REVERSIBLE logic circuits are widely used for its power minimization characteristics having the application such as low power CMOS design, optical computing, quantum computing, deoxy ribonucleic acid (DNA) computing, digital signal processing (DSP), optical information processing etc. [1-4]. R. Landauer showed that, the irreversible system dissipated energy due to information loss and the amount of energy dissipation for one bit of information kTln2 joules, where, k denoted the Boltzmann's constant and T the operating temperature [5]. Later Bennett showed that the energy dissipation can be avoidable if the system is built using reversible logic [6].

Now a day's, CMOS technology is approaching its physical limits and facing serious challenges by designing constantly increasing frequencies and downscaling of computational devices. However such technology has found many problems like high leakage current, high power consumption, high lithography cost, low density problem and limitation of speed in GHz range. One of the alternatives is known as Quantum-dot Cellular Automata (QCA) [7-8], which has recently been recognized as one of the top six emerging technologies with potential applications in future computing [9-10] for its high speed, high scale integration and low power consumption in various computational applications [8, 11, 25]. A recent study shows quantum dot cellular automata (QCA) are one of the promising new technologies capable to implement the reversible logic circuit [7, 11-16]. In Quantum computing we have found very few proposals on reversible logic gate design like Toffoli gate [17], Double Feynman gate [18], Fredkin gate [4] etc. In this paper, we proposed an efficient and robust structure of Fredkin gate which is more efficient in terms of cell counts, complexity and area in comparison to the previous design [4].

The rest of this paper is organized as follows. Section II is dedicated to brief review of QCA basic. Section III provides proposed QCA representation of Fredkin gate. In section IV simulations and results comparison part are discussed. Finally, we conclude this paper in section V.

II. QCA BASICS

The fundamental element of a QCA device is the squared QCA cell with two mobile electrons and two quantum dots [15, 19] presented in Figure 1(a). Depending on the electrons position QCA cell has two types of polarization, P = +1 or binary 1 and P = -1 or binary 0 [14, 20] as shown in figure 1(b).

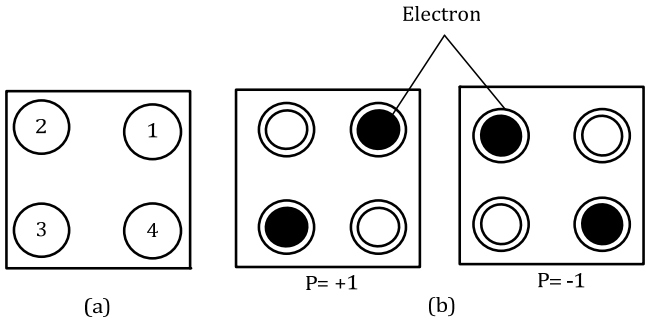

Figure 1. *(a) Basic structure of QCA cell with four dots, (b) different position of the electrons based on polarization*

The QCA-based design normally constructed using QCA wire, 3-input majority gate and inverter gate [15]. In QCA wire, the binary signal has propagated from input to output according to the electrostatic interactions between cells and each cells arranged in the same direction as the driving cell [16] shown in Figure 2.

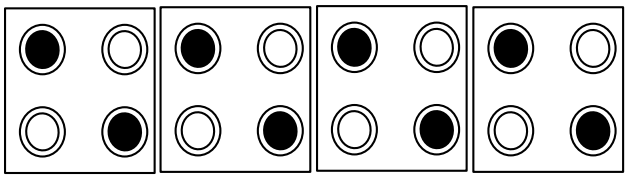

Figure 2. *QCA wires*

The 3-input majority voter gate consists of five cells; three input cells, a middle cell and one output cell [15, 19] shown in figure 3 (a). This 3-input majority gates can be programmed as 2-input AND gates or a 2-input OR gates, simply by fixing one of the three input to 0 or 1, as shown in figure 3 (b).

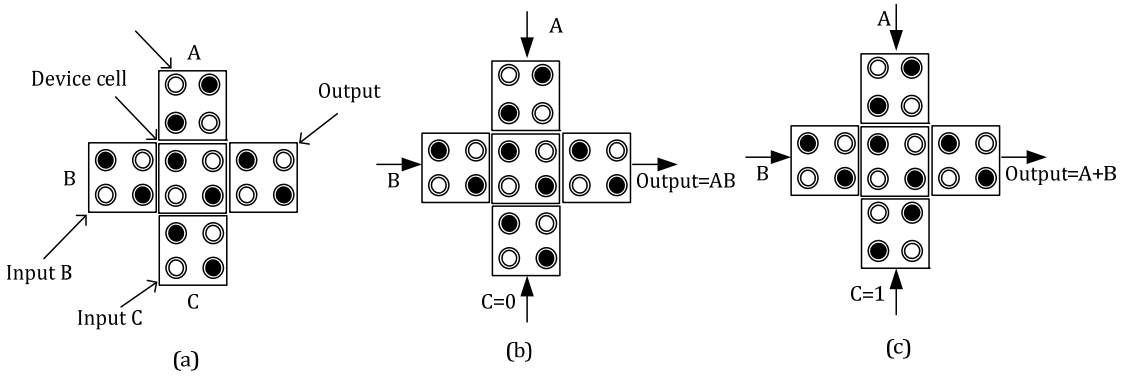

Figure 3. *The QCA majority gate (a), function as (b) the AND gate and (c) the OR gate*

The QCA inverter basically transfers the cell polarization to the opposite polarization. Different structures of QCA inverter are given in figure 4. In first structure figure 4 (a), the input signals polarization directly changed in the output cell, on middle one figure 4 (b) the input signal passed through two 45^0 cells and finally output get opposite polarization and in the last structure, the input polarization split into two polarizations and at the end, two wires join and make the reverse polarization.

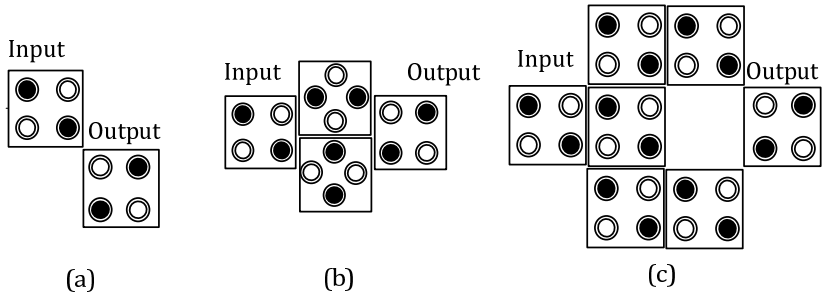

Figure 4. *Three different structures of inverter gates*

III. Proposed QCA Representation of Fredkin Gate

Fredkin gate is one of the basic 3-input and 3-output parity preserving reversible logic gate [23, 24] that is the parity of the outputs are the same of the inputs parity. Here, input vector is I_v *(A, B, C)* and the output vector is O_v *(P, Q, and R).* The three outputs are defined as follows; $P = A, Q = \bar{A}B + AC$ *and* $R = AB + \bar{A}C$. Table 1 represents the truth table of this gate. Equation 1 and 2 are the QCA representation of the two outputs and the schematic QCA representation Fredkin gate is shown in Figure 5.

$$Q = Maj(Maj(\bar{A}, B, 0), Maj(A, C, 0), 1) \quad (1)$$

$$R = Maj(Maj(A, B, 0), Maj(\bar{A}, C, 0), 1) \quad (2)$$

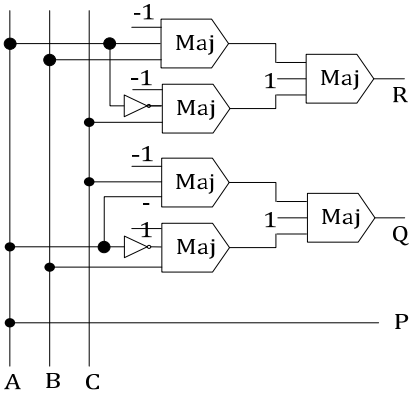

***Figure* 5.** *The schematic QCA representation Fredkin gate*

Table 1: *Truth table of Fredkin gate*

Input			Output		
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

IV. Simulation And Results Comparison

The proposed layout of Fredkin gate was simulated and verified using QCADesigner ver. 2.0.3, a common and powerful tool for QCA device design [22]. Bistable Approximation has been employed for simulating the proposed circuit with below parameters:

I. cell size = 18 nm,
II. number of samples = 50000,
III. convergence tolerance = 0.0000100,
IV. radius of effect = 65.000000 nm,
V. relative permittivity = 12.900000,
VI. clock high = 9.800000 e^{-022} J,
VII. clock low = 3.800000 e^{-023} J,
VIII. clock shift = 0,
IX. clock amplitude factor = 2.000000,
X. layer separation = 11.500000
XI. maximum iterations per sample = 100

Most of the above mentioned parameters are default values for bistable approximation [22]. The proposed circuit layout of Fredkin gate is shown in figure 6. Here, the input cells are A, B and C, and the output cells are P, Q and R. For OR operation a fixed cell polarization *P=1* and for AND operation fixed cell polarization *P= -1* is used.

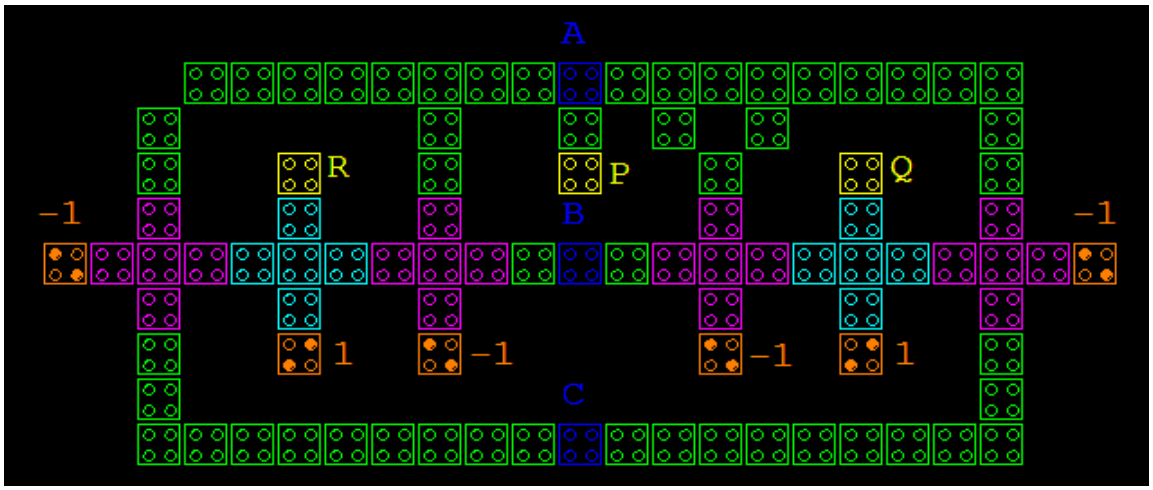

Figure 6. *Simulated circuit layout of Fredkin gate in QCA*

Figure 7 shows the input and output waveforms of the proposed layout of Fredkin gate, the red lines indicate the time delay with respect to the input signals. The overall is delay 0.75 clock cycles since the input signals clock pulse (CP) goes through three clock zones. From the output P, Q and R, the proposed gate operates properly on both falling and rising edges of the CP. Moreover, the proposed design used only 93 cells and the covered area 0.0874 μm^2. Compared to the previously designed Fredkin gate structure [4], the number of cells, covered area, and time delay of the proposed design are reduced by 62.20%, 76.70%, and 25%, respectively. Furthermore, coplanar wire-crossing is eliminated in our design while previously designed circuit [4] has five coplanar wire crossings. The performance comparison of the two Fredkin gate is illustrated in Table 2, showing that the present design has lower delay and simpler structure than previously designed gate [4].

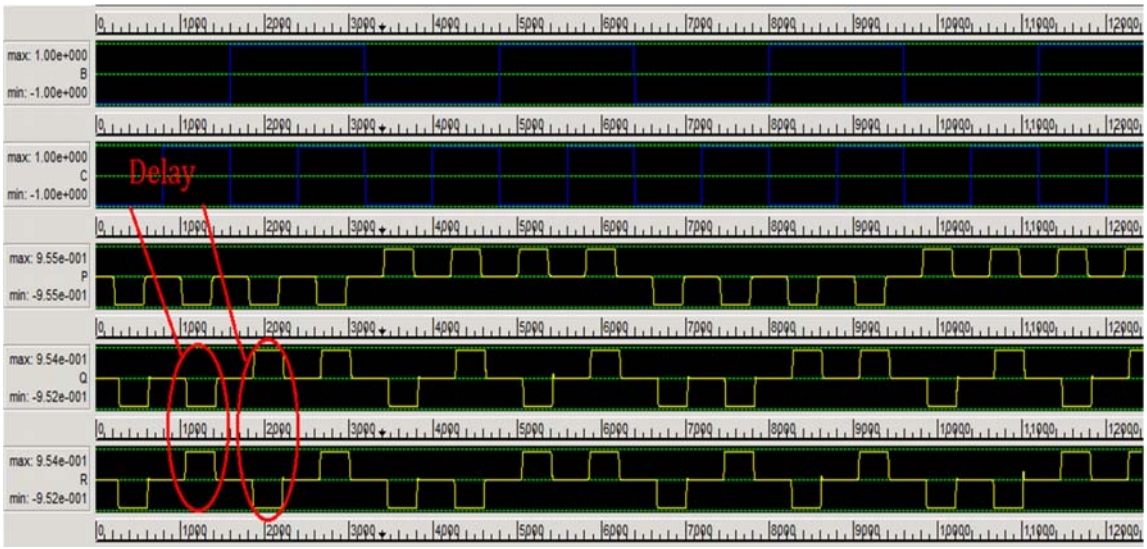

Figure 7. *Simulation results for the proposed layout of Fredkin gate*

Table 2. *Performance comparison of the two Fredkin gate*

Parameters	Fredkin gate[4]	Proposed Layout of Fredkin gate
Number of cells	246	93
Covered area (μm^2)	0.375	0.0874
Latency (clock cycle)	1	0.75
Number of wire-crossings	5	0

Figure 8 shows the overall improvement achieved in proposed layout over previous layout of Fredkin gate [4] in QCA.

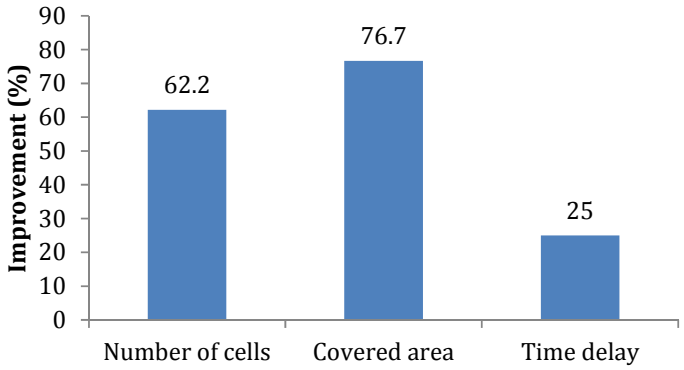

Figure 8. *Improvement achieved in proposed layout*

V. CONCLUSION

The proposed layout and previous Fredkin gate [4] designs have been compared in terms of Number of cells, covered area (size) and latency. This proposed design has been verified in QCADesigner. Simulation results reveal that the proposed layout of Fredkin gate has a simpler structure and also needs less cell counts, covered area and latency compared to the previous designs. Moreover, the proposed design reduced 62.20%, 76.70%, and 25% of the number of cells, covered area, and latency respectively compared with previous design. Finally, the proposed design avoids multi layer coplanar wire-crossing which would be very important for designing compact and fault tolerant ultra low power consuming nano device.

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