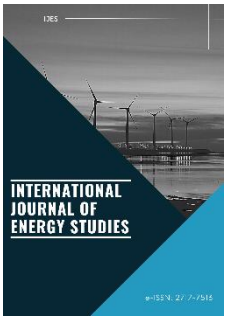
INTERNATIONAL JOURNAL OF ENERGY STUDIES

e-ISSN: 2717-7513 (ONLINE); homepage: https://dergipark.org.tr/en/pub/ijes



Research Article

Int J Energy Studies 2026; 11(1): 733-749

DOI: 10.58559/ijes.1894378

Received : 20 Feb 2026

Revised : 03 Mar 2026

Accepted : 09 Mar 2026

Super twisting sliding mode based voltage control of DC-DC SEPIC converters

Uğur Fesli[a*]

[a]*Gazi University, Faculty of Technology, Department of Energy Systems Engineering, Ankara, Turkey, ORCID: 0000-0003-3348-9140 (*Corresponding Author:ugurfesli@gazi.edu.tr)*

Highlights

- A super-twisting sliding mode controller is designed for SEPIC voltage regulation.
- Finite-time convergence is achieved with reduced chattering.
- Fixed-frequency PWM operation is maintained via duty-cycle control.
- Stable performance is validated in both buck and boost modes.
- Robust regulation is demonstrated under input, reference, and load disturbances.

You can cite this article as: Fesli U. Super twisting sliding mode based voltage control of DC-DC SEPIC converters. Int J Energy Studies 2026; 11(1): 733-749.

ABSTRACT

This paper proposes a Super-Twisting Sliding-Mode Control (STA-SMC) technique for voltage regulation of the SEPIC converter. The control error is defined as the error between the output and reference voltages. The error function is used as the sliding variable and the super twisting algorithm is integrated to reduce the chatterring. The duty cycle is generated by the integration of the sliding mode and super twisting algorithm. The effectiveness of the proposed method is validated experimentally on a SEPIC converter prototype. Steady-state results demonstrate that the controller successfully regulates the output voltage to its reference under buck and boost operating modes. Dynamic test results verify that the proposed controller is capable of output voltage regulation under variations in input voltage, reference voltage, and load resistance. In addition, the proposed STA-SMC method maintains stable voltage regulation despite operation mode transitions between buck and boost modes. It is also observed that the system variables don't include chattering.

Keywords: SEPIC converter, Sliding Mode Control, Super-Twisting Algorithm, Voltage control

1. INTRODUCTION

DC-DC converters are essential components of modern power electronics systems, widely used in critical applications such as smart grids, renewable energy systems, electric and hybrid vehicles, and industrial power supplies. These converters enable energy transfer by converting one DC voltage level to another. Various DC-DC converter topologies such as Buck, Boost, Buck-Boost, Zeta, Cuk, and SEPIC are commonly used. Each has advantages and disadvantages related to cost, application, control complexity, and efficiency [1]. Therefore, it is crucial to evaluate system requirements, operating conditions, and expected performance criteria to select the most suitable converter topology. Regardless of the chosen topology, the primary purpose of DC-DC converters is to maintain the output voltage or current at a specified reference level. The Single-Ended Primary Inductor Converter (SEPIC) stands out among these topologies with its ability to control the output voltage without reversing its polarity, regardless of whether the input voltage is greater or smaller than the output voltage.

SEPIC converters are particularly useful for applications operating with a wide input voltage range [2–4], and also, when galvanic isolation between input and output is not required, SEPIC systems reduce electromagnetic interference (EMI) and keep the input current constant. As a result, their use is very common in portable power supplies, solar energy systems, and battery chargers [5]. Controlling SEPIC converters is challenging due to their wide input voltage range, nonlinear dynamic characteristics, and varying load conditions [3]. The high dynamic dependence created by the coupling capacitor between the input and output inductor currents significantly limits the effectiveness of conventional control methods [6]. To overcome these limitations, there is a growing need for improved control systems that offer better performance, reliability, and faster dynamic response. Correct control methods are crucial for improving transient performance, making systems more efficient, and meeting the stringent quality standards of modern applications. Numerous control solutions have been proposed to improve the performance of SEPIC converters [7–10].

Conventional PID controllers are widely used, especially in solar energy applications [9]. However, these linear controllers have limited performance during rapid dynamic changes and are susceptible to parameter errors. SEPIC converters operating over a wide input voltage range encounter tuning difficulties due to the dependence of PID gains on operating points [10, 11]. To overcome these limitations, numerous development strategies have been proposed to improve the stability and robustness of PID-based controllers [8, 12, 13]. While these methods provide certain performance improvements, they often increase model complexity and computational

requirements. References [8] and [9] have examined Model Predictive Control (MPC) for SEPIC converters and demonstrated improved dynamic performance compared to conventional PID controllers. MPC-based methodologies exhibit numerous limitations, such as increased sensor requirements, significant computational costs, limited robustness against parameter fluctuations, and significant dependence on an accurate converter model [14]. Consequently, their usefulness may be limited. Due to its intrinsic robustness and resistance to parameter ambiguity, Sliding Mode Control (SMC) has proven to be an excellent alternative for managing DC-DC converters in this context [15]. The main advantage of SMC is its capacity to provide system stability regardless of model uncertainties, which is crucial, especially for nonlinear systems such as SEPIC converters [11, 16]. In the literature, various DC-DC converter designs, including buck, boost, buck-boost, Cuk, and SEPIC converters, have been effectively implemented with SMC. Traditional categories for contemporary SMC methodologies include observer-based SMC, integral SMC, terminal SMC, and classical SMC [17]. Traditional first-order SMC approaches, despite their robustness, produce high-frequency oscillations called jitter due to discontinuous control structures. This shortens the lifetime of power electronics components, increases switching losses, and exacerbates electromagnetic interference. [16], a PI controller was used to generate the current reference. This controller defined a simple sliding surface based on the inductor current error. A hysteresis band and a first-order control input were used to reduce the jitter effect. Despite its relative simplicity, significant vibrations resulting from the need for high sampling frequencies limit its use. To overcome these limitations, PWM-based SMC solutions have been designed. These methods facilitate operation at reduced switching frequencies by providing a discontinuous signal instead of a continuous control signal. PWM-based SMC techniques reduce hardware complexity while effectively regulating output voltage and inductor currents [18–20]. Constant frequency operation is achieved by converting the discontinuous control action into a constant duty cycle signal, which provides significant practical benefits [21]. However, the design of control rules constantly limits jitter suppression and dynamic response.Nevertheless, the architecture of their control rules results in persistent constraints regarding chattering suppression and dynamic responsiveness.

Recent focus has been directed towards minimizing chattering in sliding mode control while enhancing its efficacy. Nonetheless, attaining an optimal equilibrium among noise mitigation, rapid dynamic performance, control intricacy, and finite-time convergence continues to pose a formidable research challenge. A second-order SMC method that guarantees finite-time convergence in this context without necessitating the explicit derivative of the sliding variable is termed Super-Twisting Sliding Mode Control (ST-SMC) [22]. ST-SMC is an optimal control

solution for DC-DC converters, since it offers superior switching behavior compared to traditional SMC due to its stable control output [23, 24]. ST-SMC markedly diminishes chattering while preserving robustness against disturbances in contrast to conventional SMC.

In [25], the ST-SMC technique was utilized for SEPIC converters, wherein a twisting-based control rule was formulated and a sliding surface was established depending on output voltage error. This technique mitigated chattering due to the absence of direct inductor current management, although exhibited constrained dynamic performance during abrupt current variations. This underscores the importance of concurrently analyzing current and voltage dynamics in SEPIC converters [26]. Furthermore, the presentation of simulation results only limits the practical validation of the proposed method. On the other hand, while conventional linear sliding surfaces provide asymptotic convergence, Terminal Sliding Surfaces (TSS) achieve finite-time convergence and have been successfully implemented in various DC–DC converter topologies [27–29]. However, the combined application of TSS and ST-SMC has not been extensively investigated in the literature. The integration of these two approaches enables finite-time convergence while providing more effective chattering suppression.

In this study, a Super-Twisting Sliding Mode Voltage Controller is designed and analyzed for the regulation of the output voltage of a DC–DC SEPIC converter. First, the averaged mathematical model of the converter operating in continuous conduction mode is derived. Subsequently, a sliding surface based on the voltage error is defined and a super-twisting control law is developed. The performance of the proposed controller is evaluated through numerical simulations under input voltage and load variations and is compared with commonly used control methods reported in the literature.

2. MODELLING OF SEPIC CONVERTER

As illustrated in Fig. 1, the SEPIC converter consists of two inductors, L_1 and L_2, together with their internal resistances, R_1 and R_2, a coupling capacitor, C_1, an output capacitor, C_2, a MOSFET switch (S), a diode (D), and a load resistance (R_L) [23].

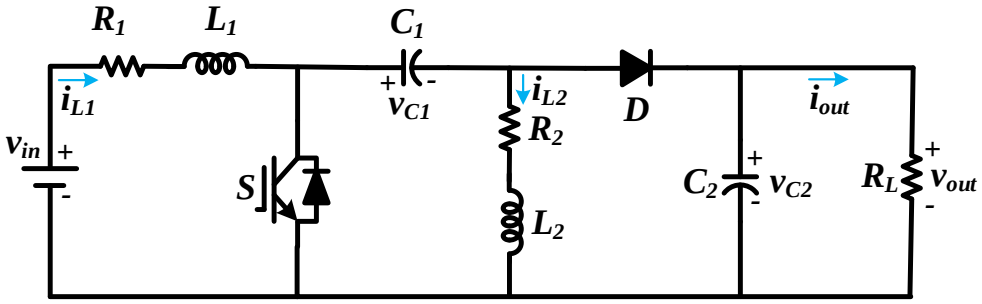


Figure 1. SEPIC converter

Depending on the switching state of the active element, the system operates in two distinct modes. The converter is assumed to operate in continuous conduction mode (CCM).

Switching State I (S = ON)

The equivalent circuit corresponding to this operating interval is illustrated in Fig. 2.

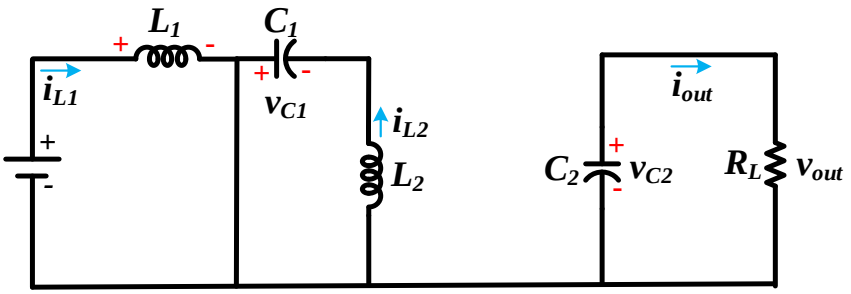


Figure 2. Equivalent circuit of the SEPIC converter during S = ON state

When the switch is in the ON state, the diode (*D*) is reverse-biased. In this condition, L_1 stores energy from the input source, while L_2 is energized through the coupling capacitor C_1. The load is supplied solely by the output capacitor C_2. The dynamic equations of the SEPIC converter corresponding to this operating mode are expressed as follows:

$$L_1 \frac{di_{L_1}}{dt} = V_{in} - R_1 i_{L_1} \quad (1)$$

$$L_2 \frac{di_{L_2}}{dt} = V_{C_1} - R_2 i_{L_2} \quad (2)$$

$$C_1 \frac{dv_{C_1}}{dt} = -i_{L_2} \quad (3)$$

$$C_2 \frac{dv_o}{dt} = -i_o = -\frac{v_o}{R_L} \quad (4)$$

Switching State II (S = OFF)

The equivalent circuit corresponding to this switching interval is depicted in Fig. 3.

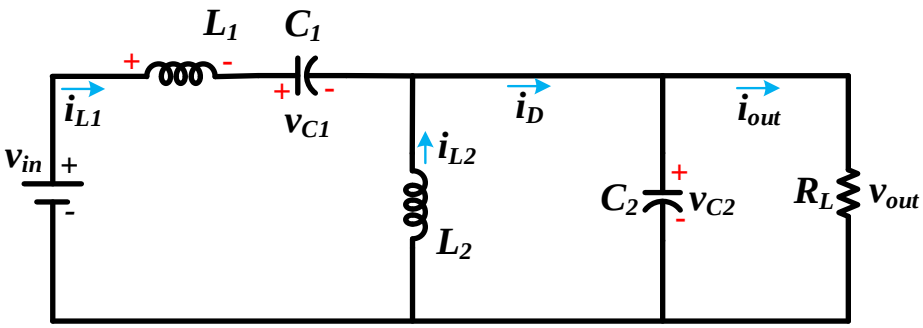


Figure 3. Equivalent circuit of the SEPIC converter during S = OFF state.

When the switch is OFF, the diode (*D*) becomes forward-biased. Under this condition, the energy stored in the inductors is transferred to the load and the output capacitor. The dynamic equations of the SEPIC converter corresponding to this operating mode are expressed as follows:

$$L_1 \frac{di_{L_1}}{dt} = V_{in} - v_o - v_{C_1} - R_1 i_{L_1} \tag{5}$$

$$L_2 \frac{di_{L_2}}{dt} = -v_o - R_2 i_{L_2} \tag{6}$$

$$C_1 \frac{dv_{C_1}}{dt} = i_{L_1} \tag{7}$$

$$C_2 \frac{dv_o}{dt} = i_{L_1} + i_{L_2} - \frac{v_o}{R_L} \tag{8}$$

By averaging the two operating modes over the switching period T_s using the duty ratio $u \in [0,1]$, the continuous-time averaged model can be obtained. The voltage gain of the SEPIC converter can be written as follows

$$\frac{v_{out}}{v_{in}} = \frac{i_{L1}}{i_{out}} = \frac{d}{1-d} \tag{9}$$

where *d* represents the duty ratio used to generate switching signal by applying a PWM generator. The use of duty ratio enables fixed-frequency operation and significantly mitigates the chattering phenomenon typically observed in classical sliding mode control. The average model of the

derivative of output capacitor voltage can be derived by combining Eqs. (4) and (8) over one switching period as follows

$$\frac{dv_o}{dt} = \frac{1}{C_2}\left[(1-d)\left(i_{L_1} + i_{L_2}\right) - d\frac{v_o}{R_L}\right] \tag{10}$$

The derivative of output voltage will be used in controller design. Based on this model formulation, the design procedure of the super-twisting sliding mode voltage controller is presented in the following section.

3. SUPER-TWISTING SLIDING MODE VOLTAGE CONTROLLER DESIGN

The objective of the controller is to regulate the output voltage of the SEPIC converter to its reference value init significantly reduces the chattering phenomenon that is typically observed in classical sliding mode control. To this end, a duty ratio based super-twisting sliding mode controller (ST-SMC) is employed, where the duty ratio *d* is generated as a continuous control signal. Now, the control error can be defined as follows

$$e = v_o - v_o{}^* \tag{11}$$

The error function is used as the sliding surface function (*s*) of ST-SMC as follows

$$s = e \tag{12}$$

The derivative of sliding surface function in (12) can be expressed by considering $v_o{}^*$ is constant and its time derivative is zero.

$$\dot{s} = \dot{v_o} = \frac{1}{C_2}\left[(1-d)\left(i_{L_1} + i_{L_2}\right) - d\frac{v_o}{R_L}\right] \tag{13}$$

It can be observed that the controller output (*d*) appears in $\dot{s}$. Therefore, the relative degree of the system is equal to one, making it suitable for the application of the super-twisting sliding mode control. Within this framework, a second-order sliding mode approach is adopted to drive both the sliding variable and its derivative to zero in finite time. The super-twisting algorithm provides significant advantages over classical sliding mode control, as it does not require the explicit

derivative of the sliding variable and ensures a continuous control signal. Accordingly, the reaching law is defined as

$$x = -a|s|^{\frac{1}{2}} sign(s) \tag{14}$$

$$y = -b \int sign(s)\, dt \tag{15}$$

Finally, the duty ratio can be obtained as a result of STA-SMC method as follows

$$d = x + y \tag{16}$$

where $a > 0$ and $b > 0$ are positive controller gains. The controller gains were selected considering the finite-time convergence conditions of the super-twisting algorithm. According to second-order sliding mode stability criteria, the gains must be chosen to ensure positivity and to guarantee that the equivalent perturbation term acting on the sliding dynamics remains bounded. In this study, the gain values were initially estimated based on the upper bound of system uncertainties and disturbance levels. Subsequently, fine-tuning was performed experimentally under nominal operating conditions (V_{in} =30V, V_o*=30V, R_L=20Ω), where the converter operates near the boundary between buck and boost modes. This operating point was intentionally selected since it represents the most critical region in terms of duty ratio variation and dynamic performance. The final gain values were determined to ensure fast transient response, minimal overshoot, and effective suppression of residual oscillations while maintaining control signal continuity. Under appropriate gain selection, both the sliding surface function *s* will converge to zero in finite time. In practical implementation, the duty ratio is constrained within the physical limits of the PWM block as $u \in [0,1]$ using a saturation function. This approach ensures that the control signal remains continuous, preserves fixed switching frequency operation, and significantly suppresses the high-frequency chattering effect observed in classical sliding mode control. The block diagram of the proposed control strategy is depicted in Fig. 4.

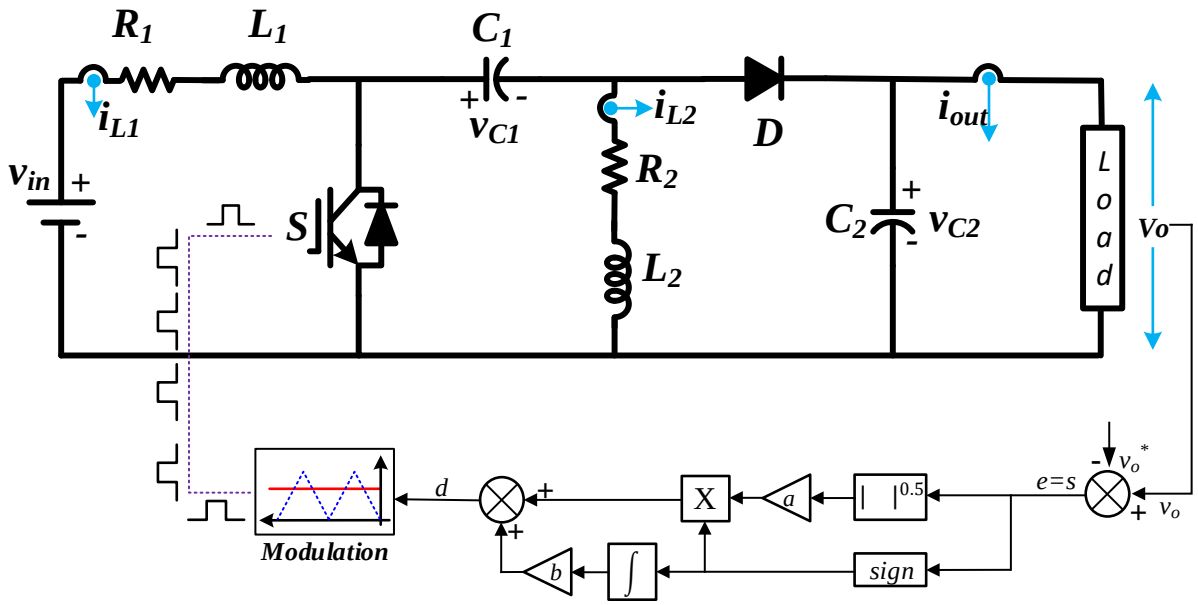


Figure 4. Block diagram of the proposed control strategy.

4. EXPERIMENTAL RESULTS

The experimental validation of the proposed super-twisting sliding mode controller (ST-SMC) was carried out on a laboratory-scale DC–DC SEPIC converter prototype. The system parameters are summarized in Table I. The controller was implemented in real time on a dSPACE MicroLabBox platform operating with fixed PWM switching frequency. The controller performance was evaluated under steady-state operation (boost and buck modes), input voltage variation, step change in the reference voltage and load disturbance conditions.

Table 1. System and control parameters

Parameter	Symbol	Value
Inductances	L_1 and L_2	730µH
Capacitances	C_1 and C_2	300µF, 1000µF
Load Resistance	R_{L1} *and* R_{L2}	20Ω, 10Ω
Converter switching frequency	f_s	20kHz
Sampling period	T_s	15µs
Controller gains	a and b	10^3, $1x10^{-5}$, 3

4.1. Steady State Response in Boost Mode

The steady-state performance of the proposed control strategy is experimentally investigated under boost operating condition. Fig. 5 illustrates the steady-state waveforms of v_{out}, v_{in}, i_{L1}, and i_o. In this test, the converter operates with V_{in} =20V, R=10Ω, and V_o*=30V conditions. It is observed that the output voltage is successfully regulated at its reference value of 30V without low-

frequency (less than switching frequency) oscillations. This confirms that the proposed controller maintains stable voltage regulation under boost mode operation. The inductor current waveform demonstrates the expected switching ripple associated with fixed-frequency PWM control. Similar to voltage result, no irregular low-frequency oscillations are observed in the current. This clearly shows that the super-twisting sliding mode controller effectively suppresses the chattering phenomenon commonly encountered in classical sliding mode control implementations.

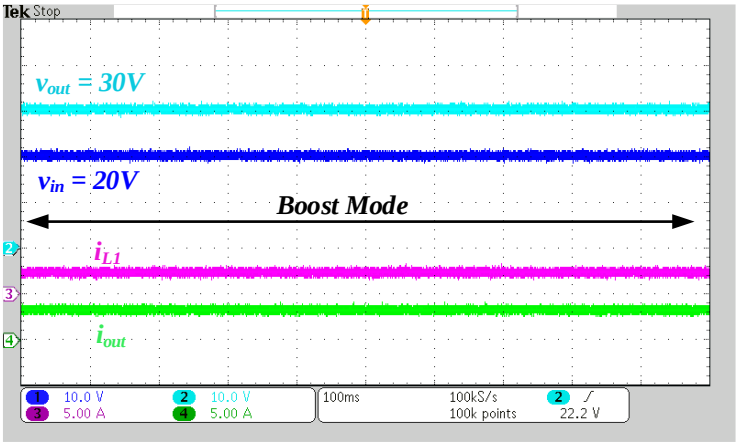


Figure 5. Experimental steady-state waveforms of v_{out}, v_{in}, i_{L1} and i_o, under boost operation.

4.2. Steady State Response in Buck Mode

To further assess the steady-state performance of the proposed control strategy, the SEPIC converter was operated in buck mode. The experimental conditions were set to V_{in} =40V, R=10Ω, and V_o*=30V. Fig. 6 shows the experimental waveforms of v_{out}, v_{in}, i_{L1}, and i_o during buck operation. The output voltage is accurately maintained at the reference 30V as shown in the figure. Compared to boost mode, the inductor current is lower due to the smaller voltage conversion ratio. The current waveform has a smooth shape and exhibits the switching ripple characteristic of constant-frequency PWM. Notably, no signs of discontinuous switching or oscillation-like movements in voltage or current were observed. This demonstrates that the proposed super-twisted slip mode controller provides consistent slip movement and accurate regulation in boost mode. Experimental results confirm the controller's ability to perform precise voltage tracking and achieve stable current performance in both boost and down modes. No parameter readjustment is required.

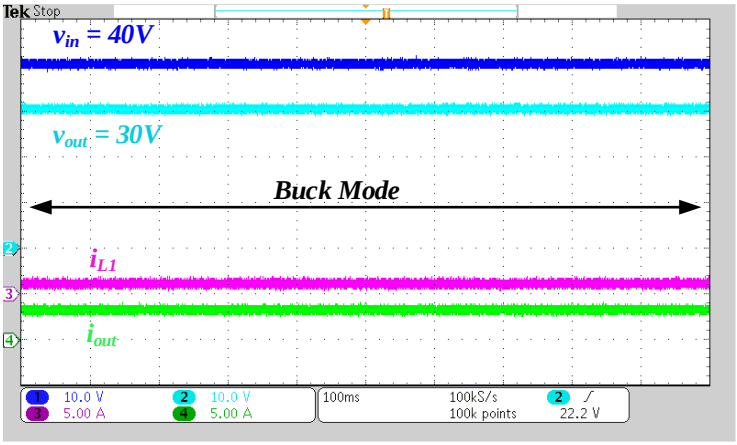


Figure 6. Experimental steady-state waveforms of v_{out}, v_{in}, i_{L1}, and i_o, under buck operation.

4.3. Step Change in The Input Voltage

To evaluate the robustness of the proposed control strategy against input voltage disturbances, a step change was applied to the input voltage while the load resistance is R=20Ω and the reference output voltage is Vo*=30V. As shown in Fig. 7, the input voltage is suddenly increased from 20V to 40V. Initially, the converter operates in boost mode.

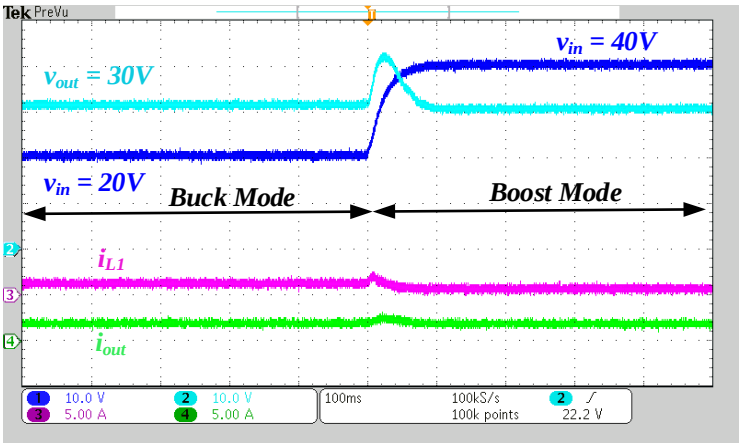


Figure 7. Experimental results under abrupt input voltage step from 20V to 40V.

After the step increase, the operating condition transitions toward buck mode due to the higher input voltage level. The abrupt input variation introduces a transient deviation in the output voltage. As a result of the abrupt change in the operating region and the associated energy redistribution within the passive components, an overshoot is occurred for a 100ms. However, the output voltage converges back to its reference value of 30V after the transient time. The inductor current i_{L1} adapts smoothly to the new steady-state condition. A temporary peak occurs during the

transition, but this peak is limited and quickly reaches equilibrium. The output current follows the dynamic behavior of the inductor current while maintaining stability and continuity. These experimental data demonstrate the robustness and wide operating range capability of the proposed control strategy, providing accurate voltage tracking and stable current behavior under sudden input voltage disturbances.

4.4. Step Change in Reference Voltage

To test the reference tracking capability of the proposed control strategy, a step change was applied to the output voltage reference while keeping the input voltage constant at Vin=30V and the load resistance R=20Ω. As shown in Fig. 8, the reference voltage is suddenly increased from 20V to 40V while the input voltage remains fixed. Under the initial condition (V_o*=20V), the converter operates in buck mode. After the reference is increased to 40V, the operating mode is changed from buck to boost. The output voltage is regulated to new reference after 34ms transition time. The inductor current is increased proportionally to meet the higher power demand and stabilizes rapidly at its new steady-state level. The experimental results demonstrate that the proposed super-twisting sliding mode controller provides smooth duty cycle adaptation, and stable dynamic performance during abrupt output voltage changes, confirming its robustness and chattering-free operation under large-signal disturbances.

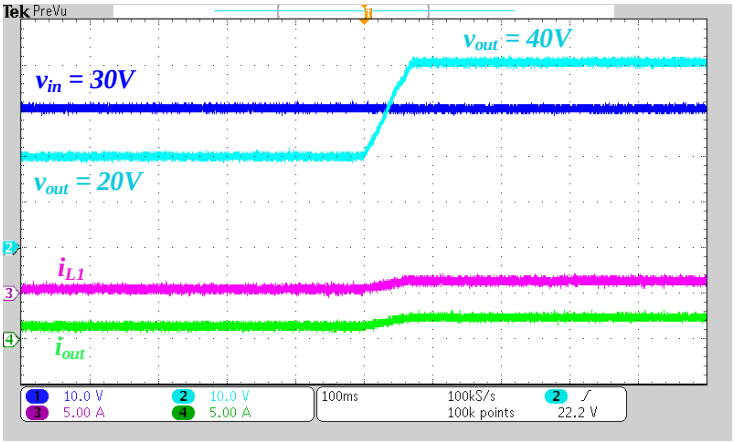


Figure 8. Experimental waveforms of v_{out}, v_{in}, i_{L1}, and i_o, under abrupt output voltage step (V_o*=20V→ 40V, $\mathbf{V_{in}}$ =30V, R=20Ω)

4.5. Step Change in Load Resistance

To evaluate the disturbance rejection capability of the proposed control strategy, the load resistance is changed from 20Ω to 10Ω while SEPIC converter is operating in boost mode under

V_{in} =20V and V_o*=30V conditison. As illustrated in Fig. 9, the output current is increased when the load resistance is decreased from 20Ω to 10Ω. This disturbance causes an undershoot in the output voltage. However, the deviation remains bounded and the output voltage quickly recovers to its reference value in 10ms. The inductor current is also increased accordingly to meet the higher load demand.

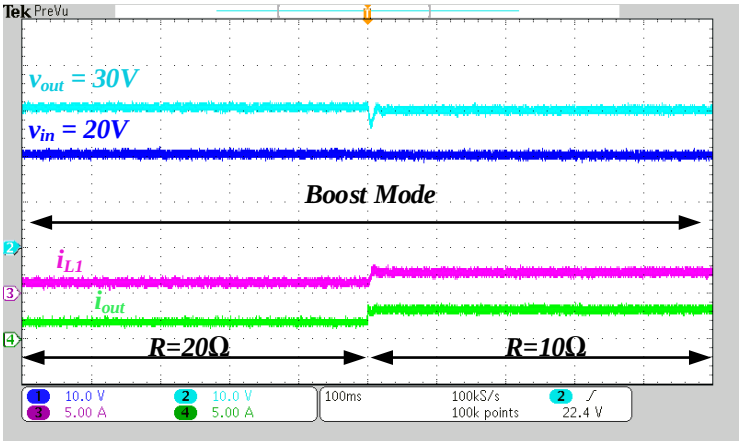


Figure 9. Experimental results under a load resistance variation in boost mode.

To further investigate the disturbance rejection capability of the proposed control strategy, a load step test was performed while the converter was operating in buck mode. In this case, the input voltage was fixed at V_{in} =40V and the reference output voltage was set to V_o*=30V. As shown in Fig. 10, the output current is increased from 1.5A to 3A due to the change in load resistance from 20Ω to 10Ω. This sudden increase in load produces a transient deviation in the output voltage due to the rapid change in power demand. The output voltage is regulated to its reference after a short transition time (less than 10ms). The inductor current is increased proportionally to supply the additional load current and settles smoothly at its new steady-state value.

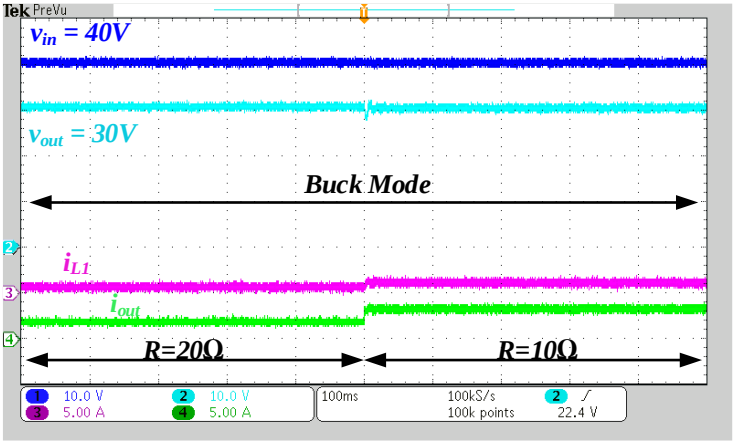


Figure 10. Experimental results under a load resistance variation in buck mode.

As a consequence of experimental results, the proposed super-twisting sliding mode controller provides strong rejection and maintains accurate voltage regulation and stable current dynamics in both buck and boost operation modes.

5. CONCLUSION

The voltage regulation of the SEPIC converter is achieved by the proposed STA-SMC method in this paper. The error function of the controller is selected as the voltage error and applied to the STA-SMC. The output of the controller (duty cycle) is applied to a pulse width modulation to generate the switching signal. The effectiveness of the proposed control technique is investigated through experimental studies. The steady state responses demonstrate that the proposed controller successfully regulates the output voltage to its reference under both buck and boost modes. In addition, the dynamic responses of the controller are tested under step changes in input voltage, reference voltage, and load resistance. The results show that the proposed STA-SMC method regulates the output voltage after the variations of the operating points of the converter. In addition, the operation mode of the converter is changed due to the variation in the input and reference voltages. The results verified that the proposed controller also provides the regulation against these large disturbances.

ACKNOWLEDGMENT

This work is financially supported by the Gazi University Scientific Research Projects Coordination Unit under Project Number FKB-2025-9943. I would like to express my gratitude to the Gazi University Scientific Research Projects Unit for their contributions.

DECLARATION OF ETHICAL STANDARDS

The author of the paper submitted declare that nothing which is necessary for achieving the paper requires ethical committee and/or legal-special permissions.

CONTRIBUTION OF THE AUTHORS

Uğur Fesli: Writing, Methodology, Data Curation, Review & Editing, the experiments and analyse the results.

CONFLICT OF INTEREST

There is no conflict of interest in this study.

REFERENCES

[1] Gorji SA, Sahebi HG, Ektesabi M, Rad AB. "Topologies and control schemes of bidirectional DC–DC power converters: An overview," IEEE Access, vol. 7, 2019, doi: 10.1109/ACCESS.2019.2937239.

[2] Chiang SJ, Shieh HJ, Chen MC. "Modeling and control of PV charger system with SEPIC converter," IEEE Transactions on Industrial Electronics, vol. 56, no. 11, 2009, doi: 10.1109/TIE.2008.2005144.

[3] Singh A, Gupta J, Singh B. "Bridgeless Modified High-Step-Up Gain SEPIC PFC Converter Based Charger for Light EVs Battery," IEEE Trans. Ind. Appl., vol. 59, no. 5, 2023, doi: 10.1109/TIA.2023.3282931.

[4] Forouzesh M, Siwakoti YP, Gorji SA, Blaabjerg F, Lehman B. "Step-Up DC-DC converters: A comprehensive review of voltage-boosting techniques, topologies, and applications," IEEE Trans. Power Electron., vol. 32, no. 12, 2017, doi: 10.1109/TPEL.2017.2652318.

[5] Gohil SN, Shah HA, Gauswami AR. "Design and Simulation of SEPIC Converter for EV Battery Charger," SSRG International Journal of Electrical and Electronics Engineering, vol. 11, no. 11, 2024, doi: 10.14445/23488379/IJEEE-V11I11P110.

[6] Cheng L et al. "Model Predictive Control for DC-DC Boost Converters with Reduced-Prediction Horizon and Constant Switching Frequency," IEEE Trans. Power Electron., vol. 33, no. 10, 2018, doi: 10.1109/TPEL.2017.2785255.

[7] Guler N, Biricik S, Bayhan S, Komurcugil H. "Model Predictive Control of DC-DC SEPIC Converters with Autotuning Weighting Factor," IEEE Transactions on Industrial Electronics, vol. 68, no. 10, 2021, doi: 10.1109/TIE.2020.3026301.

[8] Nguimfack-Ndongmo JDD, Kenné G, Kuate-Fochie R, Tchouani Njomo AF, Mbaka Nfah E. "Adaptive neuro-synergetic control technique for SEPIC converter in PV systems," International Journal of Dynamics and Control, 10(1), 203-216. 2022. doi: 10.1007/s40435-021-00808-1.

[9] Kumar S, Kumar R, Singh N. "Performance of closed loop SEPIC converter with DC-DC converter for solar energy system," in 2017 4th International Conference on Power, Control and Embedded Systems, ICPCES 2017, 2017. doi: 10.1109/ICPCES.2017.8117668.

[10] Journal I. "A Review on Control Methods of SEPIC Converters," INTERANTIONAL JOURNAL OF SCIENTIFIC RESEARCH IN ENGINEERING AND MANAGEMENT, vol. 07, no. 10, 2023, doi: 10.55041/ijsrem26064.

[11] Khather SI, Ibrahim MA. "Modeling and simulation of SEPIC controlled converter using PID controller," International Journal of Power Electronics and Drive Systems, vol. 11, no. 2, 2020, doi: 10.11591/ijpeds.v11.i2.pp833-843.

[12] Shagor MRK, Mahmud AJ, Nishat MM, Faisal F, Mithun MH, Khan MA. "Firefly Algorithm Based Optimized PID Controller for Stability Analysis of DC-DC SEPIC Converter," in 2021 IEEE 12th Annual Ubiquitous Computing, Electronics and Mobile Communication Conference, UEMCON 2021, 2021. doi: 10.1109/UEMCON53757.2021.9666555.

[13] Kirikci FM, Akyazi O, Kahveci H. "WSO-Optimized PID Controller Design for SEPIC Converter Voltage Stability," in 8th International Artificial Intelligence and Data Processing Symposium, IDAP 2024, 2024. doi: 10.1109/IDAP64064.2024.10710743.

[14] Wang B et al. "Event-Triggered Model Predictive Control for Power Converters," IEEE Transactions on Industrial Electronics, vol. 68, no. 1, 2021, doi: 10.1109/TIE.2019.2962489.

[15] Komurcugil H, Biricik S, Bayhan S, Zhang Z. "Sliding Mode Control: Overview of Its Applications in Power Converters," IEEE Industrial Electronics Magazine, vol. 15, no. 1, 2021, doi: 10.1109/MIE.2020.2986165.

[16] Komurcugil H, Biricik S, Guler N. "Indirect Sliding Mode Control for DC-DC SEPIC Converters," IEEE Trans. Industr. Inform., vol. 16, no. 6, 2020, doi: 10.1109/TII.2019.2960067.

[17] Wu L, Liu J, Vazquez S, Mazumder SK. "Sliding Mode Control in Power Converters and Drives: A Review," Mar. 01, 2022, Institute of Electrical and Electronics Engineers Inc. doi: 10.1109/JAS.2021.1004380.

[18] Rinaldi G, Menon PP, Ferrara A. "Design and Experimental Validation of an Embedded Sliding Mode Controller for Voltage Regulation With SEPIC Converters," IEEE Trans. Power Electron., vol. 39, no. 9, 2024, doi: 10.1109/TPEL.2024.3415164.

[19] Wondimu SA, Dagne DT, Fante KA. "Indirect sliding mode adaptive fractional order nonlinear observer based controller with fractional order single-ended primary inductor converter," International Journal of Electrical Power and Energy Systems, vol. 170, 2025, doi: 10.1016/j.ijepes.2025.110848.

[20] Martinez-Trevino BA, El Aroudi A, Cid-Pastor A, Garcia G, Martinez-Salamero L. "Synthesis of Constant Power Loads Using Switching Converters under Sliding-Mode Control," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 68, no. 1, 2021, doi: 10.1109/TCSI.2020.3031332.

[21] Liu J, Xiao F, Ma W, Fan X, Chen W. "PWM-based sliding mode controller for three-level full-bridge DC-DC converter that eliminates static output voltage error," Journal of Power Electronics, vol. 15, no. 2, 2015, doi: 10.6113/JPE.2015.15.2.378.

[22] Levant A. "Higher-order sliding modes, differentiation and output-feedback control," Int. J. Control, vol. 76, no. 9–10, 2003, doi: 10.1080/0020717031000099029.

[23] Bagheri F. "Cascaded Terminal Super Twisting Sliding Mode Control for DC-DC SEPIC Converters," IEEE Transactions on Industrial Electronics, 2025, doi: 10.1109/TIE.2025.3608035.

[24] Furqan M, Uddin W, Zeb K, Khalid M, Neamah HA. "Super twisting sliding mode control for high-efficiency and fast charging of electric vehicles using current-fed resonant converter: 400 V and 800 V validation," Results in Engineering, vol. 28, 2025, doi: 10.1016/j.rineng.2025.107945.

[25] Jin H. "Controlling the output voltage of the SEPIC converter using the second-order twisting sliding model controller," Multiscale and Multidisciplinary Modeling, Experiments and Design, vol. 7, no. 4, 2024, doi: 10.1007/s41939-024-00477-5.

[26] Abdel-Rahim O, Alghaythi ML, Alshammari MS, Osheba DSM. "Enhancing Photovoltaic Conversion Efficiency with Model Predictive Control-Based Sensor-Reduced Maximum Power Point Tracking in Modified SEPIC Converters," IEEE Access, vol. 11, 2023, doi: 10.1109/ACCESS.2023.3315150.

[27] Komurcugil H. "Adaptive terminal sliding-mode control strategy for DC-DC buck converters," ISA Trans., vol. 51, no. 6, 2012, doi: 10.1016/j.isatra.2012.07.005.

[28] Wang Z, Li S, Li Q. "Discrete-Time Fast Terminal Sliding Mode Control Design for DC-DC Buck Converters with Mismatched Disturbances," IEEE Trans. Industr. Inform., vol. 16, no. 2, 2020, doi: 10.1109/TII.2019.2937878.

[29] Long Y, Song E, Yao C. "Second-Order Discrete-Time Fast Terminal Sliding Mode Control Based on Exponential Reaching Law for Electronic Throttle," IEEE Trans. Veh. Technol., vol. 74, no. 9, 2025, doi: 10.1109/TVT.2025.3563080.