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Three-Level Boost Converter-Based Single-Phase Five-Level T-Type Inverter

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Graphical/Tabular Abstract (Grafik Özet)

This study presents a cascaded structure comprising a three-level boost converter and a five-level T-type inverter for renewable energy systems. This integration halves voltage stress, eliminates complex balancing algorithms, and ensures high-quality power delivery with low harmonics (1.22% THD), fully complying with IEEE 519 standards. / Bu çalışma, yenilenebilir enerji sistemleri için üç seviyeli yükseltici dönüştürücü ve beş seviyeli T-tipi invertör içeren kaskad bir yapı sunar. Bu entegrasyon, gerilim stresini yarıya indirir, karmaşık dengeleme algoritmalarını ortadan kaldırır ve IEEE 519 standartlarına uygun, düşük harmonikli (%1.22 THB) yüksek kaliteli güç aktarımı sağlar.

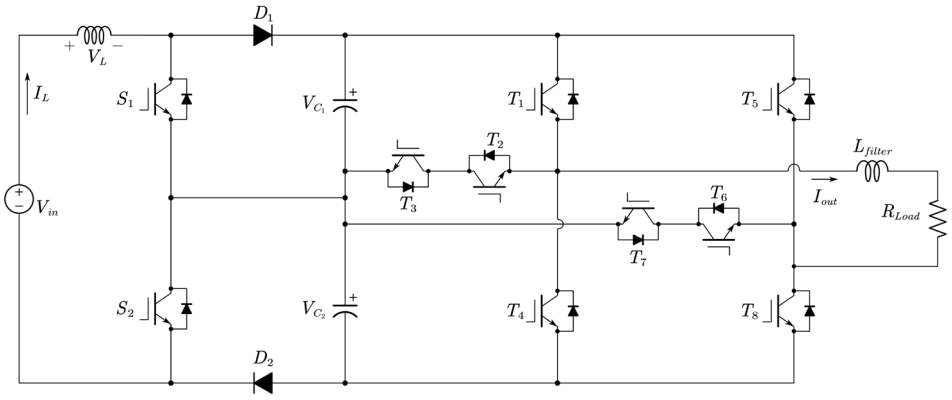

***Figure A**: Three-Level Boost Converter-Based Single-Phase Five-Level T-Type Inverter /**Şekil A:** Üç Seviyeli Yükseltici Dönüştürücü Tabanlı Tek Fazlı Beş Seviyeli T Tipi İnverter*

Highlights (Önemli noktalar)

- *A novel cascaded structure is proposed by integrating a three-level DC-DC boost converter and a five-level T-type inverter. / Üç seviyeli DC-DC yükseltici dönüştürücü ve beş seviyeli T-tipi invertör entegrasyonu ile yeni bir kaskad yapı önerilmiştir.*
- *The proposed topology reduces the voltage stress on power switches by 50%. / Önerilen topoloji ile güç anahtarları üzerindeki gerilim stresi %50 oranında azaltılmıştır.*
- *The system achieved a total harmonic distortion (THD) of 1.22% in steady-state and 1.01% under dynamic loading, complying with IEEE 519 standards. / Sistem, IEEE 519 standartlarına uygun olarak kararlı durumda %1.22, dinamik yüklemede ise %1.01 toplam harmonik bozulma (THB) değeri sağlamıştır.*

***Aim (Amaç):** To propose a cascaded power conversion structure composed of a three-level boost converter and a five-level T-type inverter for renewable energy systems. / Yenilenebilir enerji sistemleri için üç seviyeli yükseltici dönüştürücü ve beş seviyeli T-tipi invertörden oluşan kaskad bir güç dönüşüm yapısı önermektir.*

***Originality (Özgünlük):** The front-end boost converter actively balances the neutral-point voltage, entirely relieving the T-type inverter from complex balancing control algorithms. / Nötr nokta gerilim dengelemesinin doğrudan ön uçtaki yükseltici dönüştürücü tarafından yapılarak, invertördeki karmaşık kontrol algoritmalarının ortadan kaldırılmasıdır.*

***Results (Bulgular):** The system maintained a stable symmetric 350Vdc DC-link and generated a five-level output with a THD of 1.22% in steady-state and 1.01% under dynamic loading. / Sistem, kararlı simetrik 350Vdc DC-bara gerilimi sağlamış ve kararlı durumda %1.22, dinamik yüklemede ise %1.01 THB değerine sahip beş seviyeli çıkış üretmiştir.*

***Conclusion (Sonuç):** The proposed cascaded topology halves the switch voltage stress and achieves a rapid settling time, offering a robust and high-efficiency solution for renewable applications. / Önerilen kaskad topoloji, anahtar üzerindeki gerilim stresini yarıya indirir ve hızlı dinamik yanıt sağlayarak yenilenebilir uygulamalar için sağlam ve yüksek verimli bir çözüm sunar.*

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Abstract

This study proposes a cascaded power conversion structure composed of a three-level DC-DC boost converter and a single-phase five-level T-type inverter to address the high performance and power quality demands of renewable energy systems. The integrated topology is designed to overcome the limitations of conventional two-level architectures by combining high voltage gain with reduced voltage stress on power switches and minimized total harmonic distortion (THD). The paper presents a comprehensive mathematical model and a robust control strategy, utilizing decoupled loops for total DC-link voltage regulation and neutral-point balancing, alongside a synchronous reference frame current controller for the inverter stage. Simulation studies conducted in the MATLAB/Simulink environment validate the operational characteristics of the proposed system. The results demonstrate that the boost stage maintains a stable symmetric DC-link voltage of $350V_{dc}$ ($\mp 175V_{dc}$). Furthermore, the T-type inverter generates a five-level output waveform with a THD as low as 1.22% under steady-state conditions and 1.01% under dynamic loading, compliant with IEEE 519 standards. This confirms the system capability to reduce voltage stress on switches by 50% while ensuring high-quality power delivery.

Üç Seviyeli Yükseltici Dönüştürücü Tabanlı Tek Fazlı Beş Seviyeli T-Tipi İnverter

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Öz

Bu çalışma, yenilenebilir enerji sistemlerinin yüksek performans ve güç kalitesi taleplerini karşılamak için üç seviyeli bir DC-DC yükseltici dönüştürücü ve tek fazlı beş seviyeli T-tipi invertörden oluşan kademeli bir güç dönüştürme yapısı önermektedir. Entegre topoloji, yüksek voltaj kazancını güç anahtarlarındaki voltaj gerilimini azaltarak ve toplam harmonik bozulmayı (THB) en aza indirerek geleneksel iki seviyeli mimarilerin sınırlamalarının üstesinden gelmek üzere tasarlanmıştır. Makale, toplam DC bağlantı voltajı regülasyonu ve nötr nokta dengelemesi için ayrı döngüler kullanan kapsamlı bir matematiksel model ve sağlam bir kontrol stratejisi ile birlikte invertör aşaması için senkron referans çerçeve akım kontrolcüsünü sunmaktadır. MATLAB/Simulink ortamında yapılan simülasyon çalışmaları, önerilen sistemin çalışma özelliklerini doğrulamaktadır. Sonuçlar, yükseltici aşamanın $350V_{dc}$ ($\mp 175V_{dc}$) kararlı simetrik bir DC bağlantı voltajını koruduğunu göstermektedir. Ayrıca, T-tipi invertör, IEEE 519 standartlarına uygun olarak, kararlı durum koşullarında %1.22 ve dinamik yükleme altında %1.01 kadar düşük THD ile beş seviyeli bir çıkış dalga formu üretir. Bu, sistemin yüksek kaliteli güç iletimini sağlarken anahtarlar üzerindeki voltaj stresini %50 oranında azaltma yeteneğini doğrular.

1. INTRODUCTION (GİRİŞ)

The growing use of distributed renewable energy systems, electric vehicle (EV) charging infrastructure, and smart grid applications has increased the demand for high-efficiency, high-quality power conversion stages. Due to their ability to achieve reduced voltage stress, low harmonic distortion, and high efficiency, multilevel converter topologies have gained significant popularity, especially in medium- and high-power applications. Three-level boost converters offer enhanced voltage gain and reduced inductor current ripple in comparison with conventional two-level converters,

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rendering them ideal for photovoltaic (PV), energy storage, and power factor correction (PFC) systems [1]–[3]. Recent advancements have demonstrated that three-level boost converters can enhance dynamic performance further and reduce switching losses under various control schemes [3–5].

To overcome the inherent buck limitation of conventional voltage source inverters (VSI), recent researches have focused extensively on integrating boost capabilities into T-type inverter topologies. Do and Nguyen introduced the quasi-switched boost T-type inverter to achieve high voltage gain with a reduced passive component count [6], a concept further improved by Tran et al. to minimize voltage stress across the DC-link [7] and later enhanced to maximize the boost factor for wider operation ranges [8]. In the context of renewable energy applications, Osman et al. proposed a hybrid boost converter structure specifically for solar PV systems [9], while Nguyen et al. developed a single-stage boost-derived architecture featuring self-balanced capacitor voltages to eliminate complex balancing algorithms [10]. Beyond topological innovations, recent studies have also addressed system reliability through fault-tolerant control methods [11] and explored high-efficiency implementations using wide-bandgap materials [12]; however, these advanced configurations often entail trade-offs regarding increased control complexity, higher component counts, and electromagnetic interference challenges.

These advanced topologies are increasingly being adapted for specific applications such as grid-connected solar systems and electric mobility. Sharma et al. provided a comprehensive review detailing modulation techniques specifically tailored for grid-connected PV systems [13]. Similarly, in EV charging technology, Zinchenko et al. demonstrated the benefits of minimizing conversion stages to enhance power density in on-board chargers [14], while Guler et al. introduced a model predictive control (MPC) scheme for bidirectional chargers utilizing three-level F-type converters [15]. However, single-stage architectures frequently suffer from restricted voltage regulation ranges under wide load variations, and applying advanced control to complex structures imposes significant computational burdens and sensitivity to parameter mismatches.

Although topological integration offers potential, the effective operation of these systems relies heavily on robust control strategies. To address power quality, Jana and Biswas developed a generalized space vector pulse width modulation (SVPWM) scheme aimed at reducing switching frequency and harmonic distortion [16]. MPC has also emerged as a powerful alternative; Yang et al. successfully applied predictive current control to cascaded systems [17] and later proposed a constant switching frequency method to eliminate complex weighting factors [18]. Additionally, İnci investigated improved hysteresis current control to enhance dynamic performance [19], and Lakshmi and Kumar provided comparative reviews of T-type configurations [20]. Nevertheless, these methods exhibit certain limitations: hysteresis controls often lead to variable switching frequencies, complicating filter design, while advanced predictive and generalized modulation schemes typically remain sensitive to parameter mismatches. Moreover, existing studies often focus on topological structures rather than offering comprehensive solutions to the dynamic instability and steady-state error challenges inherent in cascade systems.

Considering the limitations of these power converters in literature, this study proposes a cascaded power conversion structure composed of a three-level boost converter and a single-phase five-level T-type inverter. While both 3-level boost converters and 5-level T-type inverters have been studied individually, the primary aim of this paper lies in their topological integration. The front-end three-level boost converter actively manages and balances the neutral-point voltage. This balancing entirely relieves the T-type inverter from complex balancing control algorithms and reduces the overall control burden. Consequently, the combined architecture offers a systemic advantage: it achieves high voltage gain and superior power quality (THD $\approx$ 1.22%) while providing dynamic stability and maintaining symmetrical voltage stress ($V_{out}/2$) across all semiconductor devices without requiring complex control schemes. This study aims to fill the gap in literature by providing comprehensive mathematical modeling, detailed dynamic simulation analysis, and robust decoupled controller design for this cascaded structure.

2. MATHEMATICAL MODEL OF THE THREE-LEVEL DC/DC BOOST CONVERTER (ÜÇ SEVİYELİ DC-DC YÜKSELTİCİ DÖNÜŞTÜRÜCÜNÜN MATEMATİKSEL MODELİ)

The three-level DC-DC boost converter is a high-gain step-up topology extensively utilized in high-voltage applications, such as PV-grid integration and EV powertrains, due to its ability to mitigate the voltage stress limitations of conventional boost converters. The typical three level DC-DC boost

converter is shown in Figure 1. By employing a structure with two active switches and a split-capacitor output DC link, this topology clamps the voltage across each semiconductor device to half of the total output voltage, thereby enabling the use of lower-voltage-rated transistors with better switching characteristics. This reduction in voltage stress minimizes switching losses and electromagnetic interference (EMI) and effectively doubles the frequency of the inductor current ripple, allowing for a significant reduction in the size of passive magnetic components while maintaining high power quality and improved power density.

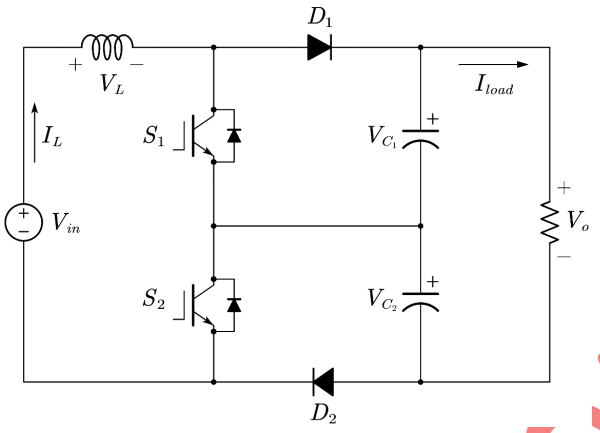


Figure 1. Three-level DC-DC boost converter (Üç seviyeli DC-DC yükseltici dönüştürücü)

The input-output voltage relationship depends on the duty cycle (D); the output voltage (V_{out}) is defined as:

$$V_{out} = \frac{V_{in}}{1-D} \tag{1}$$

A key characteristic of this topology is that the output capacitors share the voltage equally. Therefore, the voltage stress across each capacitor and switch is:

$$V_{C1} = V_{C2} = \frac{V_{out}}{2} = \frac{V_{in}}{2(1-D)} \tag{2}$$

This equation demonstrates that the switches are exposed to only half of the total output voltage, which is the primary advantage of this topology. The three-level DC-DC boost converter has four switching combinations:

When the S_1 and S_2 switches are turned-on, the inductor is connected to input and its path to capacitors is blocked by diodes. The inductor voltage (V_L) is expressed as:

$$V_L = V_{in} \tag{3}$$

Also, since the capacitors are in series and supply the load R across the total output voltage (V_{out}), the capacitor discharge currents (i_{C_1} and i_{C_2}) are physically equal and can be expressed as:

$$i_{C_1} = i_{C_2} = -\frac{V_{out}}{R} \tag{4}$$

When the S_1 switch is turned-on, and S_2 switch is turned-off, D_2 becomes forward-biased and the inductor transfers energy to the node across C_2. The inductor voltage and capacitor currents are defined as follows:

$$\begin{aligned} V_L &= V_{in} - V_{C_2} \\ i_{C_1} &= -\frac{V_{out}}{R} \\ i_{C_2} &= i_L - \frac{V_{out}}{R} \end{aligned} \tag{5}$$

When the S_1 switch is turned-off, and S_2 switch is turned-on, the inductor voltage and capacitor currents are defined as:

$$\begin{aligned} V_L &= V_{in} - V_{C_1} \\ i_{C1} &= i_L - \frac{V_{out}}{R} \\ i_{C2} &= -\frac{V_{out}}{R} \end{aligned} \tag{6}$$

When both the switches are turned-off, both diodes conduct and the inductor discharges into both series capacitors and the load. In this state, the inductor voltage (V_L) is expressed as:

$$V_L = V_{in} - (V_{C_1} + V_{C_2}) = V_{in} - V_{out} \tag{7}$$

Besides, the inductor current flows through both diodes into the series combination of C_1 and C_2, ensuring equal current distribution through the capacitors:

$$i_{C_1} = i_{C_2} = i_L - \frac{V_{out}}{R} \tag{8}$$

3. MATHEMATICAL MODEL OF THE SINGLE-PHASE T-TYPE INVERTER (TEK FAZLI T-TİPİ İNVERTER MATEMATİK MODELİ)

The single-phase five-level T-type inverter is an advanced multilevel topology that synthesizes a high-quality output voltage waveform by effectively combining the low conduction-loss characteristics of the conventional two-level inverter with the better performance of multilevel architectures.

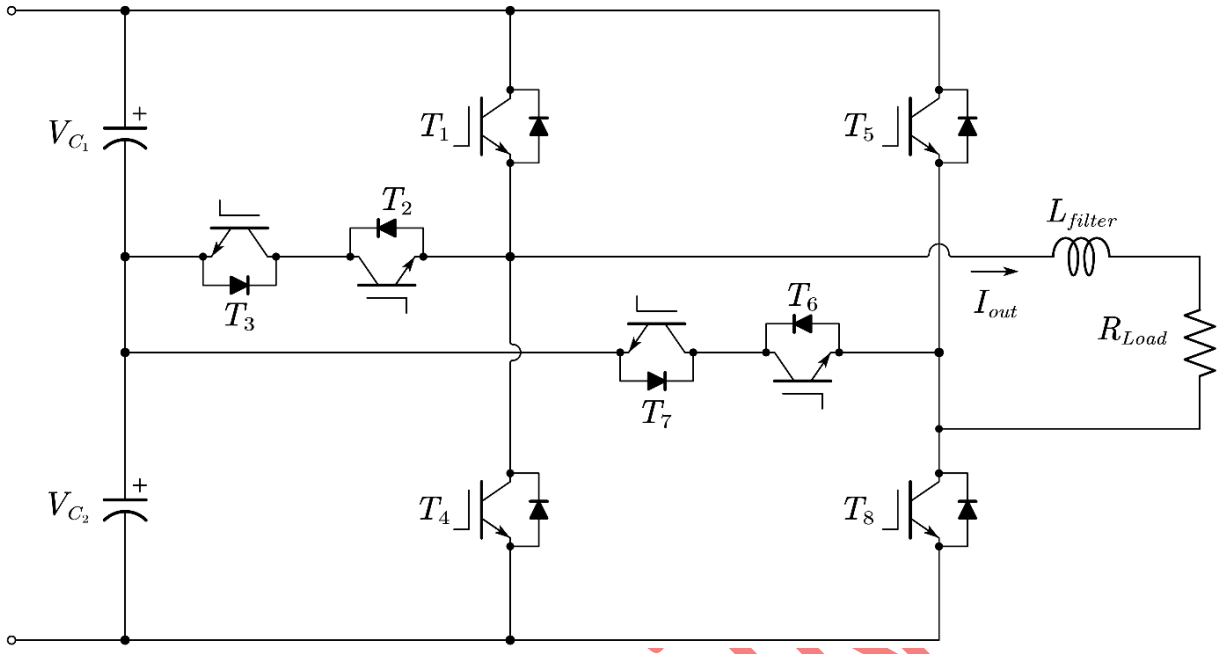


Figure 2. Five-level T-type inverter (Beş seviyeli T-tipi inverter)

As shown in Figure 2, the topology typically integrates a standard full-bridge or half-bridge configuration with bidirectional active switches connected to the DC-link midpoint, enabling the generation of five distinct voltage levels while eliminating the clamping diodes required by Neutral-Point-Clamped (NPC) converters. This configuration significantly mitigates voltage stress across the auxiliary switches to half the DC-bus voltage, allowing for the utilization of lower voltage rated power devices with faster switching speeds and reduced on-state resistance and conduction losses.

The input DC source is split by two DC-link capacitors, C_1 and C_2. Assuming ideal conditions and balanced capacitor voltages, the voltage across each capacitor is defined as:

$$V_{C_1} = V_{C_2} = \frac{V_{dc}}{2} \tag{9}$$

The inverter comprises two legs: Leg A (switches T_1–T_4) and Leg B (switches T_5–T_8). Each leg can generate five voltage levels with respect to the neutral point O: $(+V_{dc}, +V_{dc}/2, 0, -V_{dc}/2, -V_{dc})$. The switching states for Leg A (S_A) and Leg B (S_B) can be defined by the following switching functions:

For Leg A: (10)

$$S_A = \begin{cases} 1, & if\ T_1\ is\ on \\ 0, & if\ T_2 and\ T_3\ is\ on \\ -1, & if\ T_4\ is\ on \end{cases}$$

For Leg B:

$$S_B = \begin{cases} 1, & if\ T_5\ is\ on \\ 0, & if\ T_6 and\ T_7\ is\ on \\ -1, & if\ T_8\ is\ on \end{cases}$$

Consequently, the voltages relative to the neutral point O are expressed as:

$$V_{AO} = S_A \frac{V_{dc}}{2} \qquad V_{BO} = S_A \frac{V_{dc}}{2} \tag{11}$$

The output voltage of the inverter, applied to the load terminals, is the difference between the two leg voltages. It can be formulated as:

$$V_{out} = V_{AO} - V_{BO} = (S_A - S_B)\frac{V_{dc}}{2} \tag{12}$$

Based on the possible combinations of S_A and S_B, the inverter can produce five voltage levels at the output:

$$V_{out} \in \left\{+V_{dc}, +\frac{V_{dc}}{2}, 0, -\frac{V_{dc}}{2}, -V_{dc}\right\} \tag{13}$$

Table 1. Switching states and output voltages (Anahtarlama durumları ve çıkış gerilimleri)

State Level	Output Voltage (V_{out})	S_A	S_B	Conducting Switches
+2	$+V_{dc}$	1	-1	T_1, T_8
+1	$+\frac{V_{dc}}{2}$	1	0	T_1, T_6, T_7
0	0	0	0	T_2, T_3, T_6, T_7
-1	$-\frac{V_{dc}}{2}$	0	1	T_2, T_3, T_5
-2	$-V_{dc}$	-1	1	T_4, T_5

Table 1 summarizes the switching states, the corresponding output voltage levels, and the conducting devices for the proposed topology.

4. PROPOSED TOPOLOGY (ÖNERİLEN TOPOLOJİ)

The proposed power conversion system, illustrated in Figure 3, comprises a front-end three-level DC-DC boost converter and a single-phase five-level T-type inverter. The input stage interfaces the low-voltage DC source with the split DC-link capacitors. Unlike the conventional two-level boost converter, the three-level DC-DC boost converter consists of two active switches, two diodes, and a single input inductor. The key characteristics of this topology include reduced voltage stress across each active switch, which is limited to half of the total DC-bus voltage, this feature allows for the utilization of low-voltage rated transistors with better switching characteristics. Furthermore, the independent control of the upper and lower switches provides to balance the voltages across capacitors, which is critical for the proper operation of the subsequent multilevel inverter stage. The second stage performs the DC-AC conversion using a dual-leg T-type inverter configuration. Each leg consists of four power switches configured to generate voltage levels relative to the DC-link neutral point.

The integration of the boost converter with the T-type inverter offers several advantages for grid-connected or standalone applications. Primarily, the generated five-level output significantly reduces the THD compared to conventional H-bridge inverters, thereby minimizing the size and cost of the required output passive filters. Additionally, the system benefits from decoupled control capabilities where the boost stage actively assists in neutral-point voltage balancing, effectively decreasing the control burden on the inverter stage and ensuring stable operation under unbalanced load conditions.

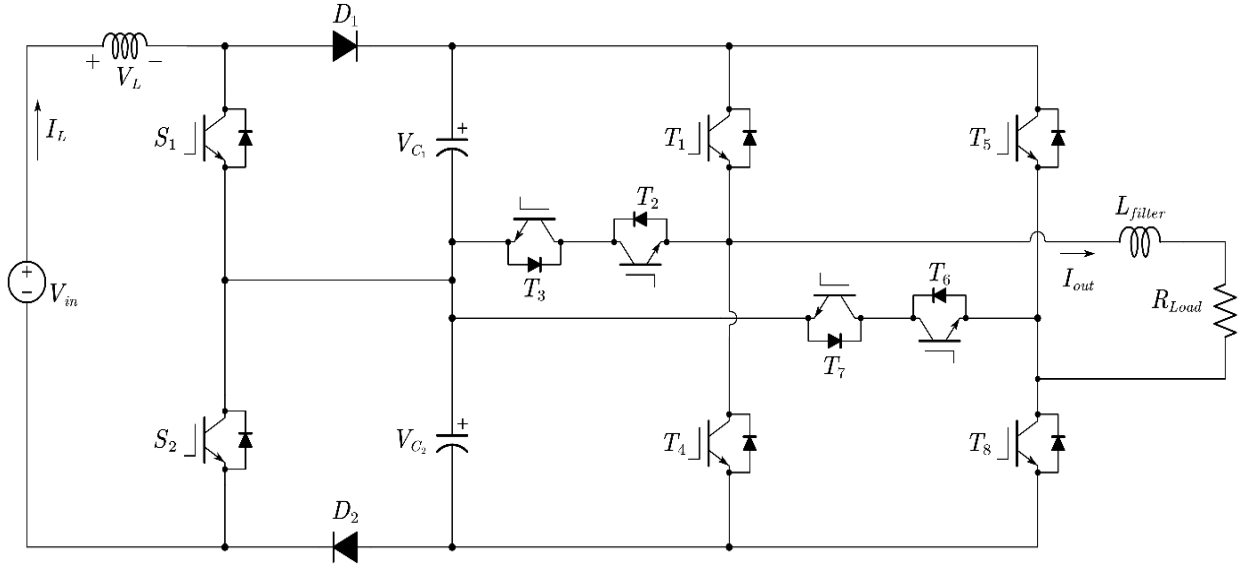


Figure 3. Proposed topology (Önerilen topoloji)

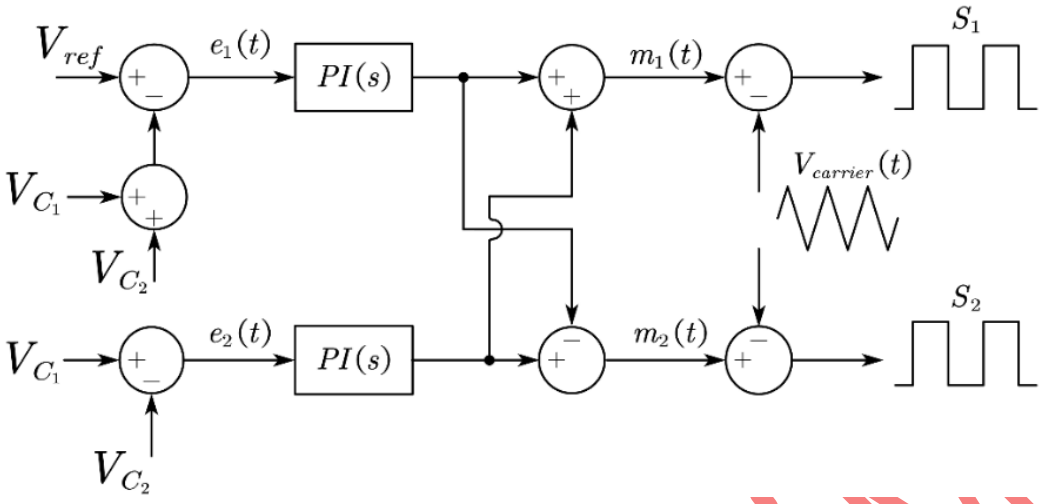


Figure 4. Three-level boost converter control diagram (Üç seviyeli yükseltici dönüştürücü control diyagramı)

4.1. DC-Link Voltage Control and Balancing Scheme (Dc Bara Gerilimi Kontrolü ve Dengeleme Şeması)

The control structure depicted in Figure 4 consists of two decoupled control loops: the total DC-link voltage controller to regulate the total energy, and the neutral point balancing controller to ensure voltage symmetry between capacitors C_1 and C_2. The control scheme processes two distinct error signals derived from the measured capacitor voltages (V_{C_1}, V_{C_2}) and the reference voltage (V_{ref}).

Total voltage error (e_1) represents the deviation of the total DC-bus voltage from the reference value:

$$e_1(t) = V_{REF} - \left(V_{C_1}(t) + V_{C_2}(t)\right) \tag{14}$$

Voltage balance error (e_{bal}) represents the voltage imbalance between the upper and lower capacitors. The reference for this difference is implicitly zero:

$$e_2(t) = V_{C_1}(t) - V_{C_2}(t) \tag{15}$$

Both error signals are processed by separate Proportional-Integral (PI) controllers to generate the necessary control actions. The output of the main voltage controller (u_{main}) is defined as:

$$u_{main}(t) = K_{p_1} e_1(t) + K_{i_1} \int_0^t e_1(\tau) d\tau \tag{16}$$

The output of the balancing controller ($u_{balance}$) is defined as:

$$u_{balance}(t) = K_{p_2} e_2(t) + K_{i_2} \int_0^t e_2(\tau) d\tau \tag{17}$$

where K_p and K_i denote the proportional and integral gain coefficients, respectively. To achieve simultaneous control of the output voltage and capacitor balancing, the balancing signal ($u_{balance}$) is imposed onto the main control signal (u_{main}). This results in two modified modulation signals (m_1 and m_2) for the upper and lower modulation references:

$$\begin{aligned} m_1(t) &= u_{main}(t) + u_{balance}(t) \\ m_2(t) &= u_{main}(t) - u_{balance}(t) \end{aligned} \tag{18}$$

By adding and subtracting the balancing term, the duty cycles are adjusted asymmetrically. When $V_{C_1} > V_{C_2}$, $u_{balance}$ becomes positive, increasing m_1 and decreasing m_2. This action modifies the power flow to discharge C_1 and charge C_2, thereby restoring balance ($V_{C_1} = V_{C_2}$).

Finally, the modulation signals are compared with a high-frequency carrier wave, $V_{carrier}(t)$ to generate the gating signals S_1 and S_2. The switching logic is expressed as:

$$\begin{aligned} S_1 &= \begin{cases} 1, & \left(m_1(t) - V_{carrier}(t)\right) \geq 0 \\ 0, & otherwise \end{cases} \\ S_2 &= \begin{cases} 1, & \left(m_2(t) - V_{carrier}(t)\right) \geq 0 \\ 0, & otherwise \end{cases} \end{aligned} \tag{19}$$

4.2. Current Control and PWM Generation (Akım Kontrolü ve PWM Üretimi)

The control system depicted in Figure 5 utilizes a synchronous reference frame current control strategy to regulate the output current of the T-type inverter. The control structure is divided into two main stages: the dq-frame current controller and the PWM switching signal generation.

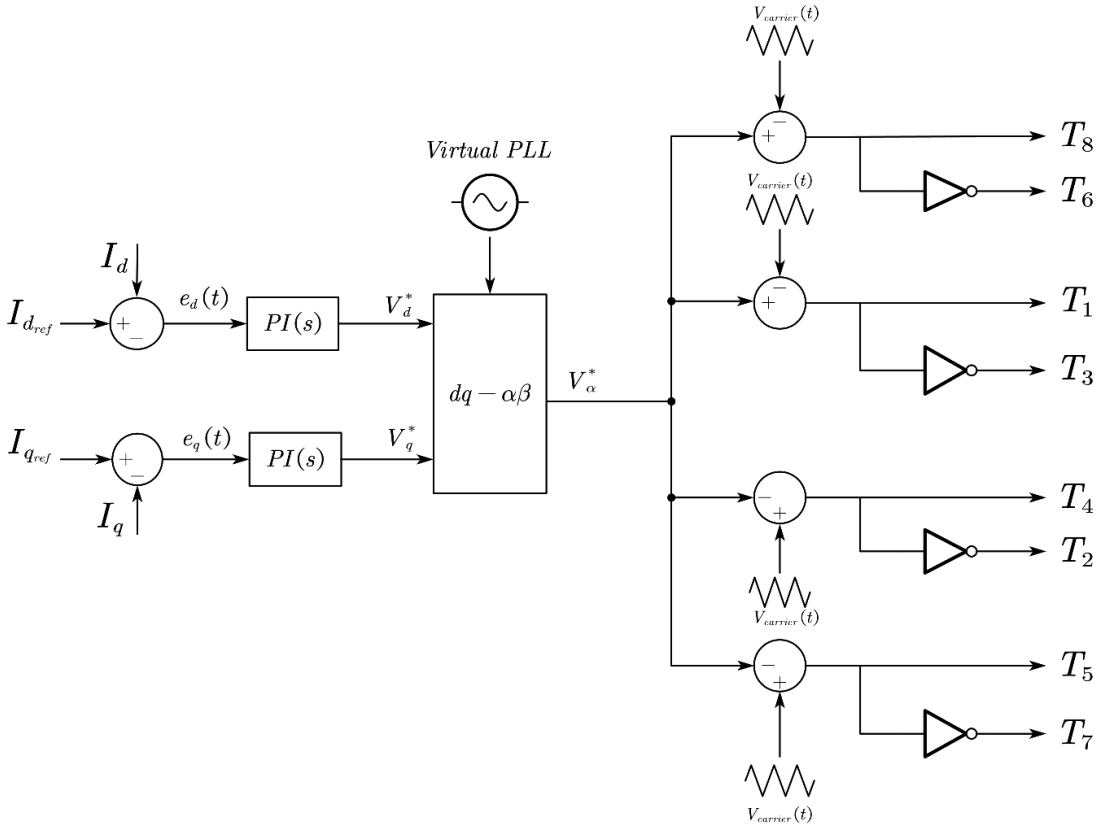


Figure 5. Single-phase five level T-type inverter control diagram (Tek fazlı beş seviyeli T-tipi inverter control diyagramı)

The control scheme operates in the rotating reference frame to achieve zero steady-state error for the AC current.

Since the proposed system operates with a single-phase output, the orthogonal current component (I_β) required for the synchronous reference frame (dq) transformation is not physically available. To address this, a virtual orthogonal signal generation method based on a quarter-cycle phase shift (T/4 delay) is employed. The measured load current serves as the α-axis component ($I_\alpha(t) = I_{load}(t)$), while the β-axis component is generated by delaying the measured current by 90 electrical degrees ($I_\beta(t) = I_{load}(t - T/4)$). This approach facilitates the transformation of the single-phase AC quantities into DC quantities (I_d, I_q) in the rotating reference frame, enabling zero steady-state error tracking via PI controllers. The error signals (e_d, e_q) are calculated by comparing the measured currents (I_d, I_q) with their respective reference values ($I_{d_{ref}}$, $I_{q_{ref}}$):

$$e_d(t) = I_{d_{ref}} - \imath_d(t)$$
$$e_q(t) = I_{q_{ref}} - \imath_q(t) \quad (20)$$

These error signals are processed by two independent Proportional-Integral (PI) controllers to generate the reference voltage components in the dq domain (v_d^*, v_q^*):

$$v_d^*(t) = K_{p_1} e_d(t) + K_{i_1} \int_0^t e_d(\tau) d\tau$$
$$v_q^*(t) = K_{p_2} e_q(t) + K_{i_2} \int_0^t e_q(\tau) d\tau \quad (21)$$

To generate the modulation signal for the physical switches, the reference voltages in the rotating frame must be transformed back to the stationary reference frame. This is achieved using the Inverse Park Transformation, utilizing the phase angle ωt:

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \begin{bmatrix} cos(\omega t) & -sin(\omega t) \\ sin(\omega t) & cos(\omega t) \end{bmatrix} \begin{bmatrix} v_d^* \\ v_q^* \end{bmatrix} \quad (22)$$

As shown in Figure 5, the α-axis component (v_α) which represents the primary modulation signal is used for the single-phase PWM generation.

Table 2. The logic states for the gate signals (Kapı sinyallerinin lojik durumu)

Switch Pair	Gate Signals
$T_6 = \overline{T_8}$	$T_8 = \begin{cases} 1, & if\ \alpha \geq v_{carr1} \\ 0, & otherwise \end{cases}$
$T_3 = \overline{T_1}$	$T_1 = \begin{cases} 1, & if\ \alpha \geq v_{carr2} \\ 0, & otherwise \end{cases}$
$T_2 = \overline{T_4}$	$T_4 = \begin{cases} 1, & if\ \alpha \geq v_{carr3} \\ 0, & otherwise \end{cases}$
$T_7 = \overline{T_5}$	$T_5 = \begin{cases} 1, & if\ \alpha \geq v_{carr4} \\ 0, & otherwise \end{cases}$

Table 3. Simulation parameters (Simülasyon parametreleri)

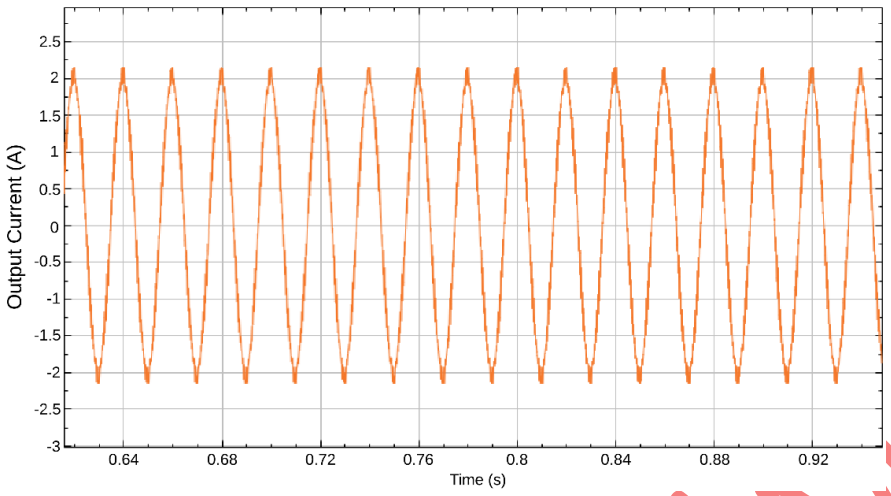
Parameter	Symbol	Value
Three level boost converter inductor	L_{in}	300uH
Input voltage	V_{in}	$100V_{dc}$
Output resistance	$Load$	100Ω
Output filter inductor	L_f	10mH
Output frequency	f	50Hz
T-type inverter switching frequency	f_{sw_1}	10kHz

5. SIMULATION STUDIES (SİMÜLASYON ÇALIŞMALARI)

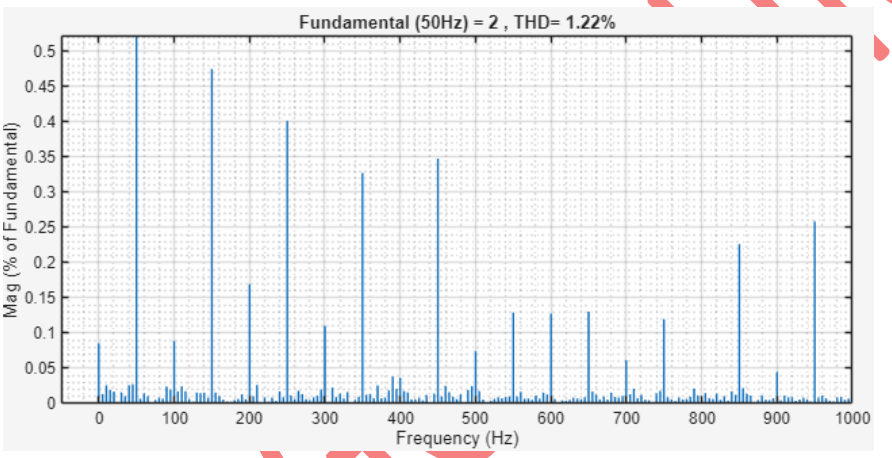
To verify the theoretical framework and operational characteristics of the proposed system, simulation studies are conducted using MATLAB/Simulink. The investigation focuses on the integration of a three-level boost converter with a single-phase five-level T-type inverter. The obtained results indicate that the proposed configuration operates successfully under steady-state conditions. The subsequent analysis of the waveforms demonstrates the system's superior performance in terms of DC-link voltage balancing and output waveform quality, thereby proving the robustness of the proposed control and modulation strategy. The simulation parameters are given in Table 3.

Figure 6 (a) presents the output current waveform obtained from the proposed system. The current exhibits a highly sinusoidal profile with a peak amplitude of approximately 2 A. By using the five-level T-type inverter topology, it is possible to obtain clean current waveform with a reduced filter size. The smooth sinusoidal nature of the current, despite the stepped nature of the voltage waveform, indicates effective filtering and THD. This demonstrates the inverter's capability to supply high-quality power to the load, making it suitable for grid-connected applications or sensitive AC motor drives where current quality is important.

Figure 6 (b) presents the harmonic spectrum and the THD value of the proposed system under steady-state conditions. The resulting THD value is measured at 1.22 %. This significantly low value explicitly verifies the effectiveness of the current controller and the capability of the T-type inverter to generate a high-level output voltage. Notably, the low amplitude of the harmonics surrounding the switching frequency multiples demonstrates both the success of the five-level modulation strategy and the appropriate sizing of the output filter. A THD value of 1.22 % confirms that the inverter meets the stringent power quality requirements, such as those imposed by the IEEE 519 standard for grid-connected systems, making it an ideal power supply for sensitive loads or motor drives where current quality is crucial.



(a)



(b)

Figure 6. (a) Output current (load current) (b) current THD value ((a) Çıkış akımı (yük akımı) (b) akım THD değeri)

The output voltage waveform of the single-phase T-type inverter is depicted in Figure 7. The inverter successfully generates a five-level output voltage ($+V_{dc}$, $+V_{dc}/2$, 0, $-V_{dc}/2$, $-V_{dc}$), corresponding to voltage steps of roughly ± 175 V and ± 350 V. This five-level waveform significantly reduces the voltage stress on the power switches compared to conventional two-level inverters. Furthermore, the clear distinction between voltage levels indicates proper switching transitions and effective dead-time implementation, which minimizes voltage spikes and EMI.

The stability of the neutral point potential is a critical parameter for the reliability of multilevel inverter topologies. Figure 8 illustrates the voltages across the DC-link capacitors, C_1 and C_2 (V_{C_1} and V_{C_2}). As observed, the proposed three-level boost converter effectively regulates the total DC-bus voltage while maintaining a balanced distribution between the upper and lower capacitors. Both V_{C_1} and V_{C_2} are maintained at approximately 175 V, resulting in a total DC-bus voltage of 350 V.

Figure 9 demonstrates the dynamic performance of the proposed current control strategy by illustrating the step response of the output current in the dq axis. The dq axis current reference ($i_{d_{ref}}$) is set to zero (0) to maintain unity power factor, and the resulting i_d current tracks its reference perfectly with minimal oscillation and a near-zero steady-state error. Concurrently, the q-axis current reference ($i_{q_{ref}}$) undergoes a step change, increasing from 2A to 3A. The i_q current responds rapidly and precisely to this step change, settling at the new reference value within approximately 0.1 s. This fast and stable response successfully validates the ability of the designed PI-based controller to achieve highly dynamic current regulation and zero steady-state error, proving the system effectiveness against rapid changes in power reference.

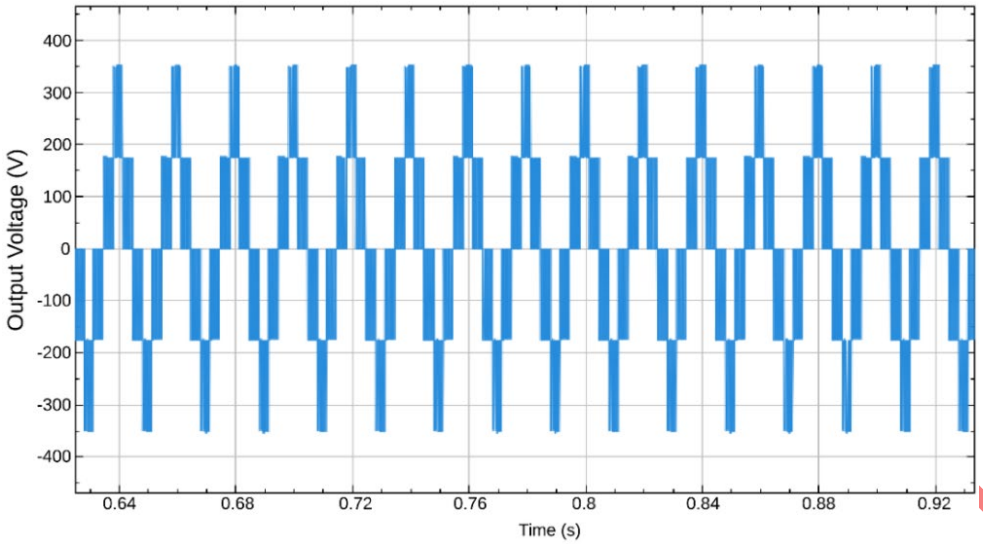


Figure 7. Output voltage waveform (Çıkış gerilim formu)

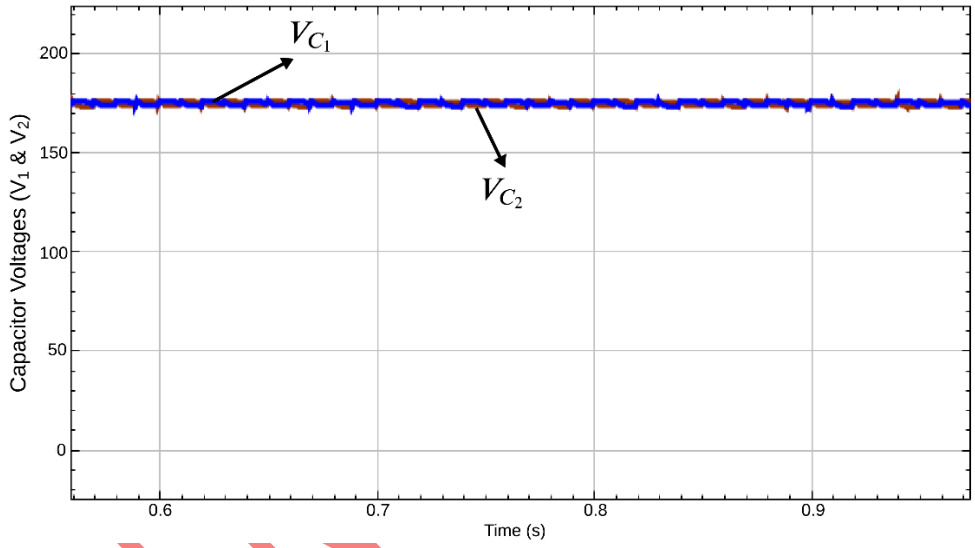


Figure 8. Capacitor voltage balance (Kondansatör gerilim dengesi)

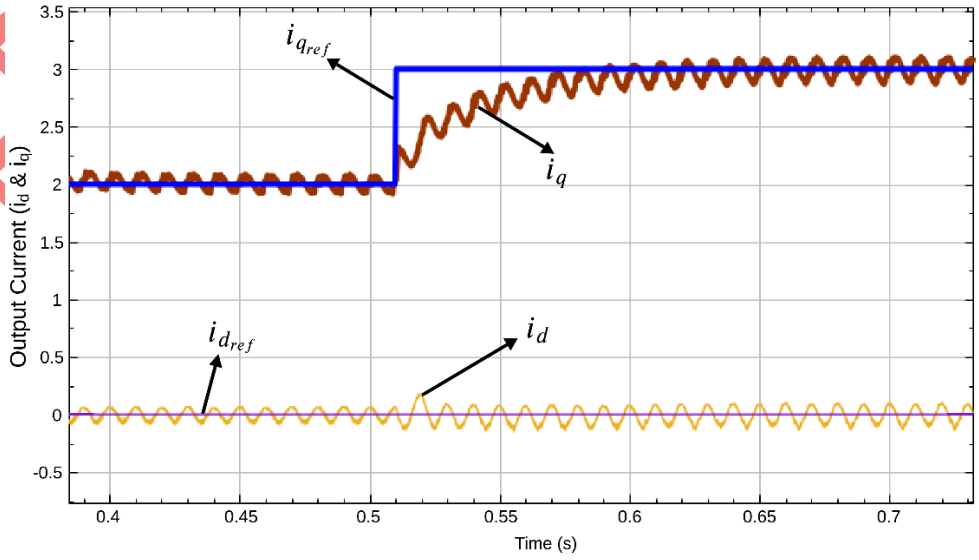
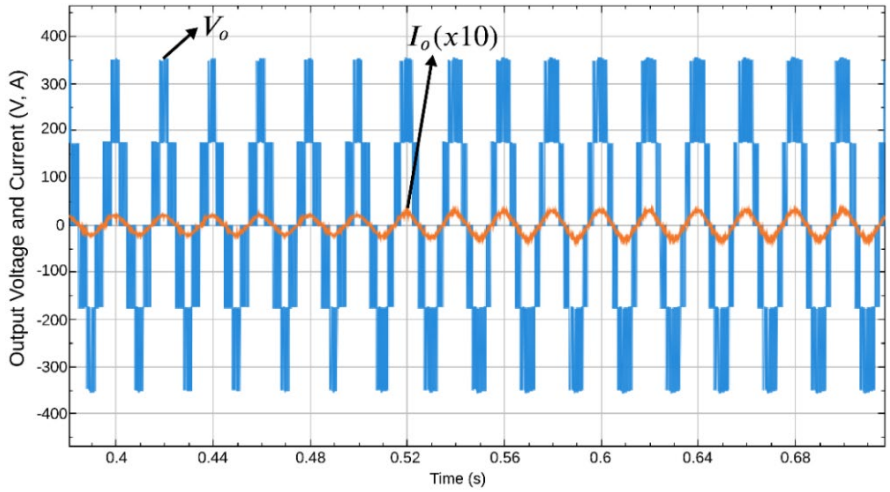
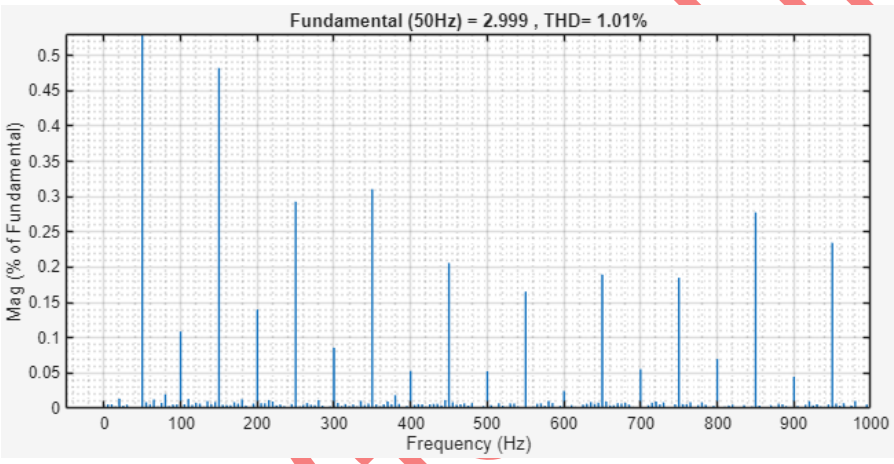


Figure 9. Step response of the output current in a dq axis reference frame (dq referans eksen çerçevesinde çıkış akımının adım cevabı)



(a)



(b)

Figure 10. (a) Step response of the output current and output voltage waveforms (b) current THD value after a step response ((a) Çıkış akımı ve çıkış gerilim dalga formlarının adım cevabı (b) adım cevabı sonrası akım THD değeri)

As observed in Figure 9, the step response takes approximately 5 grid cycles ($0.1\ s$) to completely settle to the new reference value. To prevent severe transient voltage fluctuations on the cascaded DC-link capacitors during rapid load changes, the bandwidth of the PI controllers is restricted deliberately. By limiting the current tracking speed, the system ensures that the neutral-point balancing and the total DC-bus voltage remain stable, prioritizing overall system reliability and safety over dynamic tracking.

Figure 10 (a) presents the step response waveforms for both the five-level output voltage (V_o) and the sinusoidal output current (I_o) of the proposed topology under increased load. Despite the current waveform (I_o, scaled by x10) experiencing a step increase, the output voltage (V_o) maintains its characteristic structure without exhibiting any significant distortion or transient ripple. This observation indicates the stability of the DC bus voltage and the effectiveness of the boost converter control. The T-type inverter's ability to sustain a clean and distinct five-level staircase structure, with voltage levels at $\mp V_{dc}$ and $\mp V_{dc}/2$, even under increased current demand, confirms both the benefit of reduced switching stress inherent to the topology and the control capability to generate a high-quality waveform during dynamic operation.

Figure 10 (b) displays the harmonic spectrum and the THD value of the output current immediately following a dynamic step change in load. After the current reference increased from 2A to 3A, the THD value is determined to be 1.01 %. This result indicates a level of harmonic distortion that is even lower than the steady-state value (1.22 %), confirming the superior dynamic stability and high current quality of the proposed control strategy.

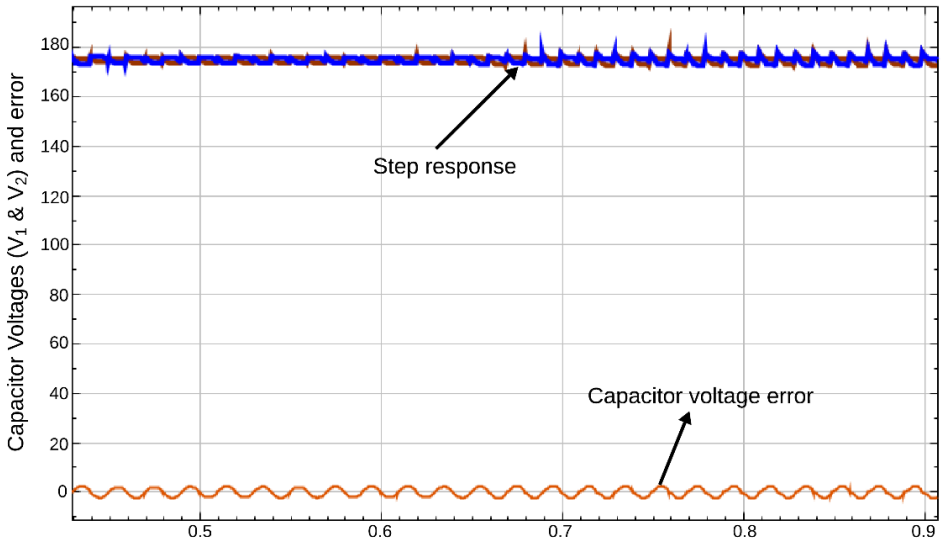


Figure 11. Step response of the capacitor voltages and capacitor voltage error ($V_{C_1} - V_{C_2}$) (Kondansatör gerilimleri ve kondansatör gerilim hatasının adım cevabı)

Table 4. Comparison of the proposed topology with conventional architectures (Önerile topolojinin klasik mimariler ile karşılaştırılması)

Feature / Topology	Conventional boost + 2-level inverter	Single-stage boost inverter	Proposed (3-level boost + 5-level T-type)
Power stage stages	Two-Stage	Single-Stage	Two-Stage
Voltage gain	Limited (High duty cycle issues)	High	High (Extended by 3-level boost)
Voltage stress on boost switches	Full Output Voltage (V_{out})	High Stress	Half Output Voltage ($V_{out}/2$)
Inverter output levels	2-level	Typically, 2 or 3-level	5-level
Output THD performance	Low (Requires large filter)	Moderate	High Quality (THD ≈ 1.0-1.2%)
Filter size requirement	Bulky (L,C)	Moderate	Compact (Reduced L,C)

Figure 11 displays the step response of the DC-link capacitor voltages V_{C_1} and V_{C_2} and the associated capacitor voltage error signal ($V_{C_1} - V_{C_2}$) for the three-level boost converter stage. At the instant of the step change (around t = 0.68 s), momentary fluctuation is observed in both capacitor voltages. However, due to the implemented neutral point balancing controller, the voltages quickly recover and are maintained symmetrically around their nominal value of approximately $175V_{dc}$. Crucially, the capacitor voltage error signal ($V_{C_1} - V_{C_2}$) is tightly regulated around the nominal zero reference throughout the step response, with peak ripple remaining at a very low magnitude. These results clearly demonstrate the boost converter successfully regulates the total DC bus voltage while concurrently ensuring voltage symmetry between the capacitors, even when subjected to dynamic load conditions.

Finally, to demonstrate the specific advantages of the proposed design, a comparison with conventional topologies is summarized in Table 4. As highlighted in the analysis, the proposed structure distinguishes itself by limiting the voltage stress on the boost switches to half of the DC-link voltage ($V_{out}/2$), unlike conventional topologies that expose components to the full bus voltage. Furthermore, the superior five-level output significantly minimizes THD without requiring bulky passive filters, proving that the proposed topology offers a more robust and efficient trade-off between component count and power quality.

6. DISCUSSION (TARTIŞMA)

This study proposed that integrating a three-level boost converter with a five-level T-type inverter would provide an advantage by decoupling the neutral-point balancing from the inverter stage, thereby simplifying control while enhancing power quality. The method involved developing a comprehensive mathematical model with corrected current dynamics and implementing a decoupled PI-based control strategy in the rotating reference frame. The simulation results strongly validate the mathematical model of the system. Proposed topology successfully achieved a stable symmetric DC-link of 350 V_{DC} and generated a five-level output. Especially, the system maintained a THD of 1.22% in steady-state and 1.01% under dynamic loading, strictly complying with IEEE 519 standards.

Despite these advantages, the proposed system has certain limitations. The cascaded structure increases the total semiconductor component count, which may lead to slightly higher conduction losses compared to single-stage architectures. Additionally, as observed in the dynamic analysis, the transient response was delayed (settling in 0.1 s) to prioritize DC-link voltage stability and protect the capacitors from severe fluctuations. Future work will focus on implementing advanced non-linear control strategies, such as MPC, to accelerate dynamic response times without compromising DC-bus stability.

7. CONCLUSION (SONUÇLAR)

In this paper, an integrated power conversion system combining a three-level boost converter and a single-phase five-level T-type inverter was designed and analyzed. The simulation results explicitly validated the theoretical design: the three-level boost converter successfully clamped the switch voltage stress to 175 V_{DC} (half of the 350 V_{DC}), and the implemented control strategy achieved a rapid settling time of approximately 0.1 s during load transients. With a superior output current THD of 1.01% under heavy load, the proposed cascaded topology stands out as a robust and high-efficiency solution for next-generation renewable energy applications where power quality and component longevity are paramount.

DECLARATION OF ETHICAL STANDARDS (ETİK STANDARTLARIN BEYANI)

The authors of this article declare that the materials and methods they use in their work do not require ethical committee approval and/or legal-specific permission.

Bu makalenin yazarları çalışmalarında kullandıkları materyal ve yöntemlerin etik kurul izni ve/veya yasal-özel bir izin gerektirmediğini beyan ederler.

AUTHORS' CONTRIBUTIONS (YAZARLARIN KATKILARI)

***Sadık ÖZDEMİR*:** He conducted the conception, design and supervision process.

Konsept geliştirme, tasarım ve denetim sürecini yönetmiştir.

Zafer ORTATEPE: He performed the interpretation, writing and critical review process.

Çeviri, yazım ve eleştirel inceleme süreçlerini gerçekleştirmiştir.

Kadir KUNT: He conducted the literature review, experiments and analyzed the results.

Literatür taramasını yapmış, deneyleri gerçekleştirmiş ve sonuçları analiz etmiştir.

CONFLICT OF INTEREST (ÇIKAR ÇATIŞMASI)

There is no conflict of interest in this study.

Bu çalışmada herhangi bir çıkar çatışması yoktur.

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