A Generic Circuit Model for Memristor-Based One Diode-One Resistor Devices

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***Abstract*—Memristor-based resistive random access memory (RRAM) devices are very good competitors for next generation non-volatile crossbar memory applications. The sneak paths problem is one of the main constraints in fabricating crossbar memory devices. The one diode-one resistor (1D1R) structure design is effective for suppressing the sneak paths problem. Suitable circuit models are needed to simulate semiconductor structures.**

A general circuit model for memristor-based one diode-one resistor structures is proposed in this work. The Simulation Program with Integrated Circuit Emphasis (SPICE) environment was used to simulate the designed circuit. Well-known mathematical models such as those of Strukov, Biolek, Joglekar, Prodromakis and Zha were used to simulate the memristor component of the circuit. The current-voltage characteristics were obtained for different mathematical models. All results were compatible with the expected characteristics. The best fit characteristics were acquired using the Zha and Strukov models.

Index Terms— **Circuit model, memristor, One diode-one resistor, resistive random access memory.**

I. INTRODUCTION

PRESENT MEMORY Technologies such as Dynamic Random Access Memory (DRAM), Static Random Access Memory (SRAM), NAND flash and NOR flash will soon encounter challenges due to the continued scaling down of their designs [1]. Several types of memory technologies have been suggested for next generation memory devices including Spin-Transfer Torque RAM (STT-RAM), Phase Change Memory (PCM) and Resistive RAM (ReRAM) [2]. Researchers have focused on the Resistive Random Access Memory (RRAM) because of its ultra-high density production potential, faster switching speed and lower energy consumption for non-volatile memory applications. Memristors, while used as resistive switching memory devices, are very good candidates for forthcoming RRAM devices as they have properties similar to those mentioned above [1]. One of the main problems in the production of crossbar RRAM devices is the sneak paths problem. The sneak paths problem can be defined as the crosstalk interference from current through nearby cells which can lead to misreading. The one diode-one resistor (1D1R) structure design is effective for suppressing the sneak paths problem [3]. Memristor-based 1D1R devices demonstrate pinched hysteresis memristive loops at the 1st quadrant (Positive – Positive) of the current-voltage (I-V) plane, whereas they show diode curves at the 3rd quadrant (Negative - Negative) [1,4]. A typical I-V curve for the 1D1R memristor device is depicted in Fig.1.

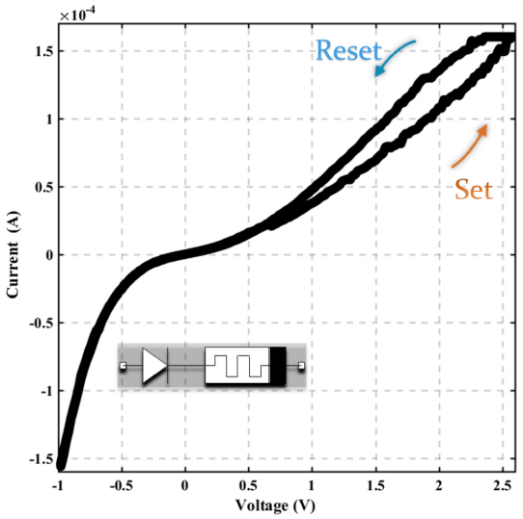

Fig.1. Schematic representation showing typical I-V curve of the memristor-based 1D1R structure [4]

In 2008, Williams et al. of the Hewlett-Packard (HP) Laboratories presented the fabrication and mathematical model of the semiconductor memristor [5], which was first introduced in 1971 by Chua [6]. The memristor provides the missing relationship between charge and flux for the completeness and symmetry of the circuit parameters [6]. A memristor is a two-terminal fundamental passive circuit element having a nonlinear pinched hysteresis I-V characteristic which could not be realized by any arrangement of the other three fundamental passive circuit elements (resistor, inductor and capacitor) [7].

Several mathematical models have been suggested for modeling the memristor, including those of Strukov [5], Biolek [8], Joglekar [9], Prodromakis [10] and Zha [11].

It is necessary to model the semiconductor structures when designing memristor-based circuits and systems because this enables the researchers to simulate some properties of the circuits like memristance and operation frequency without

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needing a physical device [12-13]. It seems that the realization of an actual memristor with the desired characteristics will not be possible in the near future. Since it is of great benefit to circuit designers to be able to model the memristor, researchers have focused on the SPICE-based models and emulators in order to use the memristor-based circuits [14]. Several suitable memristor emulators [15-27] and materials [28-29] have been proposed for memristor-based systems.

In this paper, a generic circuit model consisting of two diodes, two resistors and a memristor has been proposed to simulate the 1D1R structures. The current-voltage (I-V) characteristics of the circuit were obtained using different memristor models in a SPICE environment. The results obtained for the presented circuit showed that the models of Strukov [5] and Zha [11] were more compatible with the experimental results compared to the other models.

II. Linear Drift Model and Window Functions of the Memristor

Analysis and simulation of memristor-based systems require a proper model. The distinguishing feature of the memristor is that the I-V characteristics display the pinched hysteresis loop [6]. Several models have been suggested for achieving the pinched hysteresis loop [5,8-11]. The Strukov or HP memristor model based on the drift of oxygen vacancies, also known as the linear drift model, is widely used [5]. It was also the first model to be proposed.

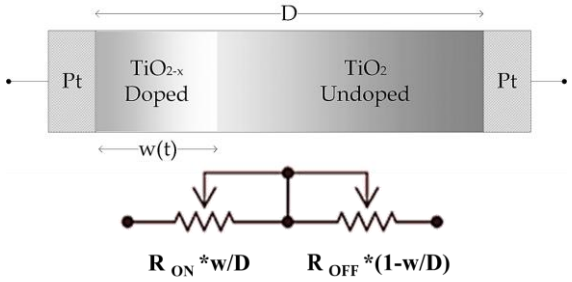


Fig.2. The structure of the TiO_2/TiO_{2-x} based memristor and simplified circuit model.

The amount of total resistance for a memristor can be calculated from the summation of the doped region resistance (R_{ON}*w/D) and un-doped region resistance (R_{OFF}*(1-w/D). The active-layer thickness of the device is stated as D, with w(t) representing the thickness of the doped region (**Fig. 2.**) [5].

The voltage and current relationship of the memristor is defined by Eq. (1) in the linear drift model.

$$v(t) = \left[R_{ON}x(t) + R_{OFF}(1-x(t))\right]i(t) \quad (1)$$

$$x(t) = \frac{w(t)}{D} \qquad \in (0,1) \quad (2)$$

where R_{ON} and R_{OFF} are the values of the resistance for w(t) = D and w(t) = 0, respectively.

From Equations (1) and (2), the memristance (M) can be expressed by Eq. (3).

$$M(q(t)) = \frac{v(t)}{i(t)} = R_{ON}x(t) + R_{OFF}(1-x(t)) \quad (3)$$

The change of the memristor resistance is represented by the x(t) variable in Eq. (2). The speed of change of the boundary between the un-doped and doped layers is stated by dx / dt in Eq. (4), where μ_v is the ion mobility of the TiO_2.

$$\frac{dx(t)}{dt} = \mu_v \frac{R_{on}}{D^2} i(t) \quad (4)$$

The following Eq. (5) is derived when Eq. (4) is taken as a time integral.

$$x(t) = \mu_v \frac{R_{on}}{D^2} q(t) \quad (5)$$

When Eq. (5) is put in its place in Eq. (3), the memristance expression is derived as Eq. (6)

$$M(q(t)) = R_{on}\mu_v \frac{R_{on}}{D^2} q(t) + R_{off}\left(1 - \mu_v \frac{R_{on}}{D^2} q(t)\right) \quad (6)$$

The simplified form of the linear drift model expression is shown in Eq. (7) on condition that $R_{ON} << R_{OFF}$, where M, μ, q, D, R_{ON} and R_{OFF} values are represented by memristance, mobility, charge, active-layer thickness, low-resistance state and high-resistance state, respectively [5].

$$M(q(t)) = R_{off}\left(1 - \mu_v \frac{R_{on}}{D^2} q(t)\right) \quad (7)$$

In nano scale devices, small voltage fluctuations can produce a large electric field, causing a non-linear drift of the ions near the boundary interfaces. A window function is needed to provide nonlinearity for the boundary problems pointed out above [5,8-11]. This function is realized by rearranging the expression of Eq. (4). In Eq. (8), the *f(x(t))* indicates the window function.

$$\frac{dx(t)}{dt} = \mu_v \frac{R_{on}}{D^2} i(t)\, f(x(t)) \quad (8)$$

Numerous window functions have been proposed for memristor modeling. Some of the suggested window functions include those of Strukov [5], Joglekar [9], Proromakis [10], Biolek [8] and Zha [11], as shown in Table I.

TABLE I
EXPRESSIONS OF WINDOW FUNCTIONS

Name	Expressions
Strukov	$f(x) = x - x^2$
Joglekar	$f(x) = 1 - (2x-1)^{2p}$
Prodromakis	$f(x) = j\left(1 - \left[(x-0.5)^2 + 0.75\right]^p\right)$
Biolek	$f(x) = 1 - (x - stp(-i))^{2p}$
Zha	$f(x) = j\left(1 - \left[0.25(x - stp(-i))^2 + 0.75\right]^p\right)$

III. SPICE MODEL OF THE CIRCUIT

Modeling of the semiconductor memristor is necessary in the designing of memristor-based circuits and systems. The Simulation Program with Integrated Circuit Emphasis (SPICE) simulators are of great benefit to circuit designers in modeling memristor-based systems [8,13-14,30].

The 1D1R memristor-based circuit model was designed by using two generic diodes, two resistors and one memristor (Fig. 3). The D1 and D2 diodes simulate the forward-bias region and reverse-bias region, respectively. The R3 resistor is used to prevent the reverse bias over-current which flows through the D2 diode. The R2 resistor models the contact resistance of the semiconductor devices. A sinusoidal voltage was applied to the circuit to acquire current-voltage characteristics. Finally, the R1 resistor was used to represent the internal resistance of the active layer.

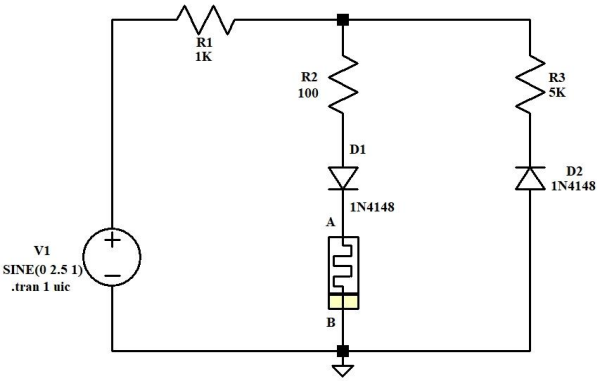


Fig.3. The proposed SPICE circuit model for 1D1R devices

The circuit was simulated using the LTSpice simulation program. The parameters required to achieve the mathematical model of the memristor are given in Table II, where μ is the dopant mobility, D is the active-layer thickness, p is the constant number for the window function, R_{ON} is the ON state resistance, R_{OFF} is the OFF state resistance and R_{INIT} is the initial state resistance. A 2.5 V 1 Hz sinus voltage source was used to run the circuit.

TABLE II
SPICE MODEL PARAMETERS OF THE MEMRISTOR

D	p	μ	R_{ON}	R_{OFF}	R_{INIT}
10 nm	1	$10*10^{-14}$	100 Ω	160 KΩ	35 KΩ

The comparative I-V characteristics of the circuit for all of the models are depicted in Figure 4. All models showed nearly equal characteristics in the 3rd quadrant of the I-V scale. The current-voltage relationship for the Joglekar [9] model exhibited a hard switching mechanism in the 1st memristive quadrant as compared to the other models, which showed smooth switching mechanisms (Fig. 4).

Current-voltage curves were obtained from the proposed circuit based on the memristor modeled with the mentioned window functions. Each I-V curve was then compared to the experimental result. The Joglekar, Biolek and Prodromakis models were not fully fitted to the experimental results (Fig. 5. a-c).

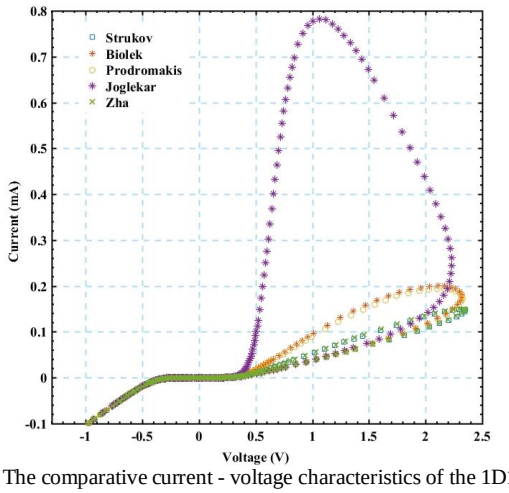
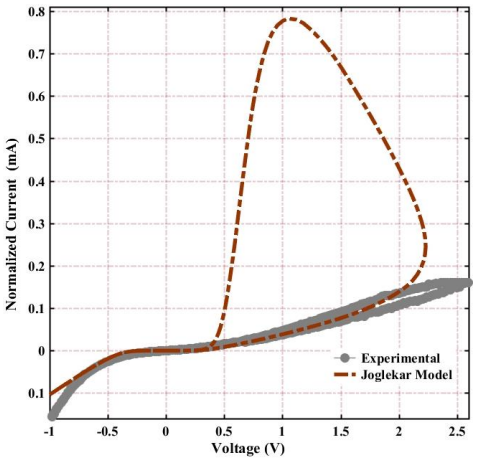


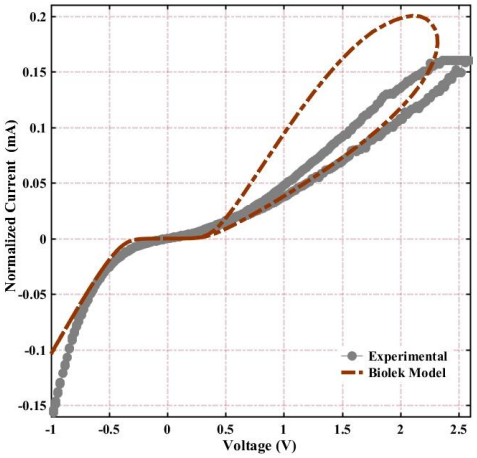
Fig.4. The comparative current - voltage characteristics of the 1D1R circuit model with different window functions

The Joglekar model in particular exhibited greatly different characteristics from the experimental results. Both the Biolek and Prodromakis models showed I-V curves similar to the experimental results, but these results were not fully fitted. The Zha and Strukov models were well fitted with the experimental curve (Fig. 5. d-e)

(a)



(b)



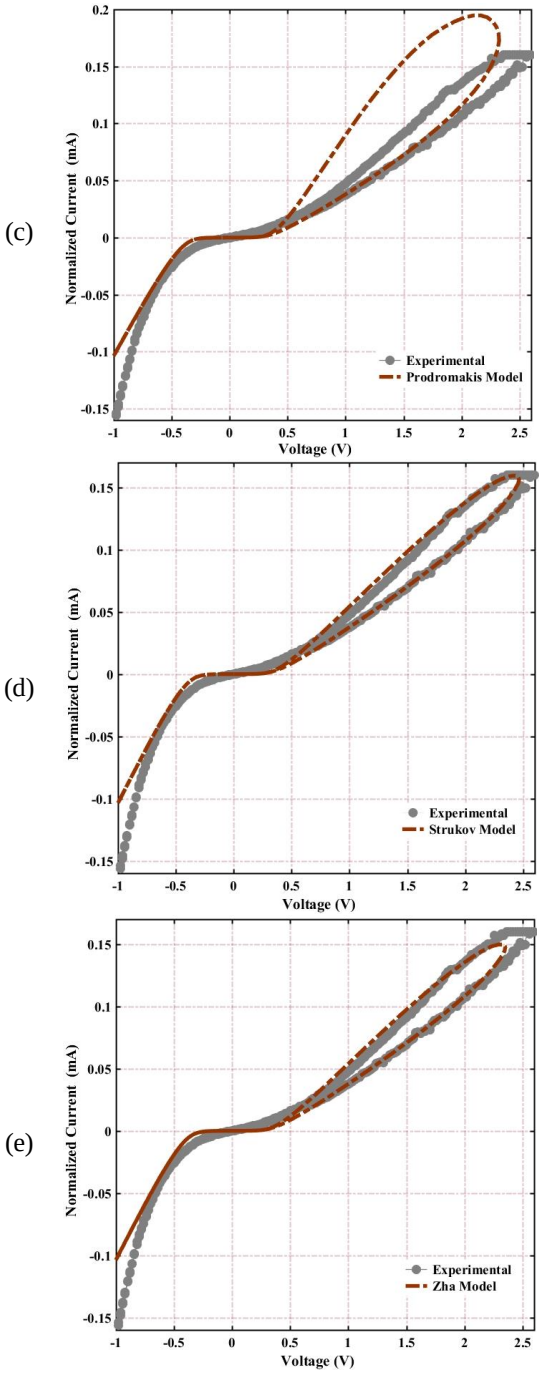


Fig.5. Current - voltage characteristics of 1D1R circuit model with different window functions: (a) Strukov, (b) Biolek, (c) Prodromakis, (d) Joglekar and (e) Zha

As a result, all models exhibited the expected memristor* based one diode-one resistor current-voltage characteristics. In other words, all models demonstrated pinched hysteresis memristive loops at the 1st quadrant (Positive - Positive) and diode curves at the 3rd quadrant (Negative - Negative) of the I-V planes [1,4]. The simulation results of the Zha [11] and Strukov [5] models exhibited the characteristics most similar to the experimental curve when compared to the others.

IV. CONCLUSIONS

A circuit was designed for the simulation of memristor-based 1D1R semiconductor structures using LTSpice. One memristor, two generic diodes and three resistors were used to design the circuit. The memristor element was modeled using different window functions. The circuit was simulated for each of the memristor models. All simulation results were compatible to the typical characteristics of 1D1R devices. The best fit results were obtained with the Zha and Strukov models.

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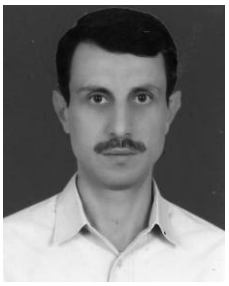
BIOGRAPHIES



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