Active Only Realization of Image Reject Complex Filter

H. A. YILDIZ

Abstract— **A new complex-filter which offers substantial area reduction is presented. According to this topology, the real-active only integrator is used for implementing the first order image reject filter. We have also discussed the design of a new area effective second order complex filter using lossy integrator building blocks. Using SPECTRE simulation tool, we have also justified the feasibility of the proposed circuit.**

Index Terms— **Real active-only integrator, Complex filters, Low-IF Receivers, Integrated Circuits.**

I. INTRODUCTION

IN ORDER to remedy the limitation of the zero IF and conventional IF receivers, low-IF architectures are proposed and effectively used in state-of the art RF transceivers [1]. This architecture provides a good trade-off in terms of power dissipation, integration capability and complexity.

However, the image problem is one major problem of such architectures and reduces overall system performance. The common approach to overcome this problem is to use complex filters which is usually used in the low-IF wireless receiver to filter out the image signal, for its easy integration on chip [2-6]. This kind of filters are formed from two paths in which a pair of signals (I and Q channels) with equal amplitude and quadratic phases are applied at their inputs.

In IC realization, these filters are intended to reject low image frequencies, therefore they require with capacitors with large values; hence occupy very large chip area due to the value of IF frequency [7-10].

On the other hand, circuits called as real active only filters, which use the intrinsic capacitors of the active devices at the various nodes of circuit, may be employed to implement IF filters with small chip area [11].

Herein, in order to achieve the issues encountered in realizing image-reject complex filters, it is proposed a design of a new area-effective first order complex-filter topology capable of providing electronically adjustable time constant.

To further justify the usefulness of the proposed approach, a second order complex filter using lossy integrator building blocks is proposed.

HACER ATAR YILDIZ, is with Department of Electronics and Communication Engineering University of Istanbul Technical University, Istanbul, Turkey,(e-mail: haceryildiz@itu.edu.tr).

https://orcid.org/0000-0002-2306-6008

In order to illustrate the feasibility of the filter, simulation results using SPECTRE in the CADENCE design tool are provided. The obtained results verify that the circuit is indeed feasible and can be used to implement area-effective complex filter circuit.

II. LOW IF RECEIVER ARCHITECTURE

A typical low-IF receiver architecture is given in Fig.1. The image reject complex filter entails very large time constants due to the low frequency operation in low IF circuits. Therefore, this kind of filters are required large value capacitors which occupy large chip area.

In order to achieve this issues, a new design of area effective complex filter topology is proposed in this paper. This filter employs real active-only integrator which operates at high-frequencies and provides electronically adjustable time constant with wide tuning area.
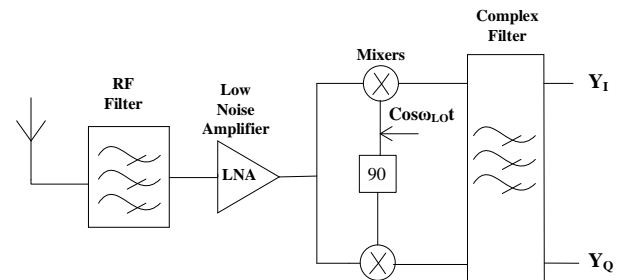

Fig.1. Block diagram of a typical low-IF Receiver [12]

III. CIRCUIT IMPLEMENTATIONS

A. Basics of Complex Filter

For realization of first order complex filter, the basic topology is given in Fig.2. After routine analysis, the equivalent transfer function is obtained as follows:

$$H(s) = \frac{V_0^I + jV_0^Q}{V_i^I + jV_i^Q} = \frac{g_m}{sC_p + g_0 - jg_{m,cpl}} \tag{1}$$

where g_0 is the nonzero output conductance of the CCCII. The complex first-order filter consists of a pair of real lossy integrators which are cross-coupled by the transconductors $g_{m,cpl}$. The transfer function of a complex first-order filter could be easily derived by performing a frequency shifting of the transfer function of the corresponding real first-order filter according to the transformation $s \rightarrow s - j\omega_0$
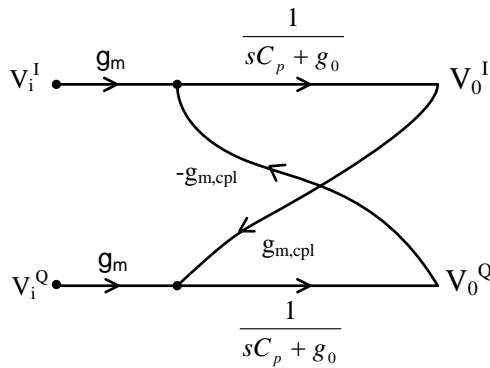
Fig.2. Basic topology for active-only first-order filter implementation

where ω_0 is the frequency shift given by:

$$\omega_0 \approx g_{m,cpl}/C_p \ , \quad \frac{g_{m,cpl}}{C_p} \rangle\rangle \frac{g_0}{C_p} \qquad (2)$$

As it can be seen from the equation above, it is derived an asymmetrical band-pass filter function from a first order filter function by providing frequency transformation.

The possible procedure is given in Fig.3 in accordance with the topology of Fig.2. This procedure describes how to turn a given active-only first-order filter into a complex filter.
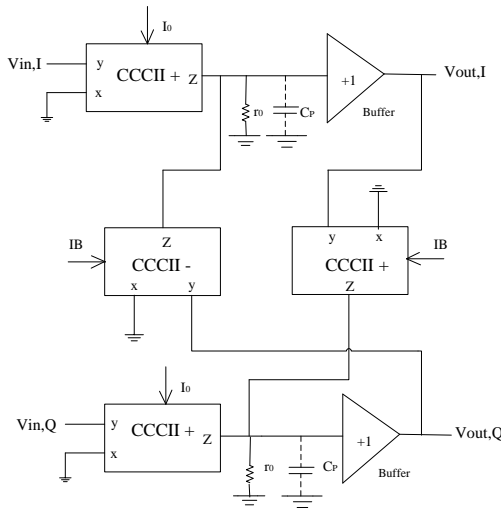

Fig.3. The functional block diagram of proposed first order complex filter

The cross-coupled branch's admittance $g_{m,cpl}$ can be realized by using intrinsic resistance of CCCII element, as shown in Fig.3. By coupling of these elements, first-order filter is converted into active-only complex filter. Taking into account all these modifications, we can obtain the following node equation:

$$V_0^Q = \frac{1}{sC_p + g_0}(g_m V_i^Q + g_{m,cpl} V_0^I) \qquad (3)$$

It should be also noted that in Fig.3, the transconductances of the CCCII elements are given by $g_{m,cpl} \approx \omega_0 C_P$, where ω_0 is the center frequency of the complex bandpass filter. Since the

basic first-order filter frequency is obtained as $\omega_p \approx g_m/C_P$ from (3), the transconductance ratio $g_{m,cpl}/g_m$ should be ω_0/ω_p.

B. Active only Integrator

As it can be seen from Fig.4a, it is showed a typical integrator which is commonly used in many filter circuits as the main building block. The transconductance element is used to perform the basic voltage to current converter in this circuit. The integrator's time constant of this circuit is described by the ratio of the equivalent capacitor seen at the output of the transconductance element (C_p) and the transconductance gain (g_m), which is the inverse of the CCCII's x-terminal parasitic resistance, r_x. x-terminal parasitic resistance is an electronically controllable parameter through a biasing current I_0. For the CMOS CCCII realization in [14], the expression that relates r_x to I_0 is given by:

$$r_x = \left(K\mu_n C_{ox} \frac{W}{L} I_0 \right)^{-1/2} \qquad (4)$$

where μ_n, C_{ox}, W/L and I_0 are respectively the electron mobility of NMOS, gate oxide capacitance per unit area, transistor aspect ratio and bias current of CCCII, while K is a constant dependent on the circuit topology.

In addition, the equivalent capacitor C_p consists of the parallel combination of the z-terminal intrinsic capacitors of the CCCIIs and the input capacitance of the voltage buffers at the circuit outputs.
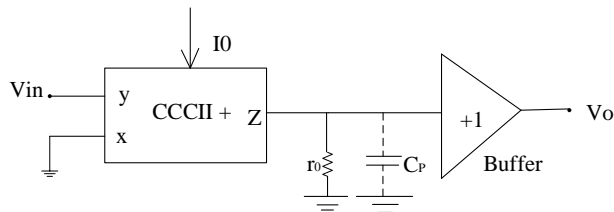
The input capacitance of the voltage buffer is substantially dominated by the gate-source capacitance of the MOSFET transistors and accepted highly linear as long as the transistors remain in saturation [13]. Therefore, the size of the MOS transistors at the buffer input are chosen as large as possible.

In this manner, the capacitance C_p becomes much more dominant than the z-terminal parasitic capacitances of the CCCIIs, so the proper integrator design is provided.

Considering the design criteria described above, the obtained integrator transfer function is characterized by the following transfer function:

$$V_0(s)/V_i(s) = 1/(sc_p + g_0)r_x \qquad (5)$$

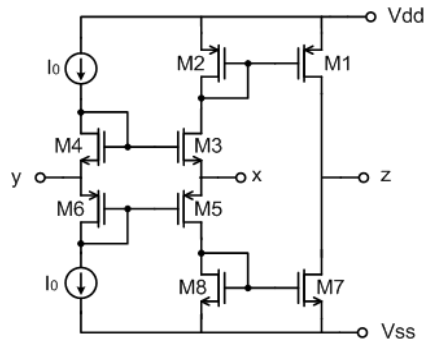The aspect ratio of the MOSFETs in Fig 4.b are chosen as given in Table 1.

Table.1 Transistor dimensions of CCCII

M_1	42μm/0.4μm
M_2	42μm/0.4μm
M_3-M_4	15μm/0.4μm
M_5-M_6	35μm/0.4μm
M_7	15μm/0.4μm
M_8	15μm/0.4μm
NMOS current mirrors	12 μm /1 μm
PMOS current mirrors	30 μm /1 μm

(a)

(b)

Fig.4 a) Active-only integrator block. b) Transistor level realization of the CCCII

IV. REALIZATION OF SECOND ORDER IMAGE-REJECT COMPLEX FILTER

In this section, it is considered the design issues of a second order complex filter based on real active-only filter with two integrator loop configurations in Fig.5. As it can be seen from this figure, two of CCCIIs are used to realize voltage–to-current conversion in the filter feedback loops [11].

It is possible to find the filter transfer functions with routine analysis as follow:

$$\frac{V_{LP}}{V_{in}} = -\frac{H_1\omega_0^2}{s^2 + s\dfrac{\omega_0}{Q} + \omega_0^2}, \qquad \frac{V_{LP}}{V_{in}} = -\frac{H_2 s\dfrac{\omega_0}{Q}}{s^2 + s\dfrac{\omega_0}{Q} + \omega_0^2} \qquad (6)$$

$$\omega_0 = \sqrt{\frac{1}{r_{x2}r_{x3}C_{p1}C_{p2}}} \qquad Q = \sqrt{\frac{C_{p1}}{C_{p2}}}\frac{r_{x4}}{\sqrt{r_{x2}r_{x3}}} \qquad (7)$$

where $\quad H_1 = \dfrac{r_{x3}}{r_{x5}}$, $\quad H_2 = \dfrac{r_{x4}}{r_{x5}}$

As it can be seen from the transfer function given above, it is possible to set the center frequency of the filter electronically to the desired value by intrinsic resistances r_{x2}, r_{x3}. It can be also adjusted the filter's quality factor by the intrinsic resistance, r_{x4}, after adjusting center frequency to the desired value.
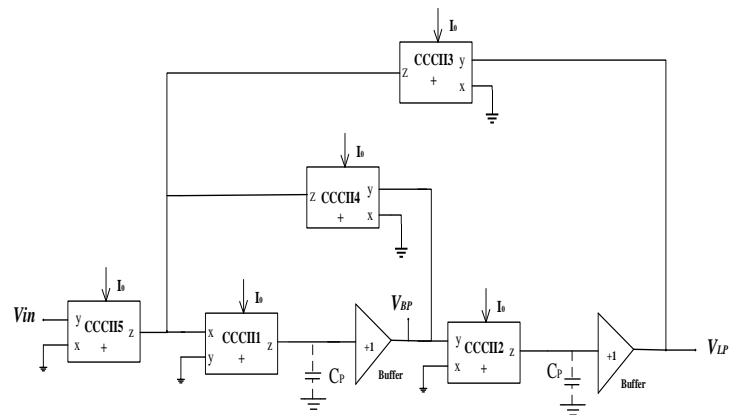

Fig. 5 Real active-only two integrator loop filter

By applying the procedure described in Section III to the circuit in Fig.5, we can obtain the second order complex filter shown in Fig.6. For this circuit implementation, two of the real active only loop filters are interconnected according to the procedure defined in Section III by appropriate using the intercoupling branches.

From the other side, as it can be known, in-phase (I) and quadrature (Q) components have equal amplitude and 90-degree phase difference in an ideal low IF mixer. In case of the gain and phase mismatch between in-phase and quadrature signals, IQ imbalance calibration circuit should be used. Therefore, it should be also noted that, the proposed second order complex filter implementation is realized without using any cascade configuration. Hence, it is expected that the IQ imbalance calibration circuit would be simple, in case of any gain and phase mismatches between in-phase and quadrature signals.

It can be seen that from the Fig.6, the proposed filter with all key parameters are electronically adjustable. It should be noted that, the lack of passive capacitors and resistors in the circuit design has significantly reduced the area covered by the filter.

Note that, the current conveyors which are used for cross-coupled branches are connected to the quadrature part of the filter as the same way and only one half of the circuit is shown for the sake of simplicity.
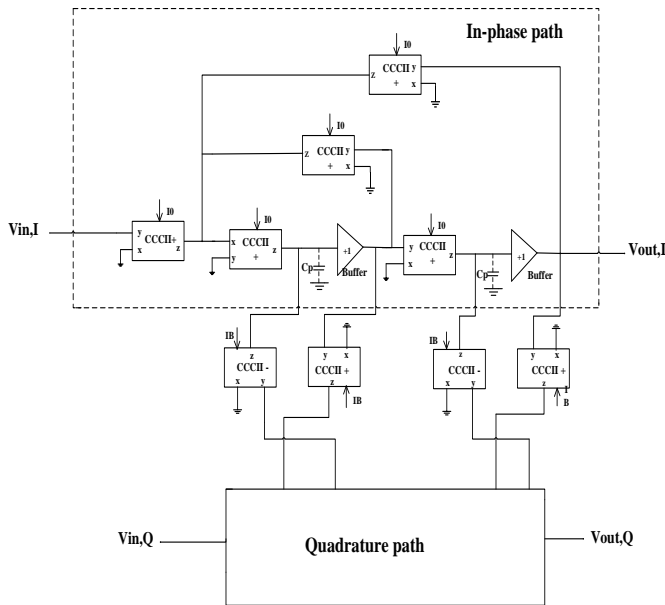
Fig.6 Implementation of the second-order complex filter (for the sake of simplicity, the quadrature part of the complex filter is not shown).

V. SIMULATION RESULTS

In order to justify the usefulness of the proposed approach, we have simulated first-order complex filter using design tool in CADENCE environment. All the current mirrors are designed by using simple current mirrors and the ±1.65V power supply is used for circuit biasing. The complex band-pass filter with a central frequency of 2MHz and a bandwidth of 1MHz is realized. For this design, integrator's cut-off frequency and frequency shift value are required to be 500kHz and 2MHz respectively. According to this implementation, the image-reject ratio is obtained to be as approximately 18dB, as shown in Fig.7.

As explained above, the complex band pass filter's center frequency and first order filter frequency are obtained respectively, such as: $\omega_0 = g_{m,cpl}/C_p$ and $\omega_p = g_m/C_p$. According to these equations, for a 2MHz bandpass filter characteristic with a bandwidth of 1MHz, the transconductance ratio should be 4 ($g_{m,cpl}/g_m = \omega_0/\omega_p$). Considering square-law characteristic of CMOS, it can easily be said that the current ratio is obtained also 16.
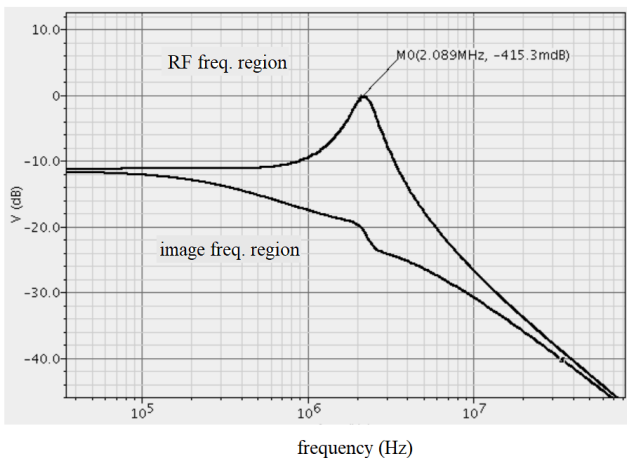

Fig.7 Normalized simulation result of first order complex filter

In addition, the proposed second order complex filter is realized with a center frequency of 8.5MHz and bandwidth of 2MHz by using 0.35um AMS CMOS process.
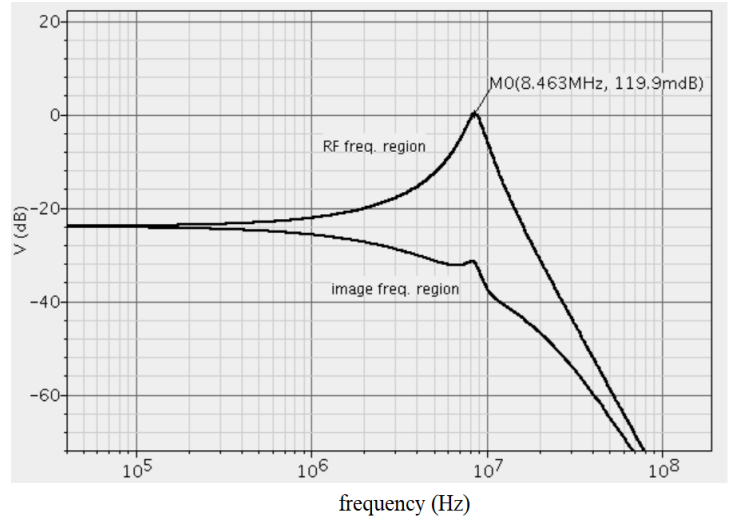

Fig.8 Normalized simulation result of second order complex filter

For the second order complex filter characteristic, the image rejecttion ratio is obtained approximately 30dB. The simulation results verfy that the proposed filters operate properly.

In addition to these simulations, it is obtained the simulation results of the second order complex filter for different biasing currents of CCCIIs. As shown in Fig.9, the bandpass filter can be adjusted electronically from 4.3 MHz to 9.3 MHz by controlling the biasing currents. As it can be seen clearly from these results, the bandpass filter has an electronic tuning range of about half a decade.
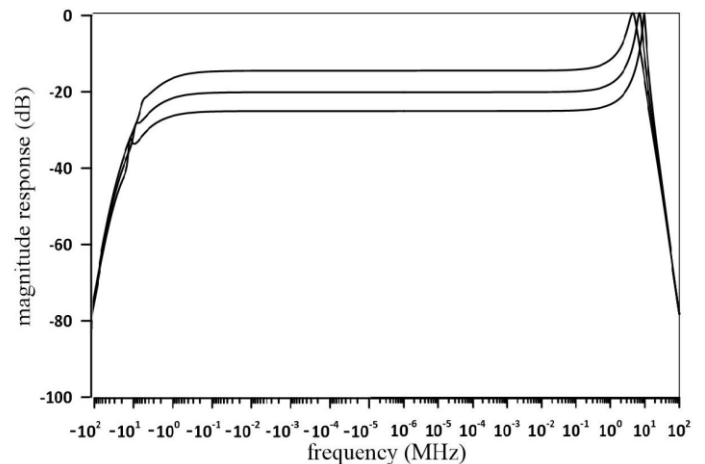

Fig.9 Normalized bandpass filter response of the second order complex filter for different values of the biasing currents

It should be said that, one of the important point to be considered in filter design is the sensitivity of the filter's quality factor (Q) and center frequency (ω_0). As a result, the sensitivity of the basic parameters of the filter circuit is shown below:

$$-S_{rx2}^{\omega 0} = -S_{rx3}^{\omega 0} = -S_{Cgs1}^{\omega 0} = -S_{Cgs2}^{\omega 0} = 0.5 \text{ and}$$

$$S_{Cp1}^{Q} = -S_{Cp2}^{Q} = -S_{rx2}^{Q} = -S_{rx3}^{Q} = 0.5$$

As it can be seen here, the sensitivities of the filter are smaller than one.

VI. CONCLUSION

In this paper, a first order and second order complex filters having a simple topology with electronically adjustable filter parameters are presented. The proposed filters are simulated using SPECTRE in the CADENCE without using any on chip bulky capacitors.

In order to illustrate the feasibility of the circuits, simulation results are obtained by using design tool in CADENCE environment. Note that in this implementation, it is achieved not only substantial reduction in the chip area but also complex filters capable of providing electronically controllable parameters. The another advantage of the filters is that it is possible to cascade the circuits. Therefore, it should be noted that, in application where high-order filters are required, the proposed complex filters can be used in cascade configuration to provide necessary image rejection.

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BIOGRAPHY

HACER ATAR YILDIZ was born in Trabzon, Turkey. She received the B.Sc. and M.Sc. degrees in Electronics Engineering from the Faculty of Electrical and Electronics Eng., Karadeniz Technical University, Turkey in 1997 and 2000, respectively. She received her Ph.D. degree in 2015 in Electronics Engineering from Istanbul Technical University. Her research interests include analog circuit design, active-only filters and analog neural networks.