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Using power decoupled technique for improvement of SEPIC Converter

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Abstract. In almost all solar to electrical power converter systems capacitor is placed across the solar panel. In these systems, the capacitor across the solar panel has unwanted ripple. The capacitor voltage is observed by the maximum power tracking controller and due to existence of unwanted ripple, Maximum power point tracking (MPPT) controller fall into error and MPPT will be lost. In this paper by using the power decoupled circuit in the grid connected systems, voltage ripple is eliminated and MPPT can be realized. In this paper a new inverter with high gain ratio and high efficiency base on SEPIC converter is proposed. The proposed converter maintains MPPT and improves the efficiency and voltage gain.

Keywords: Maximum Power Point Tracking, Power decoupling, SEPIC Converter, Solar panel, voltage ripple.

1. INTRODUCTION

Due to progress of the countries and communities, consumed power has been increasing continuously. Huge investment has been made to producing energy generator devices. Most of energy investments spend in environmentally friendly power source [1]. One of the widely used renewable energy source is sun energy that can be directly converted to electrical energy by solar panel. High efficient and reliable converter is need for renewable energy systems to reduce solar cell electricity price to a level which be compatible with Fossil fuel electricity prices. Many researchers had done many efforts to produce low cost converters for renewable systems. Among all of the renewable sources, due to free fuel price, and lower environmental pollution, the solar power has been taken to great attention. Beside of this advantage, it has some drawbacks such as high initial investment cost and the poor power conversion efficiency. To overcome these difficulties, many researches and studies is done and the cost of the system significantly decreases each year, but the price of solar power electricity is still high and future cost reduction are need. A solar electrical controller must maintain solar panel in an operation point in where maximum power can be captured. But maintaining solar power in maximum power point has some difficulties such as non linearity of output current versus voltage waveform in the solar cell and its variation with cell temperature and sun light [2]. Maximum power operating point must found quickly and tracking consciously by controller when environmental condition change.

In the grid connected photovoltaic systems, output power is AC while the power that produced by panel is DC. So difference between produced DC power and AC load power create undesirable ripple on capacitor which is connected across solar cell and is prevented inverter from proper realization of the MPPT technique.

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SEPIC converter with power coupled circuit will be discussed in this paper to increasing gain ratio and conversion efficiency of the systems [3]. In this topology a 100uF power capacitor is placed across the solar panel to realize the MPPT technique. Acceptable voltage ripple is lower than 1%, so when the power decupled circuit is not used, a large capacitor is required to keep the voltage ripple low. Employing large capacitor in the circuit will increase the size and decrease effective life time of the converter. In simulation as shown in Figure 1 the capacitor voltage varies from 43.5 to 50V, so the voltage ripple is equal to 6.5V as shown in Figure 2, that is out of the acceptable range and cant decorate the MPPT technique, So large capacitor is required to reach standard ripple. If the size of the capacitor is increased to 300mF, capacitor voltage increase from zero until reaches to about 47V in the simulation result as shown in Figure 3. In this condition voltage ripple is about 0.3V which is acceptable but 300mF is quite large capacitor that leads to increase converter volume and reduce power density and life time of the converter.

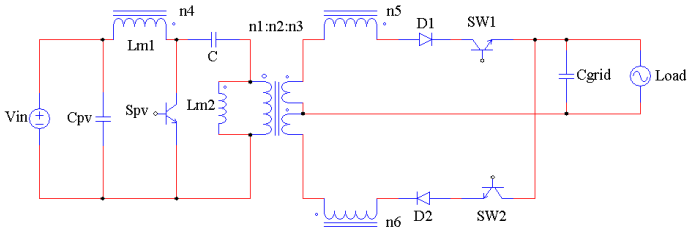

Figure 1. SEPIC inverter with high gain ratio and converter efficiency [3].

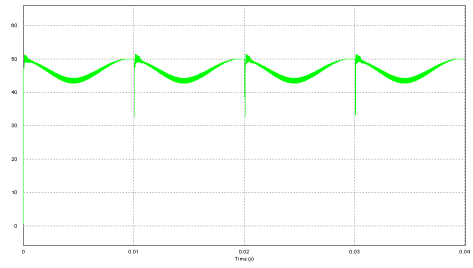

Figure 2. Ripple waveform across capacitor of CPV with capacitance of 100uf without power decouple circuit.

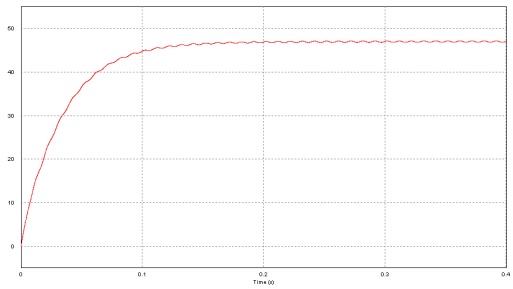

Figure 3. Ripple waveform across capacitor of CPV with capacitance of 300mF without power decouple circuit.

At first the power decoupling technique is briefly described and its relative law is discussed and finally a desirable topology base on high gain SEPIC inverter to implement power decupled circuit is presented. New Converter with power decoupled circuit will be simulated by PSIM software and its result is provided .MPPT controller maintain solar cell into its maximum operating point which lead to improving the converter efficiency.

2. POWER DECOUPLED RULES

In this paper the considered system which is based on power decoupled circuit, is resistive with unity power factor. Output current and voltage waveforms of this system are shown in Figure 4. In Resistive network like AC network displacement phase angle between voltage and current is zero. Instantaneous output power for resistive network can be calculated from (1) [4]:

$$p_{AC}(t) = \frac{1}{2} V_{pac} I_{pac} + \frac{1}{2} V_{pac} I_{pac} \cos(2wt) \tag{1}$$

Where V_{pac} is the peak of the AC voltage, I_{pac} is the peak of the AC current and w is angular frequency.

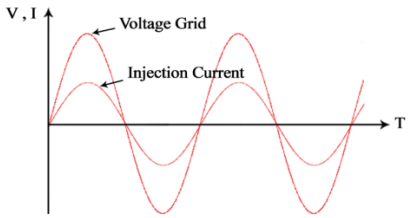

Figure 4. Continuous operation of the current and voltage in time domain.

In lossless inverter, output power is equal with power which is produced by solar cell [5]. This issue has been shown in Figure 5.

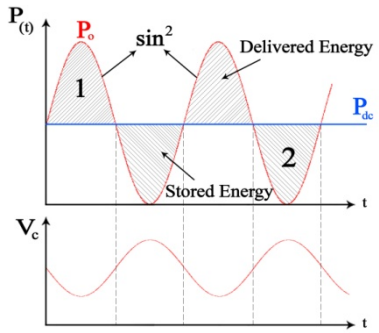

Figure 5. Power that process by the capacitor of across the solar cell.

Due to resistive output load (PF=1), output power will be sinusoidal with frequency twice as many as the grid frequency. In Figure 5 at the specified section shown by number of (1), output power is greater than the solar power and in section that specified with number of (2), output power is lower than cell power. In region of (1) decrease in power is compensated by stored energy in capacitor, so capacitor voltage decrease during this region. In region of (2) excessive power absorbed by capacitor and its voltage will increase and the voltage which is dropped in region of (1) is recovered. This event is repeating and the capacitor voltage rise and fall constantly and forced some undesirable ripples.

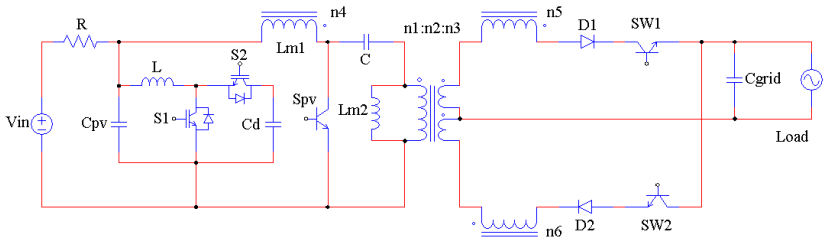

Figure 6. Proposed inverter circuit.

Goal of this paper is Appling power decoupled circuit on the single phase single stage grid connected photovoltaic inverters to cancel voltage ripple of input capacitor of the solar panel. Proposed inverter is based on a high gain ratio and conversion efficiency SEPIC type converter which associated with a power decoupling circuit.

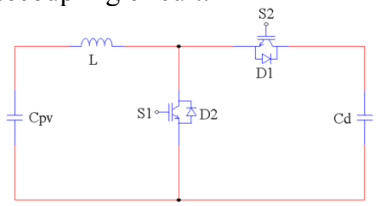

Figure 7. Proposed power decoupled circuit.

Power decoupled circuit has been employed to eliminate capacitor voltage ripple with using only small capacitor. The proposed decoupled circuit according to Figure 7 is a bidirectional buck - boost converter. The feature of the proposed converter is that it can draw current when output load power is higher than cell power and deliver current in contrary conditions. The converter is configured by an inductor, two capacitors and two bidirectional IGBT switches.
In the proposed inverter voltage ripple is eliminated while 100uf capacitor is used. So the converter size and life time are improved.

3. PRINCIPLE OPERATION OF THE PROPOSED DECOUPLING CIRCUIT

Converter has two operation modes with in each half cycle. Switch operates at frequency as high as 100kHz. Switches time operation and current direction is determining by circuit situation, amount of the required load power and PV cell produced power.

Converter operation divided to two half cycle. Duration of each half cycle is equal with $T_s/2$ (T_s is half of the period of the utility grid). As can be seen in Figure 8, the first half cycle is when the output power is lower than panel cell power. So capacitor voltage tend to risen but by the current which its direction is from C_{pv} to C_d though switch of S_1 and diode of D_1, excessive power is diverted from C_{pv}, hence increasing capacitor voltage is concealing.

In second half cycle according to Figure 9, when load energy is larger than panel energy. The capacitor voltage tend to be decreased by the current which its direction is from C_{pv} to C_d though the switch of S_2 and diode D_2, shortage power is injected to C_{pv} from C_d hence decreasing capacitor voltage is concealing.

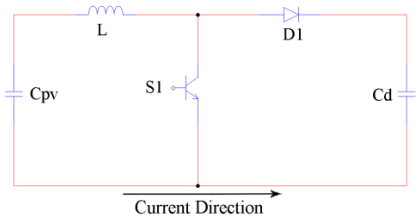

Figure 8. Proposed power decoupled circuit in first half cycle.

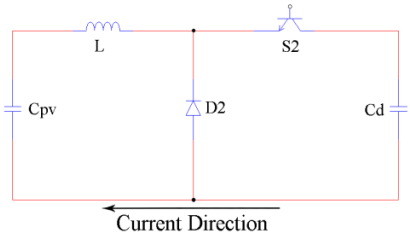

Figure 9. Proposed power decoupled circuit in second half cycle.

4. CIRCUIT OPERATION MODES

The proposed converter has four distinct operation modes which their equivalent circuits for each of them are shown in Figure 10. Mode 1 and 2 operate for positive half cycle and mode 3 and 4 operate for negative half cycle.

Mode 1: As shown in Figure 10 this mode starts when switch is turned on. During this mode S_1 is on and all remained semiconductors are off. Inductor absorbs power from capacitor C_{pv} and its current starts to increase. Inductor is charging to $V_{CPV}DT/L$ with slop of the V_{CPV}/L. When the capacitor voltage reaches to reference voltage the switch is turned off under maximum inductor current and this mode finishes. The Switch voltage is V_{cpv} when it is off.

Mode 2: In begin of this mode switch is turning off and D_1 forces to conduct inductor current. During this mode D_1 is on and all remained semiconductors are in off state. Stored energy in inductor of L is transferred to decoupled capacitor of C_d. Inductor current decreases with slop of $(V_{CPV}-V_{cd})/L$ and the capacitor continuous to charge until it completely charged. In first and second mode positive half cycle is done and energy supplied to C_d from C_{pv}.

Mode 3: Because the converter operates in negative half cycle, the current flows in opposite direction of the two previous modes. This mode starts with turning the switch S_2 on. Inductor current passes zero and its direction changes. The energy of C_d is transferred in to the inductor, so the inductor current rises in reverse direction. Inductor current rises with rate which is defined by $(V_{Cd} - V_{CPV}/L)$.

Mode4: This mode begins when anti-parallel diode of S_2starts to conducting. In first of this mode voltage of the decoupled capacitor has been reduced to its minimum value. In this mode, capacitor C_{PV} is charged by the inductor current. So the capacitor voltage will increase and

inductor current starts to fall toward zero with slop of $-V_{CPV}/L$. At the end of this mode, inductor current reaches zero and negative cycle of the circuit will be completed.

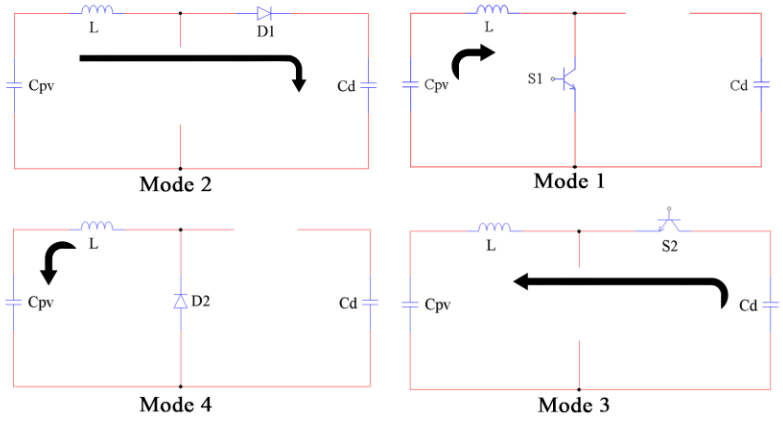

Figure 10. Different equivalent circuit mode of the proposed converter.

5. CALCULATION OF THE DECOUPLE CAPACITOR

Decoupled capacitor is considered in one cycle as output of the boost converter and in other half cycle as input of the buck converter. Energy of the decoupled capacitor in where is output of the boost converter can be calculated from following equation:

$$p_1 = \frac{1}{2} CV^2 \tag{2}$$

In where V as mentioned earlier is V_{max} and C is the capacitance of the capacitor.
Energy of the capacitor in where is input of the buck converter is obtained from:

$$P_2 = \frac{1}{2} C(V - \Delta V)^2 \tag{3}$$

According to the circuit operation modes, ΔV is variation of decoupling capacitor voltage. In this mode V-ΔV is equal with V_{in}. In this state, V_{in} is greater than the solar panel voltage.

As it can be seen from Figure 11 energy in dashed region is excessive energy. The amount of the excessive energy can be calculated from (4). It is the energy that solar cell cannot producing and must be provided by C_{pv}.

$$excessive, power = \frac{p_{out}}{w} \tag{4}$$

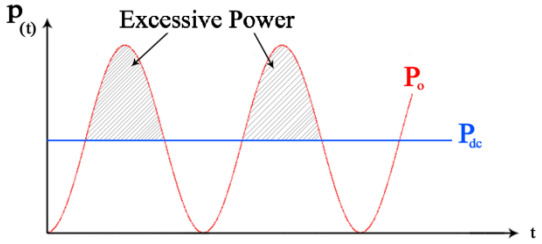

Figure11. Output and input power relation with excessive energy.

According to Figure 11, cell power and instantaneous power are different, so according to (5) to eliminate the voltage ripple, decoupled power capacitor in both cycle must compensate difference between required network power and cell power.

$$\frac{p_{out}}{w} = \frac{1}{2}CV_{\max}^2 - \frac{1}{2}CV_{\min}^2 \qquad (5)$$

Switch voltage stress of the power decupled circuit is determined by value of the V_{max} and V_{min} during the converter design procedure. As it is shown in equation (5), V_{max} and V_{min} are calculated by maximum allowable voltage for the converter switches. Decreasing and increasing voltage of the power decoupled capacitor depend on frequency, output voltage and power and ripple voltage. For example with increasing voltage, voltage ripple, frequency and capacitance of decouple capacitor will be decreased. But it must be noted that the output power and frequency are constant and are determined by the grid network. Only parameter that can be changed is switch voltage stress.

Output voltage is $220V_{rms}$, output current is $4.25A_{rms}$ and frequency is 50Hz. Design can be done in such as way that switch voltage stress is low, so in this design example switch voltage stress be lower than 200V. Voltage ripple of across capacitor must be lower than 1% of the produced voltage of the PV panel which is equal with about 0.4V. By using (5) and specified parameters, minimum value of the capacitor is calculated 800uF and in simulation 1000uFcapacitor is selected. With reducing switches voltage stress, decoupled capacitor and so on voltage ripple increases and decreases respectively. In this case, the result will be ideal. But increasing the size of capacitor is acceptable until certain value and should be limited on a reasonable range. A trade off exist between capacitance of the decouple capacitor and the voltage ripple of across of the C_{PV}.

6. SIMULATION RESULT

Schematic of the simulated converter including control circuit is shown in Figure 12. The proposed converter is simulated by PSIM software. Parameters of the converter that are used in simulation are depicted in Table 1 waveform of the output voltage inverter, output current inverter and the voltage ripple across of the C_{PV} are shown in figure 13, 14 and 15 respectively.

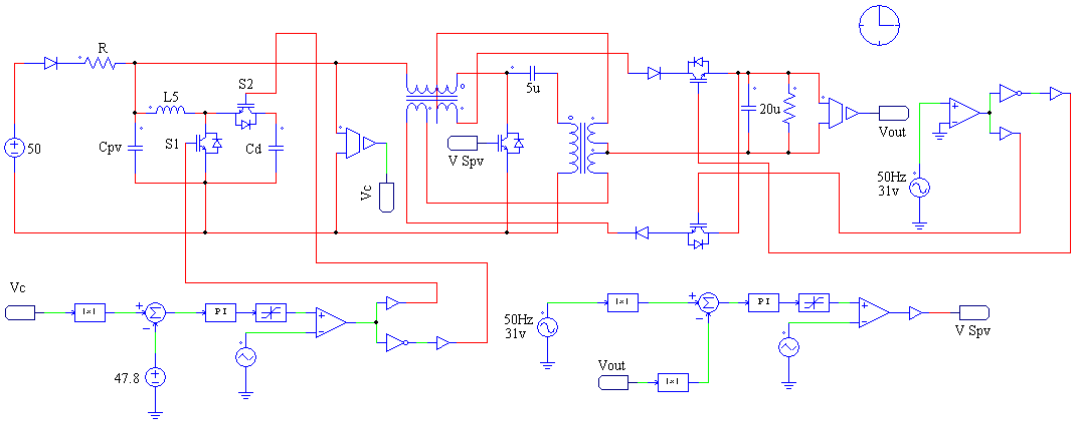

Figure 12. Schematic of proposed SEPIC type inverter with power decupled circuit which is simulated by PSIM software

As can be seen in the Figure 15 voltage ripple in the proposed converter is 0.4V which is 6.1V lower in comparison with previous circuit. This value oscillates across 46.8V, so the voltage varies between 46.6V and 47V. Both capacitor value and voltage ripple have acceptable value.

Table 1. Parameter used in simulation.

Component	value	Component	value
Coupled inductor (Lm1)	2 µH	Frequency of the main switch (S1)	100 KHZ
Magnetizing inductance of the transformer	2 µH	Frequency of the output switch	50 HZ
Capacitor of C	5 µF	Transformer turn ratio (n)	4
Output capacitor (Co)	20 µF	Coupled inductor turn ratio (m)	4
Output load (Ro)	50 Ω	Resonance capacitor (Cs)	5 µF
AC reference voltage (Vref)	31 V	Capacitor of across of the panel terminal (Cpv)	100 µF
DC reference voltage (Vref)	47.8 V	Power decoupled circuit inductor	100 µH
Input voltage (Vin)	50 V	Power decoupled capacitor (Cd)	1000 µF
Auxiliary circuit inductor (Lr)	1 µh	Frequency of the power decoupled circuit	100 KHZ

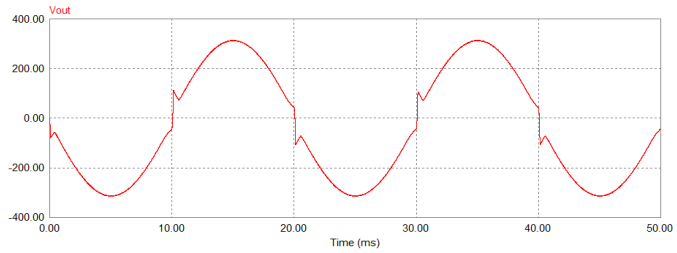

Figure 13. Inverter output voltage.

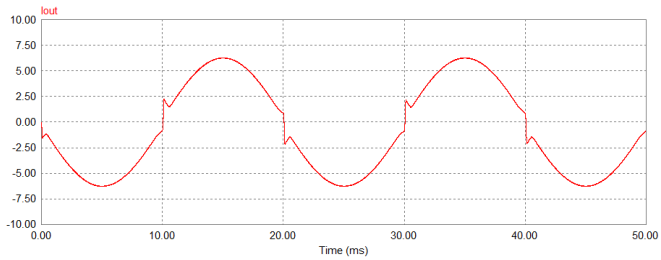

Figure 14. Inverter output current.

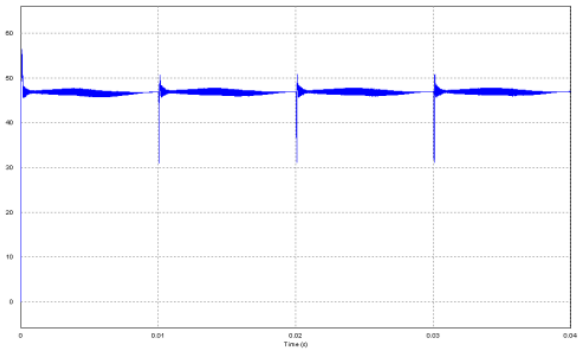

Figure 15. Ripple waveform of capacitor of CPV (100uf) with power decouple circuit.

7. CONCLUSIONS

In this paper initially high gain ratio SEPIC type inverter is introduced. In order to surpass voltage ripple of the Capacitor which is placed across the solar panel, power decoupled circuit is introduced and its operation mode describes in detail. Simulation results with employing power decoupled circuit are presented. Voltage ripple is eliminated with using small capacitor in across of solar cell. Using small capacitor improves the circuit efficiency and its life time. But this circuit (proposed inverter) has some drawbacks such as higher number of components and switching losses in power decoupled circuit. Switching losses can be minimized by using soft switching technique. In table 2 proposed converters is compared with inverter without power decoupled circuit. Proposed converter has advantage of high voltage gain ratio and efficiency conversion which makes it suitable for photovoltaic AC module application.

Table 2. Comparison between proposed inverter and inverter without power decouple circuit.

	SEPIC inverter without power decouple circuit	SEPIC inverter with power decouple circuit
Voltage Ripple of Cpv	6.5 v	Lower than 0.4 v
Capacitance of Cpv	100uf	100uf
Excessive cost	-	One inductor ,one capacitor and two switches
MPPT ISSUE	Error in MPPT	Maintain MPPT

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