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A Technique for Testing Network Connections in Parallel with Mesh Topology

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Abstract. In this paper, we connections between switches in the mesh network topology in a parallel way we've tested. The method is based on a built-in self-test, the use of buffers FIFO Each of the switches, test all connections between switches is done in parallel, not only test application time, but the area overhead of the network is reduced.

Keywords: Built-In Self-Test, Hearing, Connections, Network with Mesh Topology.

1. INTRODUCTION

Today, with advances in technology with high density integrated circuits, designers are able to nucleate the functional components of a system are integrated in a single chip. The chip, the chip - on - system (SOC) Called, may contain a mixture of different sizes and compositions are identical. Methodologies designed SOC Today has been undergoing major changes due to the emergence of substrates SOC With a large set of core functionality is embedded [1]. Data exchange between the cells through a specific communication infrastructure (eg, a shared bus) is carried out. The limitations of the communication infrastructure and the increasing complexity of chip design problems for designers and chip makers to devise complex a large number of functional cores SOC Has made possible. The mesh topology network with a new architecture, in order to solve some of the challenges that designers SOC Great faced was proposed. With a mesh topology network architecture consist entirely of switches and wires (connections) between the switches. The core functionality of the interface blocks and switches are connected through the switches on the basis of a communication protocol, Data rejected Are exchanged. Switch mesh network topology and connections between them play a key role in the communication structure. The There At the beginning of advent SOC Researchers to focus more on their core test performance, test communications infrastructure and are less of a concern. Therefore, test the communications infrastructure must also be considered. The use of nanometer technology in a mesh topology network effects in the hearing International connections has increased dramatically. Alqahay connections and mutual capacitance signal accuracy by adding noise to the carrier signal and the delayed impact and potential for logical errors and the failure to provide chips. So far, several techniques to reduce the hearing effects suggested [2,3,4]. On the other hand, due to some limitations in the design and unpredictable effects that lead to noise and delay, the test should the hearing during the manufacturing process and also during chip operation is performed. In recent years, several techniques for the production of test gate level circuits have been developed for fitting [5,6,7,8,9]. Unlike these techniques, in this paper we focused on testing the connections in the network. Recently, several methods for testing the communications infrastructure of the network and system is presented. The authors [10] By using this mesh topology network structure in a reversible way to transfer test data from an external tester (ATE) Towards the compounds have been tested. They are the

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switches and connections that have already been tested, re-use for testing other compounds have been tested. In [11] Also utilizes standard JTAG And with changes in the cells of the standard survey, the connections between the core SOC To test the hearing At the level of the target system. In this method, test data through a ATE A serial shift register that surrounds the nucleus, sent a series of experiments to analyze responses are transferred abroad. the hearing effect, due to the nature of time, the need to test the speed of the speed of operation of the circuit under test done (a test chip with faster performance). This type of experiment ATE For systems. GHz It is costly because it requires ATE With performance levels GHz A. On the other hand, external testing requires a test access mechanism (TAM) To apply the test data connections that are deeply embedded in the system, which may result in unacceptable performance overhead or area. In contrast to the external tester, built-in self test (BIST) A good way to test the speed of the chip performance is bugs, because it depends on ATE Is not (depending only on the set BIST Is.) In [12], A methodology BIST To test the connection between the switches in the network with mesh topology of point - to - point, single broadcast and multicast has been proposed. The method BIST Point - to - point presentations, generating a pair of - the - test / detector - Error - Test (TDG / TED) Have used to test each link, which includes the high area overhead. In this paper, we use a method BIST Connections between switches in the mesh network topology, we have targeted. We use this switch to buffer any embedded hardware BIST In its proposal, the way we provide all Connections between switches are tested in parallel. The proposed method not only guarantees a minimum test application time, but using a buffer of each switch, the overhead of the Ahty Is reduced. On the other hand, we have no way routing algorithms and control network, and can be applied to a class of large networks, even if they use different routing algorithms.

In the next section, we examine the structure of the model fitting shapes the hearing on self-test, including test pattern generator (TPG) And controller BIST Section 3 is given. In the fourth section, the configuration and reuse the buffer FIFO Each switch mesh network topology Has been described. Analysis of clock distribution method and its application to implement a parallel test for all connections between switches in Section V is given. Experimental results in terms of area overhead and test application time in the Sixth Are given. Section VII concludes the paper discusses and offers.

2. TEST VECTORS FOR BUGS THE HEARING

Built-in self-test method is proposed for the development of this paper, we model Maximum Aggressor Fault (Or briefly Model MAF) [13]. The effects hearing presented 've used. Model MAF An abstract presentation of all physical defects and process variations may be causing the errors is the hearing . This model is a model of the drawbacks is that the effects are due the hearing. These drawbacks include negative glitch, positive glitch, falling delay And rising delay Are the order of the sign By G_n، G_p، D_f، D_r And In this article I will refer to them. In this model, at any time, only one line (wire) connection as a victim and aggressor lines are considered. The worst way to make an impact on the joints provides the hearing makes. Figure 1 shows the signal transmission lines on the victim and attacker to create hearing impact on the victim line. For example, to create forms On the victim V The amount of the victim to the '1' Stable, and a transfer of '1' To '0' ('1'→'0') The aggressive lines are done simultaneously. We also hearing impact on the model MAF By using HSPICE For technology 0.18um Evaluated. The minimum width of the wire and simulation The minimum space between the wire and was considered a junction 8 of the Yeti the hearing effects to shapes G_p The victim wires up to 80% Voltage VDD Reaches.

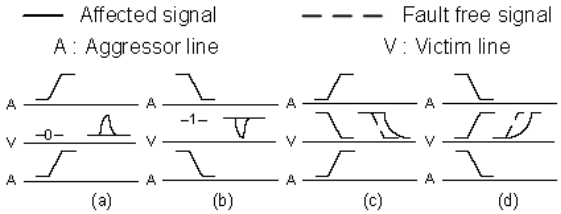

Figure 1. Error the hearing: (A) Positive Glitch (b) Negative Glitch (c) Falling Delay Fault (d) Rising Delay fault [13] (A: aggressor line, V: victim line).

Table 1 test vectors for testing maf wire i i suggest a connection. According to this table, eight test vectors to test the wires is looking for a connection with n wire, 8n vector test is required. Thus, for any errors the hearing, two successive test vectors are needed, as a test maximum aggressor (ma) defined. The weakness of this method is to provide a connection with n wire, for n large, requiring a large number of test vectors 8n because generally 4n forms must be tested, which consequently 4n experiment ma which includes 8n vector tests are to be done. So, we've used a technique in which test vectors layout test data volume without any negative impact on the coating tests ma reduces. Our proposed layout is presented in table 2. As can be seen in the left column of the table, with three wire test vector victim i i just bugs and are activated. Three vectors tested for activation problems and requirements, which are shown in the right column of the table. By this arrangement, we will examine the sequence. The first sequence of test vectors ma arranged in the left column of the table is formed and the second sequence, the complementary sequence is first. The first trail just bugs second sequence just bugs for each wire of a connection is active. So to test a connection with n wire, overall 6n take the test ma necessary because of the length of each sequence 3n and while the original model maf to 8n take the test ma is.

Table 1. Test sequences for wireless i

#	MAF	L_{i-2}	L_{i-1}	L_i	L_{i+1}
1	G_n	1	1	**1**	1
2		0	0	**1**	0
3	G_p	0	0	**0**	0
4		1	1	**0**	1
5	D_f	0	0	**1**	0
6		1	1	**0**	1
7	D_r	1	1	**0**	1
8		0	0	**1**	0

Table 2. An Array of Test Vectors MA for Detecting Bugs the Hearing

#	MAF	L_0	L_1	...	L_{n-3}	L_{n-2}	L_{n-1}
1	G_n	1	1	...	1	1	**1**
2		0	0	...	0	0	**1**
3	D_f	1	1	...	1	1	**0**
4	G_n	1	1	...	1	**1**	1
5		0	0	...	0	**1**	0
6	D_f	1	1	...	1	**0**	1
.		.	.	...	.	.	.
.		.	.	...	.	.	.
.		.	.	...	.	.	.
3N-2	G_n	**1**	1	...	1	1	1
3N-1		**1**	0	...	0	0	0
3N	D_f	**0**	1	...	1	1	1

#	MAF	L_0	L_1	...	L_{n-3}	L_{n-2}	L_{n-1}
1	G_p	0	0	...	0	0	**0**
2		1	1	...	1	1	**0**
3	D_r	0	0	...	0	0	**1**
4	G_p	0	0	...	0	**0**	0
5		1	1	...	1	**0**	1
6	D_r	0	0	...	0	**1**	0
.		.	.	...	.	.	.
.		.	.	...	.	.	.
.		.	.	...	.	.	.
3N-2	G_p	**0**	0	...	0	0	0
3N-1		**0**	1	...	1	1	1
3N	D_r	**1**	0	...	0	0	0

3. HARDWARE TEST PATTERN GENERATOR

One of the requirements for testing is to test the speed of bugs the hearing speed circuits (speed performance chips) the test run. Built-in self-test method, a test chip provides fast performance. Therefore, the design of a test pattern generator (tpg) with high flexibility and minimal area overhead for generating sequences listed in table 2, one of the requirements of the proposed method in this paper. In this section, we briefly hardware design tpg explain. The purpose of this section is to identify the components generating the configuration and use of this buffer has a switch for embedding the the proposed generator at each switch in section 4 be reiterated. This generator has two parts: the logic of the generator and its controller. Since for each line (wire) of a connection test must be administered three vectors (vectors regardless of the amendment), the two of them but the pattern all - '1' simply can not be generated by a shift register. The shift register with string n beatty "100..0" initial and its output is also capable of amendment. The class also needs to be a role model for all - '1' to complement the output of the generator and the other to generate test sequences provided in the right column of table 2. The controller generates the signals on the logic of the generator to provide for. 2. The control of as shown in figure a finite state machine (fsm) which has four modes. The transition from one state to another state, one of the three signals tck, and the rationale for the generator produces. Signal the shift register clock signals amendment to the shift register output signal pattern for all - '1' is activated. According to figure 2, the machine upon receiving the active signal e the idle state started and the transfer of to runs. The alternating cycle of until upon test production runs and sequence mode returns. Table 3 shows the results of the synthesis of in terms of area overhead show. According to this table, by reducing the clock frequency, the number of control gates dropped.

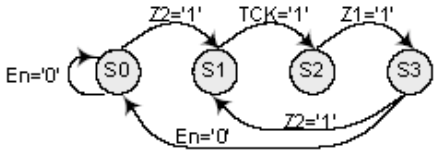

Figure 2. Test pattern generator controller

Table 3. Afzarmvld difficult area overhead test pattern.

10 MHz			1 GHz			Link width #bits
Total #gates	Controller #gates	TPG #gates	Total #gates	Controller #gates	TPG #ga tes	
708	81	624	730	103	624	16
1339	81	1248	1361	103	1248	32
2732	81	2496	2745	103	2496	64

4. THE STRUCTURE OF BIST RECOMMENDED

Switch network with mesh topology is generally a combination of a functional block operations for arbitration, routing and error control, and memory blocks FIFO As buffers, are [14,15]. Buffers FIFO You can register as a bank [16] Or arrays SRAM Dedicated [17] Implemented. In this paper, we examine the connections between switches. So we have to improvise TPG Proposed (see Section 3) in the switch from the switching buffer 've reuse, and made it possible to all communication links (Connections) Without the switches in the network to be tested in parallel. For this purpose, we have applied some changes to reconfigure the buffer cells can be tested in fashion. By redeploying the first word of an output buffer of each switch, tpg the

minimum area overhead can be embedded in the switch. Controller bist (previously served as controller tpg was introduced - see figure 2), which includes four modes, provides control signals necessary for generating embedded. The controller has low hardware overhead and embedding it in a low area overhead switch on switch l impose it. At the beginning of the experiment, the controller bist by a ate is activated in the first test cycle (setup bist), the first word of the buffer cells in the test mode. At the same time, the cells with initial values (eg, "100... 0") are the primary. In subsequent cycles, based controller fsm figure 2 acts necessary to produce a sequence of test signals by tpg embedded, is generated. Because of the one-way nature of connections in a network with mesh topology, each switch data through an output port to an input port of the switch adjacent to send and receive an immediate switch. Thus, communication links should be tested in two opposite directions.. However, consider switching to a four input ports and four output ports. Figure 3 hardware bist this switch is embedded in the show. Upon setup bist, experimental data by tpg each switch is embedded in the production and testing of links connected to the switch output ports can be exported to neighboring switches. At the same time the test answers

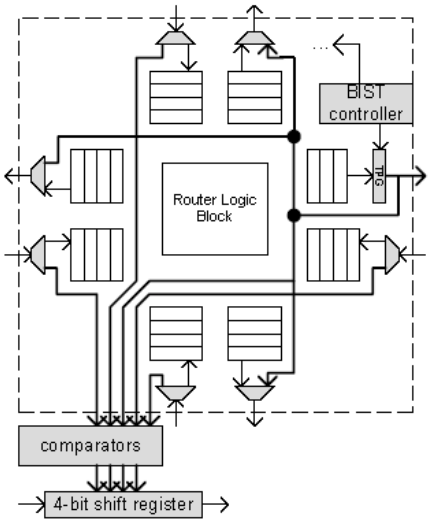

Figure 3. Hardware BIST Embedded In A Switched Network With A Mesh Topology Using This Output Buffer**.**

Four-port switch inputs are received and compared to the expected responses are sent to the trimmer. Responses are expected by the test data TPG Production and output ports simultaneously and also to analyze the responses received to the trimmer is in. In this strategy, the need to use a generator testing and analyzing the results separately for each link in the [12] Is used, it is not. It's just a structure TPG Each switch is needed, which results in a low area overhead. In order to identify the forms, the input of a comparator is needed for each link. Thus the switch quad comparator is required. The comparison of the responses received the link Compared with the corresponding responses expected and if there is a bug in the link, the corresponding flag in the shift register pass / fail Four-bit value '1' Be seated. Registers pass / fail All switches connected in series and a navigation route for transmission of test results form the object is outside the chip.

5. CLOCK FOR PARALLEL ANALYSIS OF EXPERIMENTS

In today's technologies, by reducing the size of transistors, the clock frequency is increased. The length of the wires is not decreased proportionally, because one end to the other end connected to the chip. The chip size larger, synchronous clock distribution across a chip becomes more difficult. On the other hand, most investigators are trying to skew Clack Clack improve with new methods of distribution. Since The mesh network topology has a regular structure Hess fast

and switches to communicate with one another at regular intervals, it is possible instead to skew Against the clock, take advantage of it. In [18] new method of distributing a clock-like - simultaneously (Quasi-synchronous) Suggested that a synchronous clock signal with the same frequency but with a constant phase difference will be distributed across the network with a mesh topology. In this way, the clock chip is divided into areas of the arrival time so that the clock signal (skew Clock) between two adjacent area equal clock + 1Td Is. Buffered clock signal can be entered directly from the entrance point to the nearest regions of clock distribution chip. Once the clock signal is closest to the back buffer and injected into the local clock. The clock signal Within a chip in one direction (horizontally in Figure 4) buffer, and again in the other direction (vertical) branches and carried. The methods used in this paper, a switching network with mesh topology test answers links connected to the input port and the expected responses are compared. We assume that the clock distribution strategy based on the distribution of quasi - As the clock.

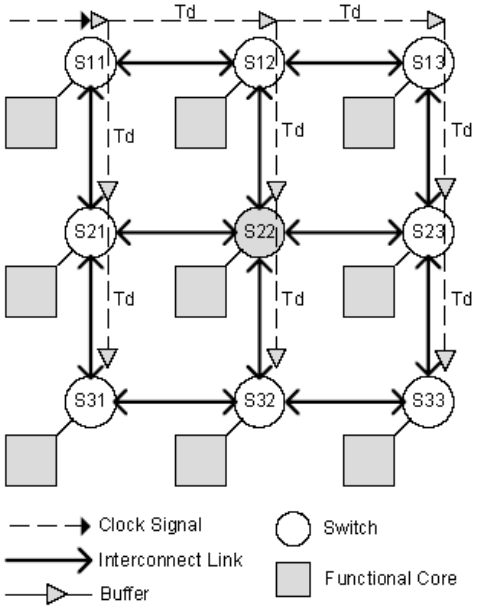

Figure 4. Distribution of the clock signal based on the quasi - simultaneously - different skew Between any two adjacent clock against the clock + 1Td Is.

According to Figure 4, the links arrow indicates that the link will need to be tested in two different directions and test all links are done in parallel. Since The strategy clock distribution, clock signal with a phase difference of each switch ± 1Td Adjacent to the switch receives for analysis of test responses in a correct way, it is required that a technique used to test the response with an expected response comparable to that of the corresponding. The technique we have an example of a Guggenheim. Switched to a (2,2) In Figure 4 Consider. The switch to four adjacent switch: switch (1,2) (Northern switch), switch (2,3) (Switches west), switch (3,2) (South switches) and switches (2,1) (Eastern switch) is connected. Our four-way incoming links to the switches to switch (2,2) Are connected, respectively, We markings. Switching the clock signal with a phase difference + 1Td Switch to (2,1) And (1,2) And the phase difference -1Td Switch to (2,3) And (3,2) Found in it. Upon receiving the switching signal, TPG Built-in test data generation and output ports connected to test links and sends them at the same time, data generated as compared to the expected Indicators for analyzing the responses received from the input links in. Since The links between the switches are tardy in sending data (usually the size of a clock cycle - for more info [19] See below), so the switch (2,2) Response test And Delayed + 1Td Are received at the same time, the expected responses in the switch (2,2) Production and thus comparison is done correctly. For switch (2,2) Clock signal with a phase difference + 1Td Switch to (1,2) And (2,1) Receives. The problem comes when you switch (2,2) Responses to the test And Receive. Since the switch (2,2) Clock signal with a phase difference -1Td Switch to

(2,3) And (3,2) Receive, and also a delay of + 1Td There is a link in the transmission of data, so the switch (2,2) Responses to the test Delayed + 2Td Receives. So to compensate for this delay and do a true comparison, you need to register the expected response delay + 2Td Switch is in. In reaching this goal, we use the property FIFO We use a switch buffer. We can take the word of a buffer to maintain the property. FIFO They compensate for the delay + 2Td We use them to line up - delays have named. Once TPG Test data generated, the data in the first word of the line - delays expected as a response to the responses received from And Stored. When the next clock signal (after + 1Td), Test data to the next word line - delays shifted and new test data to be replaced. Next clock signal causes the test data (expected response) to the receptors for Are intended to be made and compared after delay + 1Td + 1Td = + 2Td Done properly.

6. EVALUATION RESULTS

Our built-in test proposed in this paper for the three networks of different sizes in terms of area overhead and test application time were examined. The number of clock needed to be tested under simulated environment of network-level VHDL Is obtained. The simulation mechanism proposed experiment on a PC With 1GHz Processor Intel With 1G Memory DRAM Has been implemented. We assume that the link delay is equal to one clock cycle each link width of 64 bits. Table 4, the amount of time needed to test the communication links of the three networks with mesh topology. The results show that the Implementation of the proposed test method is significantly lower in the microsecond range. In terms of area overhead, using a buffer of each switch is attempting to contrive TPG Within each switch, the minimum area overhead is achieved. In [12] Writers overhead area-wide control (Global Test Controller-GTC) Have been evaluated, but our area overhead BIST Point - to - point them to compare the proposed method with an area overhead BIST Former conductor estimate and check the paper. Since the [12] A pair of blocks TGD / TED Respectively at the transmitter and receiver each link has been placed, and on behalf of each link should be tested in two opposite directions, the four pairs TDG / TED Each switch is required. Based on the results reported in [12] We have an area overhead of the method BIST Point - to - point proposal was developed from 2404 We evaluate gate, while our method 1121 Gate in detail in Table 5 have been reported. On the other hand, the application of this technique to evaluate the impact of context switches buffers to reduce the area overhead, we hold that a network packet switching SOCIN [24] Is the basis for their comparison made. Table 6 overhead area BIST Than the proposed SOCIN Various sizes show. Since the technique BIST The load imposed on the system, and this is an area that is undeniable, but the strategy BIST Proposed in this buffer using network switches with mesh topology, we try to minimize network overhead incurred the area. On the other hand it is very important that the area overhead structure BIST Decreases with increasing depth buffers, because TPG Only the first word of the buffer is built. On the other hand, compared with the number of gates in a switched network with a mesh topology (about 30,000 gates, as in [14], [20] And [21] Reported) area overhead of our implementation mechanism proposed experiment is acceptable. Therefore, the proposed method is useful in complex network implementations.

Table 4. From the time of its application for the proposed testing strategy.

Test time (Clock cycles)	Mesh network topology size
428	
444	
500	

Table 5. The area overhead of our proposed method in comparison with the same method [12].

		4 TPG / TDEs per switch (#gates)	TDE (#gates)	TDG (#gates)	point-to-point BIST method proposed in [12]
		2404	314	287	
Total (#gates)	4-bit Pass / fail shift register (#gates)	4 comparators per switch (#gates)	Controller (#gates)	TPG by reusing buffer (#gates)	our BIST method
1121	68	620	81	352	

Table 6. Overhead area BIST Compared to the size of the proposed SOCIN.

Area with proposed BIST without reusing buffer (#gates)	Area with proposed BIST By reusing buffer (#gates)	Original area (#gats)	The link width (Bit)	Mesh network topology size
59085 (42%)	51741 (24%)	41445	16	
104720 (42%)	91664 (24%)	73680	16	
163,625 (42%)	143,225 (24%)	115125	16	

7. CONCLUSION

Speed functional test chip for the effects of hearing loss by an external tester is costly. Compared with external tester, built-in self-test is a very good way to test the speed of the chip functional effects of the hearing, because this dependence is very low external tester. Therefore, in this paper, a low-cost method for testing communication links between switches mesh network topology is proposed. By using this buffer with mesh topology network switches, test pattern generator built in the first word of the buffer we made it possible for all connections between switches to be tested in parallel. Simulation results show that the proposed BIST strategy has a very low test application time and area overhead is lower compared to the same procedures as well. However, this method is not related to the control and routing algorithms can be applied to a class of large number of network implementations.

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