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Design and Modeling of Solar Photovoltaic System Using Seven-Level Packed U-Cell (PUC) Multilevel Inverter and Zeta Converter for Off-Grid Application in India

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ABSTRACT

In the present study, standalone operation of the solar photovoltaic system with storage is evaluated with the recently introduced seven-level packed U-cell (PUC) multilevel inverter. Zeta converter is used to regulate the output voltage of the photovoltaic (PV) array with the help of the MPPT algorithm. Level-shifted modulation scheme is applied for the PUC inverter. The standalone operation is taken into consideration keeping in view the application/penetration of the solar PV system in remote areas. The Ministry of New and Renewable Energy (MNRE), Government of India has set up the plan to establish the standalone solar PV system for off-grid application in the regions to meet the power requirement of those communities and regions that are difficult to connect with the grid. The climatic condition in the central and western parts of India is conductive for solar PV generation. In contrast to the other well-known inverter topologies, such as neutral point clamped, flying level capacitors, and cascaded H-bridge, among others, PUC inverter requires the least number of switches and capacitors for the same output levels. The system is modeled in the MATLAB®/Simulink using the Waaree Energies WSM-315 modules to supply a load of 2 kW. To optimize the solar PV-based system, incremental conductance optimization technique is used.
Keywords: Multilevel inverter, packed U-cell inverter, solar PV array, incremental conductance technique

Introduction

Energy is one of the most fundamental parts of our universe. The use of energy is essential for our lives especially electrical energy. All electronic devices require electricity for power. Among the renewable energy sources, solar energy is easily available at different locations in comparison with geothermal and wind energy that are too site specific. To meet the required demand of electrical energy and the environmental challenges (increasing pollution), solar-based energy system is a viable option [1]. The widespread applications of the solar photovoltaic (PV) array in off-grid application are due to its simplicity in installation and operation [2]. The recent focus of researchers worldwide is to optimize the three following things in a solar system: (1) increasing the efficiency of the system, (2) reducing the installation cost, and (3) increasing the reliability. The topology used in the present study is meeting all the above three mentioned requirements (efficiency, reliability, and overall cost).

Multilevel inverters are used to achieve high power from medium voltage source. They are emerging because of their advantages compared with conventional inverters. Multilevel output is achieved by synthesizing various voltage levels [3]. Although they do not provide the pure sinusoidal output voltage, there is a considerable improvement in total harmonic distortion (THD) compared with its two-level counterpart, thus mitigating the power quality issues [4]. The IEEE standard 519-2014 "Compliances, updates, solutions and case studies" put a limit on harmonics voltage and current at the point of common coupling. This standard fixes the harmonics limit of 5% for current and 8% for voltage waveforms [5].

Packed U-cell (PUC) inverters have a number of advantages in comparison with traditional multilevel inverters, such as low device count [6], reduced complexity in control, and overall good power quality [7]. PUC multilevel inverters were introduced in 2008 by the deduction of CHB in which two switches have been removed and two cells are connected directly

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[8]. PUC seven-level inverter only needs one DC source and one capacitor with reduced structure as compared with other multilevel inverters for the same number of levels in output voltage [9].

The complete model of the system obtained in the present study is shown in Figure 1. It consists of PV modules, such as a power source, and the MPP tracking algorithm is applied on zeta converter and PUC converter. The complete system is modeled and analyzed. For the modulation of PUC inverter, two modulation schemes (belonging to the family of level-shifted modulation), namely, (1) in-phase disposition pulse width modulation (IPD-PWM) and (2) phase opposition disposition PWM (POD-PWM) have been applied with intelligent switching combination of power converters.

A comparative analysis of the above-mentioned modulation schemes applied on the PUC-7 inverter is presented, and a comparison is done based on the power quality of output. The comparison done in the present study is based on the real parameters of the system.

The present study presents the solar PV system by using the recently introduced PUC inverter interfacing with the zeta converter, working as boost converter. A PUC inverter-based PV system using zeta converter is still unexplored. In the present study, a designing of the PV system with zeta converter is designed, modeled, and simulated in MATLAB®/Simulink environment.

Solar modules from the Waaree Energies WSM-315 have been obtained that are easily available in India and have the highest power rating among all available solar PV panel. The simulation is performed at a solar irradiation of 900 W/m^2 and at a temperature of 28 °C, which are an average insolation and temperature value in the northern region of India.

The study is organized as follows. Section 2 explains the design of the solar array and zeta converter. Section 3 shows the operation of the PUC inverter. Section 4 discusses the modeling of the PV cell and MPPT technique. Section 5 presents the theoretical analysis of carrier-based PWM schemes. Section 6 shows the experimental validation of the inverter system. Finally, Section 7 presents the conclusion.

Design of the system

The design of the system consists of the design of the PV array, design of the zeta converter, and PUC inverter operation.

Design of the PV array

A typical house has a load of 2 kW; hence, the system is modeled for the 2 kW load. The Waaree Energies-315 solar PV module has been selected. The specification of the Waaree Energies WSM-315 module of PV cell is given in Table 1.

The number of modules connected in series/parallel can be calculated by defining the voltage of the solar PV array at MPP under standard test condition as V_{mmp} =140 V

$$I_{mpp} = \frac{P_{mpp}}{V_{mpp}} = \frac{2000}{140} = 14.28\ A. \quad (1)$$

The number of modules in series required is calculated in Eq. (2):

$$N_S = \frac{P_{mpp}}{V_{mpp}} = \frac{140}{35} = 4 \quad (2)$$

Table 1. Specification of the Waaree Energies WSM-315 module PV cell

Parameters	Values
Peak power P_m	315 W
Voltage at MPP	35 V
Short circuit current	9.77 A
Current at MPP	9.0 A
No. of cell connected	72
Shunt resistance R_{sh}	313.3991 Ω
Series resistance R_{se}	0.39385 Ω

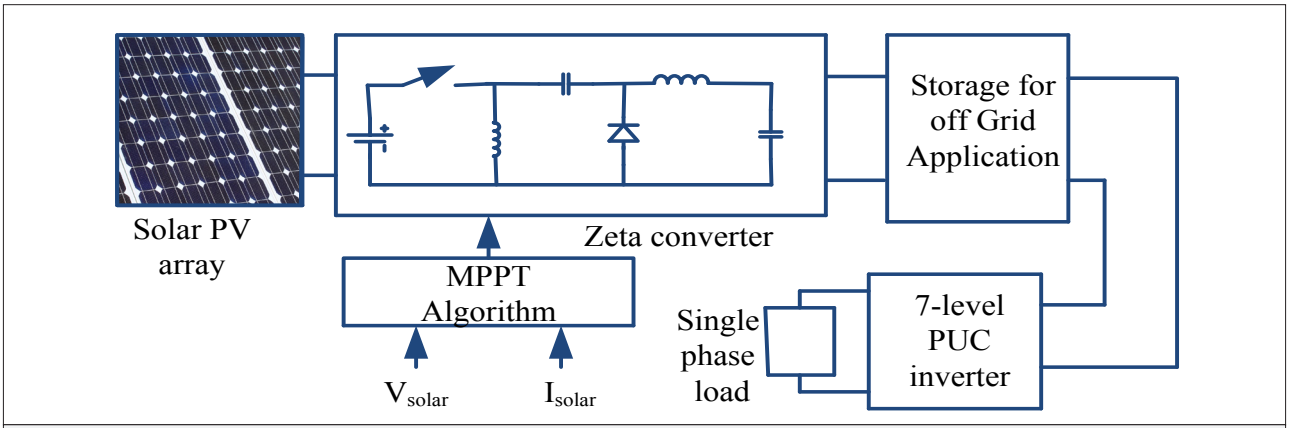

Figure 1. Block diagram of single-phase solar PV-based PUC inverter

The number of modules parallel required is calculated in Eq. (3):

$$N_P = \frac{I_{mpp}}{I_m} = \frac{14.28}{9} \cong 2 \quad (3)$$

Therefore, the solar PV array has two parallel paths with each path consisting of four modules.

Design of the zeta converter

Zeta converter is shown in Figure 3. It belongs to the family of buck-boost converter, but it draws continuous current in contrast to the buck-boost converter. The continuous current is because of the output inductance that ensures ripple-free current. With respect to component count, it comprises the same number of components as Cuk converter [10]. Moreover, in contrast to the Cuk converter, it operates in non-inverting mode means, and output voltage has the same polarity as input in contrast to the buck-boost converter; hence, the problem of negative voltage sensing is eliminated [11]. Different buck-boost converter configurations and their application to the inverter operation are reported in the literature. The reasons for using the zeta converter are its advantage over other converters as follows:

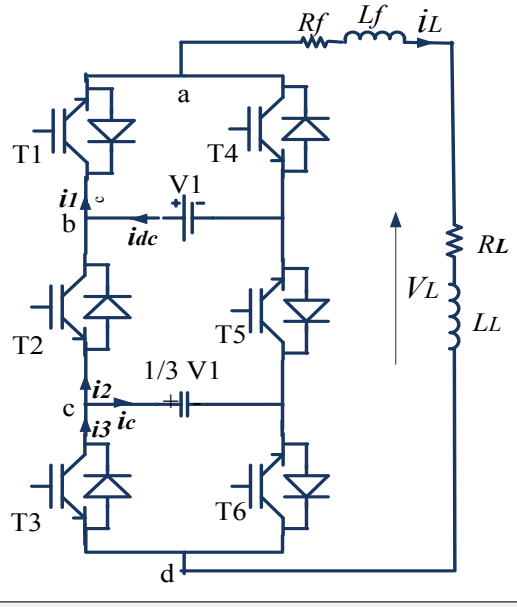

Figure 2. Packed U-Cell converter topology

1. A conventional buck-boost converter has a low component count. However, the output current is pulsating in nature that increases the ripple in output voltage.
2. SEPIC also depicts a pulsating output current. As the output stage of the power supply is very sensitive, this pulsating current is not desirable.
3. The flyback converter suffers from leakage inductance problem that imposes a limit on its rating.

To eliminate these issues, a zeta converter is employed as a buck-boost converter in the present study. It provides a continuous output current with a low ripple output voltage along with a high-level performance that is highly recommendable for solar PV applications. Its design includes the calculations of various components, such as L_1, L_2 and C_1. It always operates in CCM to reduce the stress on its elements

The design of the zeta converter is done by first estimating the duty cycle D as given by Eq. (4) [12]

$$D = \frac{V_{dc}}{V_{dc}+V_{mpp}} = \frac{250}{250+140} = 0.64 \quad (4)$$

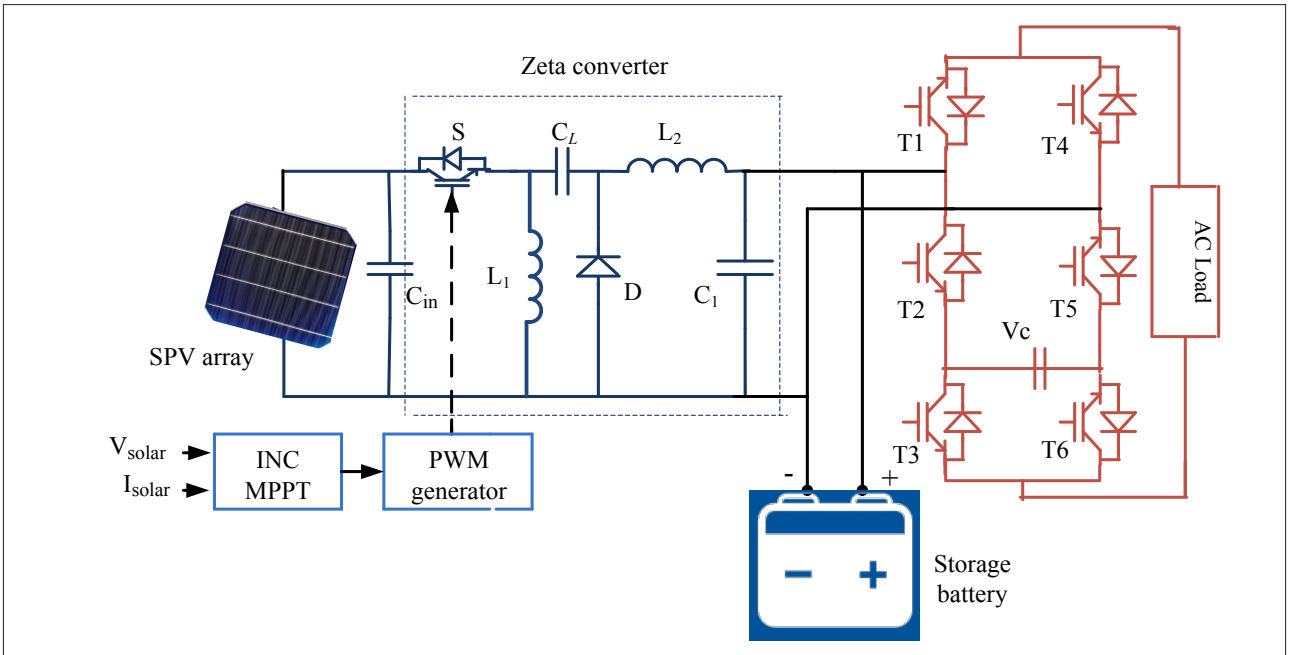

Figure 3. Proposed solar PV with zeta converter topology

Table 2. Switching table for PUC-7 inverter

States	Voltage	T1	T2	T3	T4	T5	T6
0	Va	1	0	0	0	1	1
1	Va–Vc	1	0	1	0	1	0
2	Vc	1	1	0	0	0	1
3	0	1	1	1	0	0	0
4	0	0	0	0	1	1	1
5	–Va	0	1	1	1	0	0
6	Vc–Va	0	1	0	1	0	1
7	–Vc	0	0	1	1	1	0

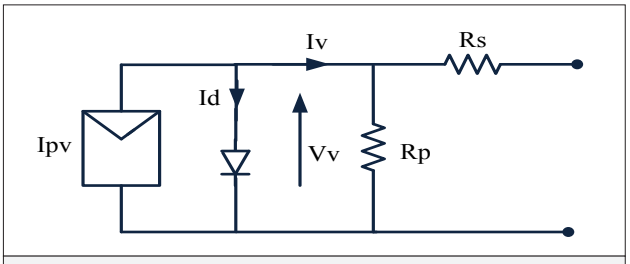

Figure 4. Single PV cell model

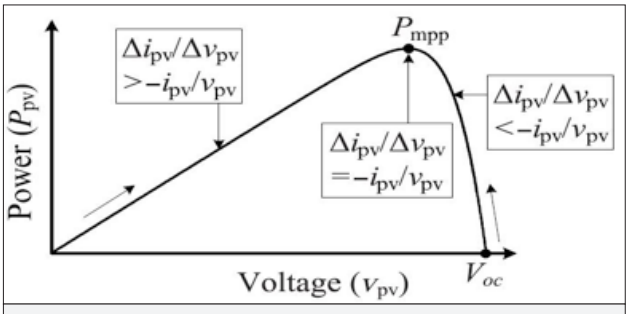

Figure 5. Illustration of the INC MPPT technique

Where V_{dc} is an average output voltage of the zeta converter equal to the rating of the load connected. The average value of the current flowing through the DC link of the inverter is given by [12]:

$$I_{dc} = \frac{P_{mpp}}{V_{dc}} = \frac{2000}{250} = 8 \text{ A.}$$

Then L_1, L_2 are C_1 calculated in Eqs. (5), (6), and (7):

$$L_1 = \frac{D \times V_{mpp}}{f_{sw} \times \Delta I_{L1}} = \frac{0.64 \times 140}{5000 \times 14.28 \times 0.06} = 20.9\ mH \quad (5)$$

$$L_2 = \frac{(1-D) \times V_{dc}}{f_{sw} \times \Delta I_{L2}} = \frac{(1-0.64) \times 250}{5000 \times 8 \times 0.06} = 37.5\ mH \quad (6)$$

$$C_1 = \frac{D \times I_{dc}}{f_{sw} \times \Delta V_{C1}} = \frac{0.64 \times 8}{5000 \times 250 \times 0.1} = 41\ \mu F \quad (7)$$

Where f_{sw} is the operating frequency of IGBT used in the zeta converter, ΔI_{L1} is the value of allowed ripple in the current through L_1, is ΔI_{L2} the value of allowed ripple in the current through L_2, and $I_{L1} = I_{mmp}$ and $I_{L2} = I_{dc}$.

Operation of the PUC inverter

The circuit topology for seven-level PUC inverter is shown in Figure 2. For seven-level operation, the capacitor voltage has to be maintained at one-third of the DC link voltage. The seven-level output can be obtained by switching scheme as shown in Table 2. The relationship between number of voltage level and number of capacitor is given by Eq. (8) [13,14]:

$$N_V = 2^{Nc+2} - 1 \quad (8)$$

Where is N_v the number of output voltage levels, and N_c is the number of capacitor used.

With reference to Figure 2, the switching function of the PUC inverter is defined by Eq. (9), and inverter output is defined by Eq. (10)

$$\left.\begin{aligned} T_i &= 0 \quad if\ T_i\ is\ off \\ &= 1 \quad if\ T_i\ is\ on \end{aligned}\right\} \quad (9)$$

$$V_{ad} = V_{ab} + V_{bc} + V_{cd} \quad (10)$$

Based on the switching table shown in Table 2, each voltage can be expressed as

$$V_{ab} = V_1(T_1 - 1) \quad (11)$$

$$V_{bc} = (V_1 - V_2)(1 - T_2) \quad (12)$$

$$V_{cd} = V_2(1 - T_3) \quad (13)$$

Hence, by combining Eqs. (11), (12), and (13), Eq. (10) can be presented as:

$$I_{pv} = I_{ph} - I_d = I_{ph} - I_s\left(exp\left(\frac{qV_V}{akT}\right) - 1\right) \quad (14)$$

Modeling of the solar PV array and INC MPP tracker

The modeling of the single-cell model of the PV cell is shown in Figure 4. The PV cell current is given by Eq. (15) [12,16]:

$$I_{pv} = I_{ph} - I_d = I_{ph} - I_s\left(exp\left(\frac{qV_V}{akT}\right) - 1\right) \quad (15)$$

For N_s and N_p, the number of connected cells in series and parallel, respectively, Eq. (15) is modified and given as Eq. (16):

$$I = N_p I_{ph} - N_p I_s\left(exp\left(\frac{q(V + R_s I)}{aN_s kT}\right) - 1\right) - \frac{V + R_s I}{R_p} \quad (16)$$

Where I_{ph} is the photocell current that only depends on solar insolation, I_s is the diode reverse saturation current, and R_s and R_p are the total series and parallel resistance of the PV array.

Maximum power point is defined by the point on the power curve at which $\frac{dP_{Pv}}{dV} = 0$, the slope $\frac{dP_{pv}}{dV}$ is positive or negative on the left or right of this point, and the maximum point is calculated by Eq. (17)

$$\frac{dP_{Pv}}{dV} \cong I + V\frac{\Delta I}{\Delta V} \quad (17)$$

Incremental conductance (INC) MPPT algorithm has a relationship between instantaneous conductance $\frac{I_{pv}}{V_{pv}}$ and ICC $\frac{\Delta I_{pv}}{\Delta V_{pv}}$ given by Eq. (18) and shown in Figure 5.

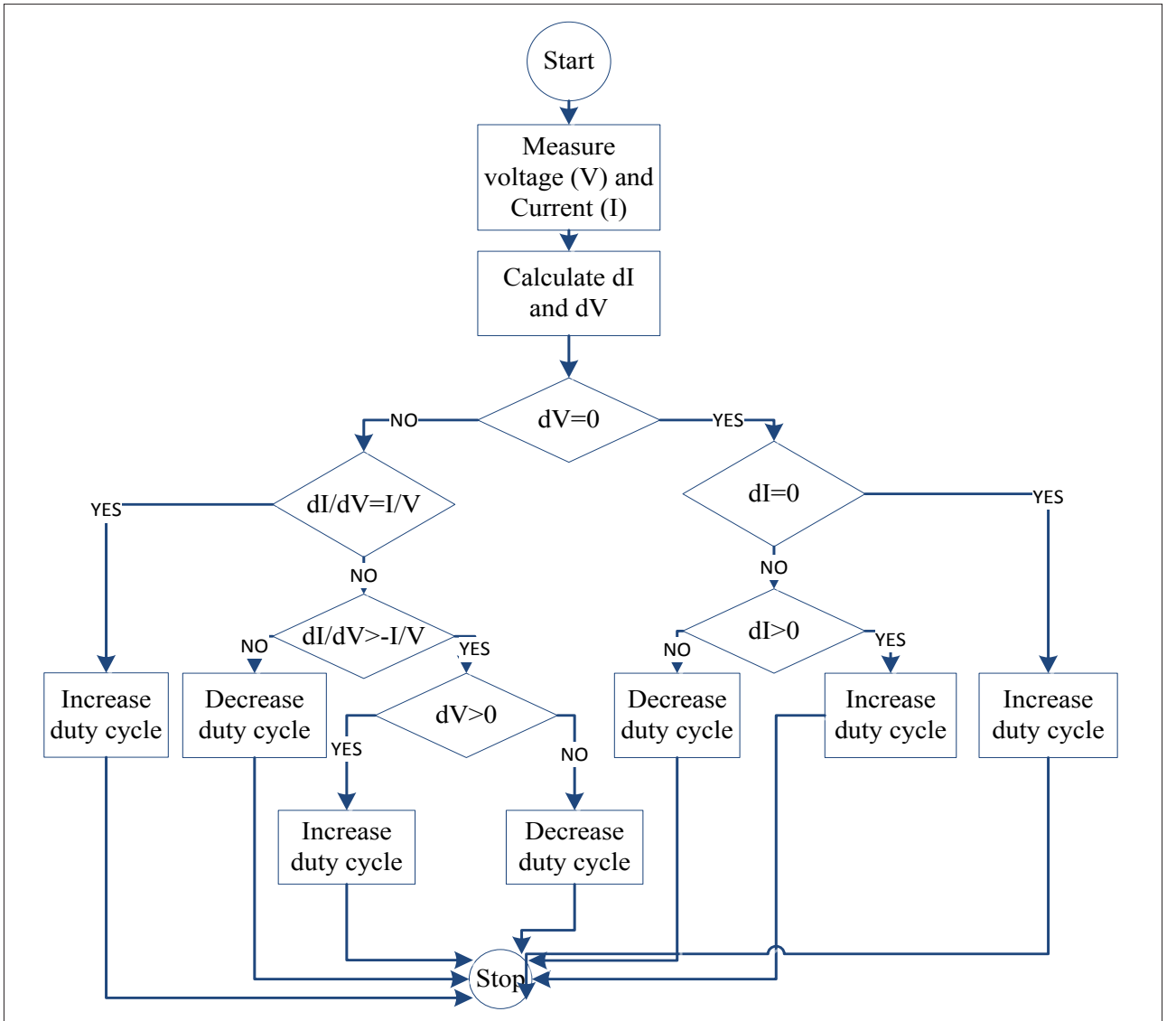

Figure 6. Flowchart of incremental conductance algorithm

$$\left.\begin{array}{l} \frac{\Delta I_{pv}}{\Delta V_{pv}} = -\frac{I_{pv}}{V_{pv}} \text{ at MPP point} \\ \frac{\Delta I_{pv}}{\Delta V_{pv}} > -\frac{I_{pv}}{V_{pv}} \text{ at left of MPP point} \\ \frac{\Delta I_{pv}}{\Delta V_{pv}} < -\frac{I_{pv}}{V_{pv}} \text{ at right of MPP point.} \end{array}\right\} \quad (18)$$

The error between INC and instantaneous conductance must be reduced to zero to enhance the tracking dynamics [17]. The flowchart of the INC algorithm is shown in Figure 6.

Simulation and analysis of the proposed system

Solar PV array and storage system

The I–V and P–V characteristics of the Waaree energy solar PV module are shown in Figure 7. The solar PV cell is simulated for an average insolation of 900 W/m^2 with a temperature of 28 °C. The battery will provide power when solar insolation is not present and it gets charged when extra power is available. The battery also enhances the dynamic stability of the inverter and improves the response [18]. Figure 8 shows the battery discharging characteristics. The specification of the battery is 250 V, 15 Ah. The open circuit voltage is calculated from its nonlinear Eq. (19) based on the actual state of charge. Actual battery voltage that depends on the charge/discharge current is given by Eqs. (20)–(22) [19].

$$E_{oc} = E_o - k\frac{Q}{Q-it} + Ae^{-Bit} \quad (19)$$

$$E_{act} = E_{oc} - \frac{Qk}{Q-it}.it - \frac{Qk}{Q-it}.i^* + Ae^{-Bit} \quad (20)$$

$$E_{act} = E_{oc} - \frac{Qk}{Q-it}.it - \frac{Qk}{it+0.1Q}.i^* + Ae^{-Bit} \quad (21)$$

$$Q = it = \int idt \quad (22)$$

Where E_{oc} is the open circuit battery voltage, E_o is the nominal voltage of the battery, and E_{act} is the actual voltage of the battery at dis-

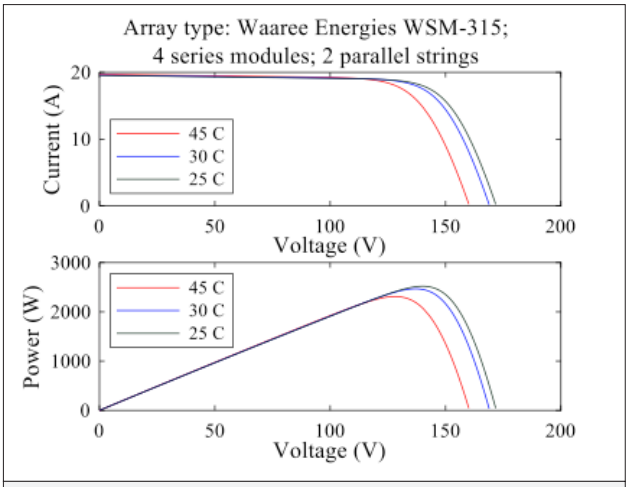

Figure 7. I–V and P–V characteristics of PV array.

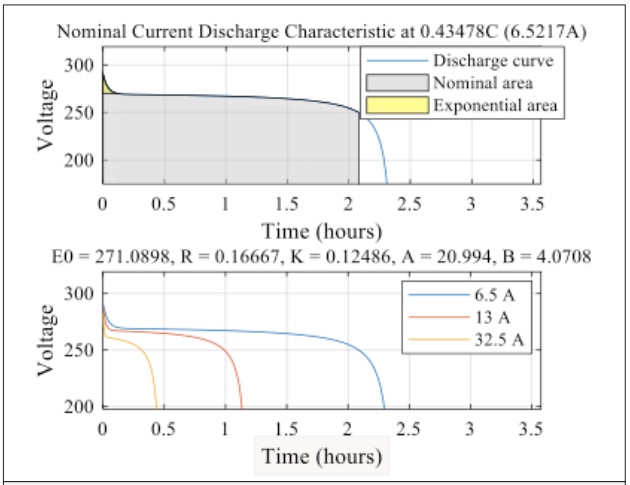

Figure 8. Battery discharging characteristics.

tinct *C* rate. *Q* indicates the maximum battery capacity in Ah. *K* indicates the polarization constant. i^* is the filtered battery current. A and B indicate the exponential voltage and capacity, respectively.

Zeta converter and MPPT performance

Zeta converter shown in Figure 3, is connected directly to the solar PV array. It boosts the voltage to a usable value and also charges the battery when more power is generated by solar array. Switching signal for zeta converter is obtained from the INC algorithm block shown in Figure 3.

Figure 9 shows the duty ratio and corresponding output voltage of the zeta converter as shown in Figure 10. From Figure 10, it can be observed that due to variation in the load condition at *t*=0.2 s, the graph fluctuates and attains a new stable state.

Modulation schemes and control

The system discussed so far is modeled and simulated in MATLAB®/Simulink by using IPD- and POD-PWM schemes.

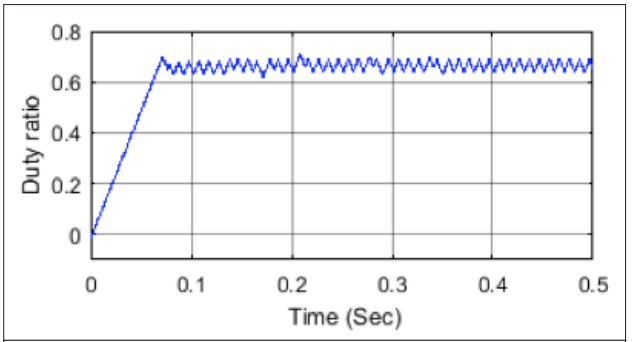

Figure 9. Duty ratio

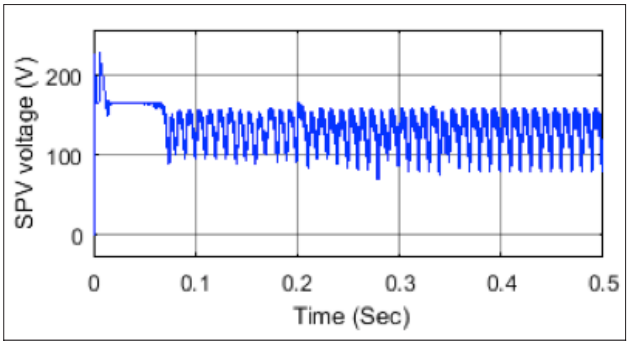

Figure 10. Zeta converter output

The phase voltage of two-level voltage source inverter with PWM and triangular modulating signal can be described as [20]:

$$F(t) = \frac{MV}{2}\cos(\omega_F t) + \frac{2V}{\pi}\sum_{m=1}^{\infty} J_o(mM\frac{\pi}{2})\sin(m\frac{\pi}{2}) .\cos(m\omega_c t) + \frac{2V}{\pi}\sum_{m=1}^{\infty}\sum_{n=1}^{\pm\infty}\frac{J_n\frac{mM\pi}{2}}{m} .sin\left((m+n)\frac{\pi}{2}\right)cos(m\omega_c + n\omega_F t) \quad (23)$$

Where *M*=modulation index, ω_c=freq. of carrier (rad/s), ω_F= =freq. of fundamental (reference), *V*=supply voltage (V), and J_o, J_n =Bessel function of the first kind.

Eq. (23) comprises three terms:

(a) The first term gives the amplitude of the fundamental component that is proportional to modulation index *M*.

(b) The second term shows the amplitude of the harmonics content at the carrier and multiple of the carrier frequency.

(c) The third term gives the amplitude of the harmonics at side band.

Level-shifted IPD-PWM multicarrier schemes for PUC inverter are shown in Figure 11. Figure 12 shows the POD-PWM scheme. The frequency of carrier wave is obtained as 5000 Hz.

For seven-level output, capacitor voltage has to be maintained at one-third of the DC link voltage [21]. A PI controller is used for this purpose. The controller block diagram is shown in Figure 13. The PI controller reduces the error and improves the dynamic stability of the inverter [22].

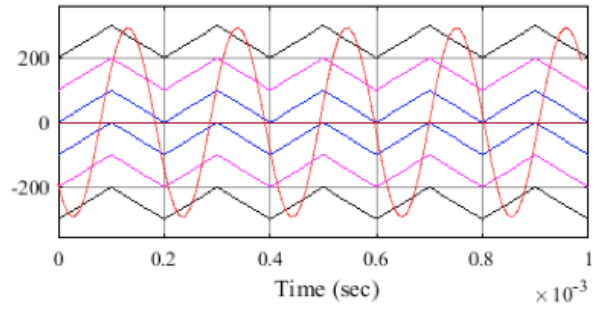

Figure 11. IPD-PWM scheme for PUC-7 inverter

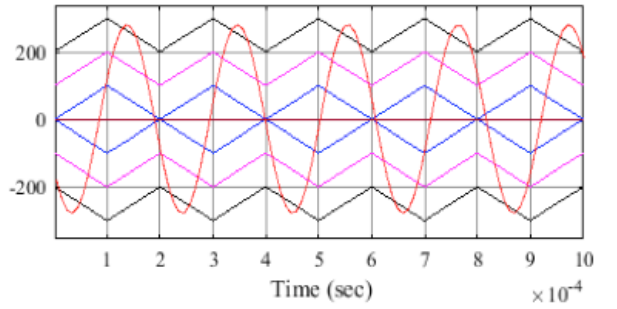

Figure 12. POD-PWM scheme for PUC inverter

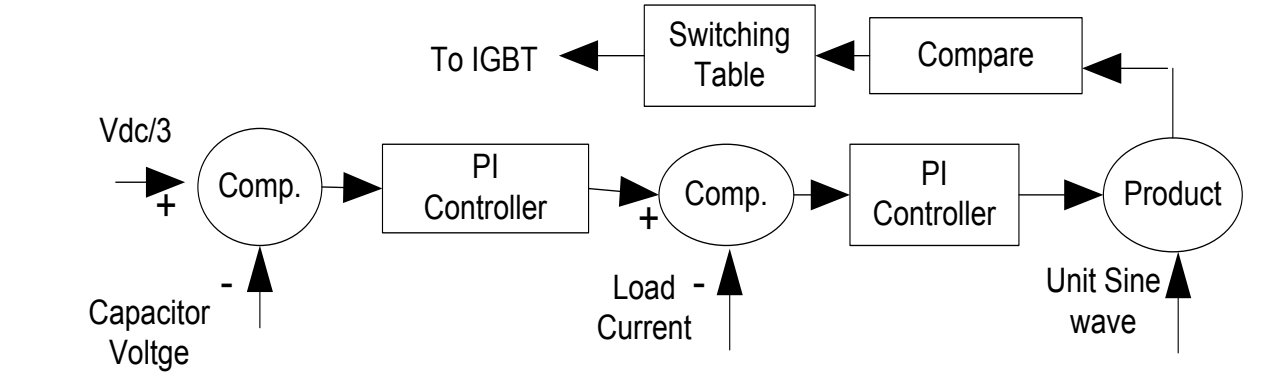

Figure 13. Voltage balancing controller

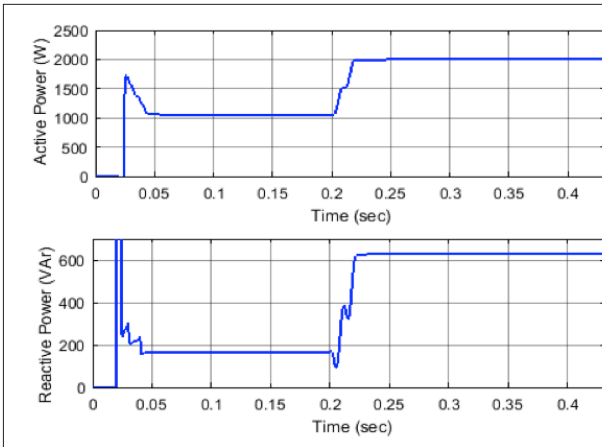

Figure 14. Active and reactive powers of inverter

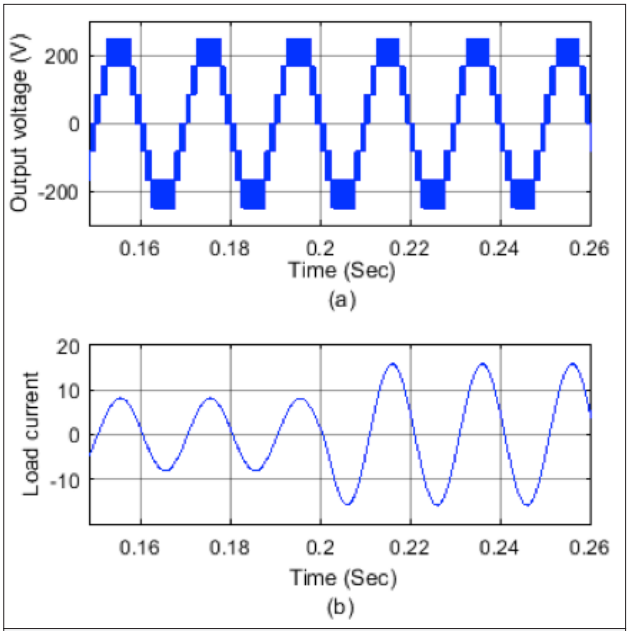

Figure 15. a, b. (a) Output voltage (a), load current in IPD-PWM (b)

The simulated capacity of the inverter with respect to active power and reactive power is shown in Figure 14. The model is simulated for 2 kW load that can be seen from Figure 14.

Performance under the IPD-PWM schemes

Figure 15 shows the output voltage and current waveform of the PUC inverter, at time *t*=0.2 s. The load is doubled (by connecting additional 40 Ω resistive load in parallel) resulting in an increase of load current as shown in Figure 15. Initially, the current is 5.8 A and at *t*=0.2 s. It becomes 11.33 A rms. The THD in the load current is found to be 0.5% at steady state. The FFT

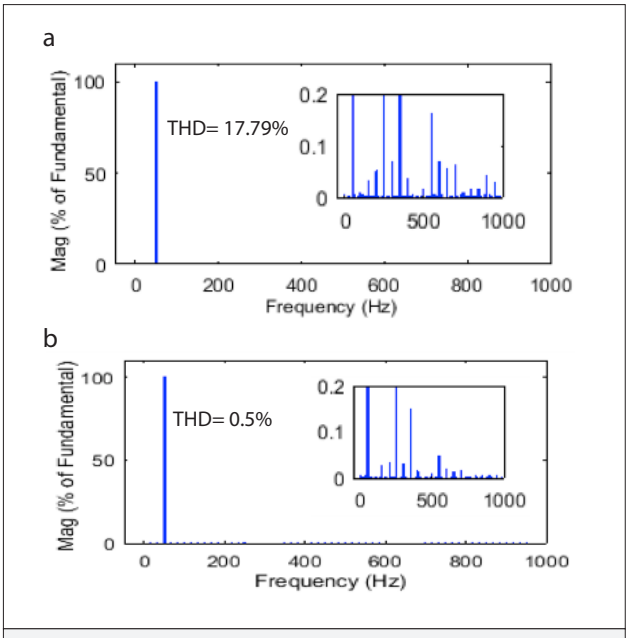

Figure 16. a, b. FFT window for (a) voltage and IPD-PWM scheme (b)

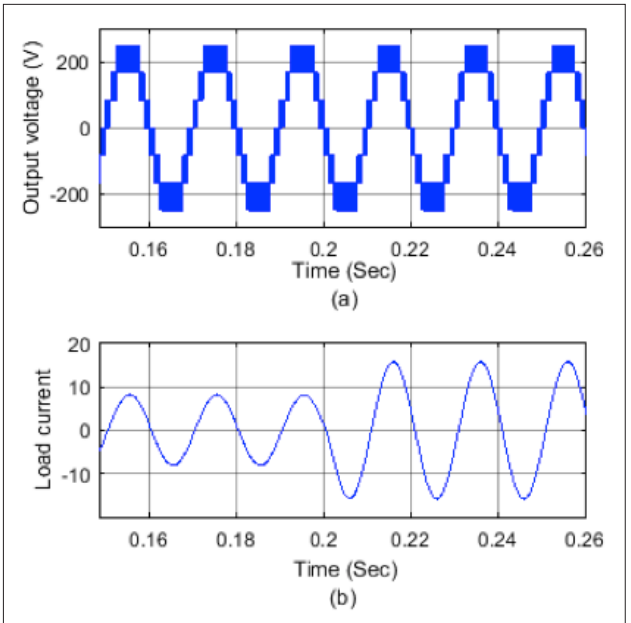

Figure 17. a, b. Voltage (a) and load current in the POD-PWM scheme (b)

analysis of the voltage waveform shows that THD is 17.79% and rms value is 178.1 V.

Capacitor voltage balancing

Figure 13 shows the detailed block diagram of controller used for capacitor voltage balancing (at one-third of the main DC bus voltage) to obtain the seven level at output. Figure 19 shows the capacitor voltage waveform for the POD-PWM scheme. Capacitor voltage varies between 79 V and 87 V with

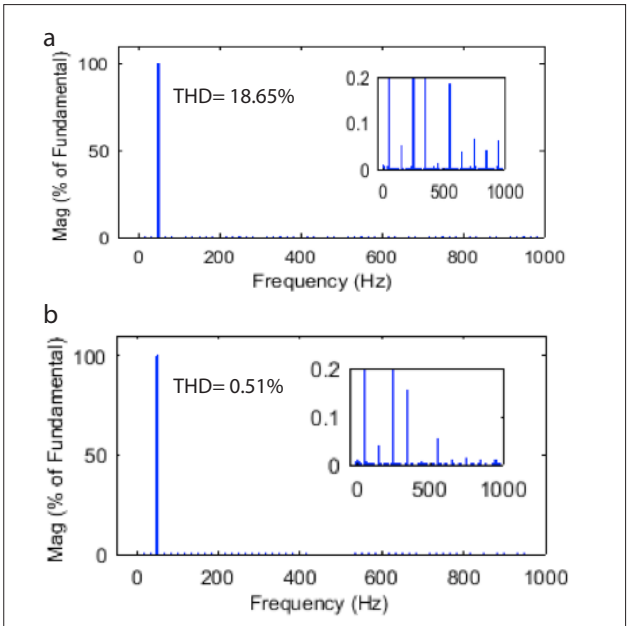

Figure 18. a, b. FFT window for voltage (a) and current in the POD-PWM scheme (b)

Table 3. Simulation parameters

Parameters	Rating
Capacitor	5000 µF
Load resistance	30 Ω
Load inductance	15 mH
Switching frequency	5000 Hz
Load change	20 Ω to 40 Ω at t=0.2 s

Table 4. FFT result for IPD- and POD-PWM schemes

Level-shifted PWM Schemes	*Parameters*	*THD %*
IPD-PWM scheme	Voltage	17.79
	Current	0.50
POD-PWM scheme	Voltage	18.65
	Current	0.51

an average value of 83 V (which is desired). It is unaffected with the load change, which is occurring at 0.2 s, showing the good dynamic performance of the controller.

Performance under the POD-PWM schemes

The POD-PWM scheme carrier waveform for PUC-7 inverter is shown in Figure 12. Reference signal is generated by the voltage balancing controller compared with these carrier signals to produce the switching signals. Figure 17 shows the output voltage and load current for the IPD-PWM scheme. This scheme is simulated for the same load as the IPD-PWM scheme. To analyze the transient behavior, load is changed from 20 Ω to 40 Ω at *t*=0.2 s as shown in Figure 17. FFT analysis of the voltage

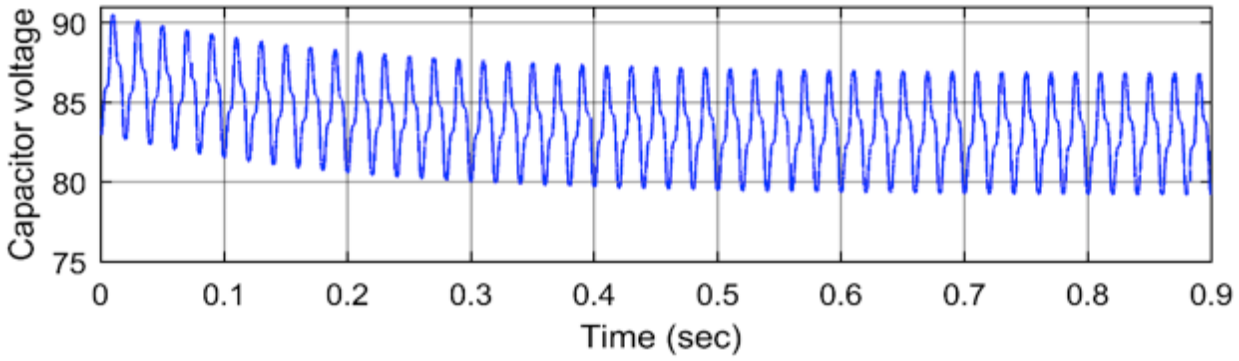

Figure 19. Capacitor voltage in the POD-PWM scheme

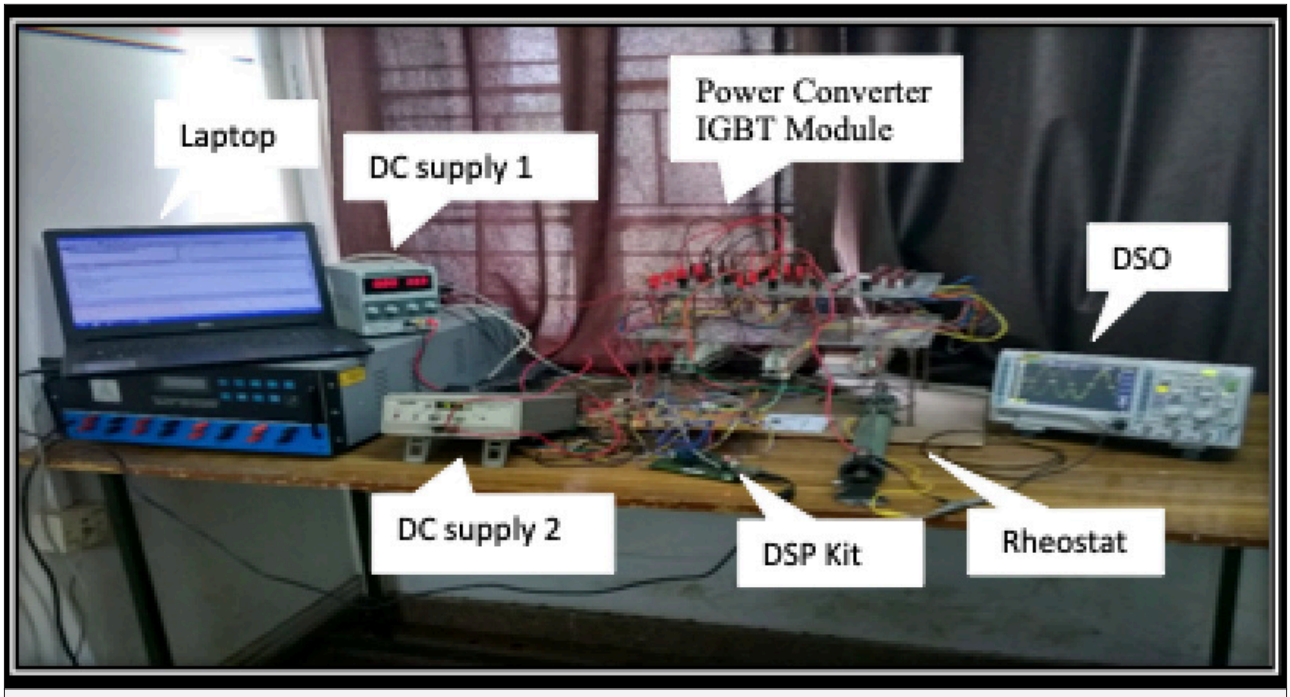

Figure 20. Experimental setup

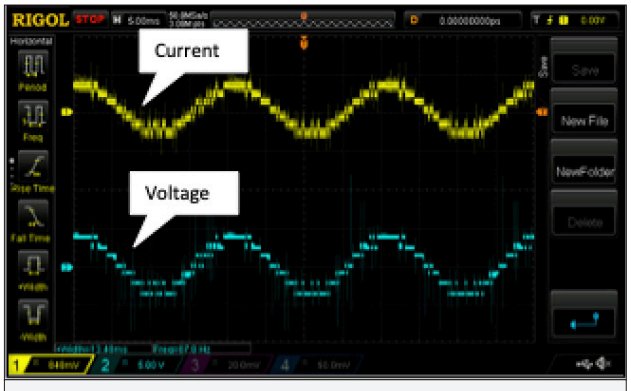

Figure 21. Output voltage and current on DSO of seven-level PUC inverter

Figure 22. Switching signals of PUC-7 level on DSO

waveform is presented in Figure 18. The THD in the voltage wave is found to be 18.65% with an rms value of 175.2 V. FFT window for load current is shown in Figure 18 with 0.51% THD,

Table 5. Parameters of the component used in the experiment

Parameters/Components	***Rating***
Two DC Voltage Supplies	0-15 V, 0-30 V
Fundamental frequency(f_o)	50 Hz
Switching frequency (f_s)	1 kHz
Rheostat	1.5 kΩ
Switches (S_1 to S_6)	SKM75GB063D (SEMIKRON)
Optocoupler	TLP 250 (TOSHIBA)
DSP	TMS320F28335(TI)
Sampling time	1μsec
Dead time	2μsec

and rms value is 11.4 A. Initially, when the load is not increasing, the current is 5.72 A.

Experimental validation

The hardware setup for the PUC multilevel inverter as shown in Figure 1 is presented in Figure 19. The laboratory prototype is fully fabricated in the laboratory. The developed prototype is of a general purpose, user interface, and can be used for the development of other converters, such as DC/DC, AC/DC, and multilevel converters, and so on. This laboratory prototype is used to implement the circuit presented in Figure 1, and the results are experimentally verified. Table 5 lists the parameters of the component used in the experiment. Figures 20 and 21 show the switching pulses required for seven level and the output voltage across the load and current through the load, respectively. Rheostats are used as a load.

Conclusion

The aim of the present study was to analyze and compare between two level-shifted modulation schemes applied on the solar PV-based seven-level PUC inverter interacting with zeta converter. The comparison is performed on the basis of power quality and some feature of zeta converter operation. Table 4 presents the power quality of the proposed system. Based on the simulation result, it is observed that IPD-PWM scheme has 17.79% THD in voltage and 0.50% in load current, whereas POD-PWM scheme has 18.65% THD in voltage and 0.51% in load current waveforms. Device switching frequency and device conduction period in case of IPD-PWM are different for each switch, and the rotation of the switching patters is more uniform as compared with the POD-PWM scheme. This is the reason of getting better performance under the IPD-PWM scheme. Simulation results suggest that the IPD-PWM scheme is favorable for application due to good power quality. The overall system is compact, has good dynamic response, is reliable, and has good power quality. It has the least number of device counts as compared with other conventional multilevel inverters. The topology is verified in MATLAB®/Simulink environment.

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References

1. U. Akram, M. Khalid, S. Shafiq, "Optimal sizing of a wind/solar/battery hybrid grid-connected microgrid system," IET Renew. Power Gener., vol. 12, no. 1, pp. 72-80, Jan. 2018. [CrossRef]
2. M. Nasir, S. Iqbal, H. A. Khan, "Optimal Planning and Design of Low-Voltage Low-Power Solar DC Microgrids," IEEE Trans. Power Syst., vol. 33, no. 3, pp. 2919-2928, May 2018. [CrossRef]
3. A. Sarwar, M. S. J. Asghar, "Multilevel converter topology for solar PV based grid-tie inverters," 2010 IEEE Int. Energy Conf. Exhib. Energy Con, pp. 501-506, 2010. [CrossRef]
4. J. Rodríguez, J. S. Lai, F. Z. Peng, "Multilevel inverters: A survey of topologies, controls, and applications," IEEE Trans. Ind. Electron., vol. 49, no. 4, pp. 724-738, 2002. [CrossRef]
5. J. Cheng, CEng, CEM, CEA, and CMVP, "IEEE Standard 519-2014," Schneider Electr., p. 50, 2014.
6. H. Vahedi, A. A. Shojaei, L. Dessaint, K. Al-haddad, "Reduced DC Link Voltage Active Power Filter Using Modified PUC5 Converter," IEEE Trans. Power Electron., vol. 33, no. 2, pp. 943-947, 2017. [CrossRef]
7. M. Tariq, M. T. Iqbal, M. Meraj, A. Iqbal, A. I. Maswood, C. Bharatiraja, "Design of a Proportional Resonant Controller for Packed U Cell 5 Level Inverter for Grid-Connected Applications," pp. 3-8, 2016. [CrossRef]
8. H. Vahedi, H. Y. Kanaan, K. Al-Haddad, "PUC converter review: Topology, control and applications," IECON 2015 - 41st Annu. Conf. IEEE Ind. Electron. Soc., pp. 4334-4339, 2015. [CrossRef]
9. H. Vahedi, K. Al-Haddad, "Real-time implementation of a seven-level packed U-cell inverter with a low-switching-frequency voltage regulator," IEEE Trans. Power Electron., vol. 31, no. 8, pp. 5967-5973, 2016. [CrossRef]
10. A. H. El Khateb, N. A. Rahim, S. Member, J. Selvaraj, B. W. Williams, "DC-to-DC Converter With Low Input Current Ripple for Maximum Photovoltaic Power Extraction," IEEE Trans. Ind. Electron., vol. 62, no. 4, pp. 2246-2256, 2015. [CrossRef]
11. S. Singh, B. Singh, G. Bhuvaneswari, V. Bist, "Power factor corrected zeta converter based improved power quality switched mode power supply," IEEE Trans. Ind. Electron., vol. 62, no. 9, pp. 5422-5433, 2015. [CrossRef]
12. R. Kumar, B. Singh, "BLDC Motor-Driven Solar PV Array-Fed Water Pumping System Employing Zeta Converter," IEEE Trans. Ind. Appl., vol. 52, no. 3, pp. 2315-2322, 2016. [CrossRef]
13. H. Vahedi, P. A. Labbé, K. Al-Haddad, "Sensor-Less Five-Level Packed U-Cell (PUC5) Inverter Operating in Stand-Alone and Grid-Connected Modes," IEEE Trans. Ind. Informatics, vol. 12, no. 1, pp. 361-370, 2016. [CrossRef]
14. M. Tariq, M. Meraj, A. Azeem, A. I. Maswood, A. Iqbal, B. Chokkalingam, "Evaluation of Level-Shifted and Phase-Shifted PWM Schemes for Seven Level Single-Phase Packed U Cell Inverter," CPSS Trans. POWER Electron. Appl., vol. 3, no. 3, pp. 232-242, 2018. [CrossRef]
15. M. Q. Duong, G. N. Sava, H. Necula, S. Leva, M. Mussetta, P. Milano, "Optimal Bypass Diode Configuration for PV Arrays under Shading Influence," vol. 2016, 2017. [CrossRef]
16. M. Q. Duong, M. Mussetta, P. Milano, "Design and Simulation of PI-Type Control for the Buck Boost Converter," vol. 2017, no. 11, pp. 79-82, 2017. [CrossRef]

17. D. C. Huynh, M. W. Dunnigan, "Development and comparison of an improved incremental conductance algorithm for tracking the MPP of a solar PV panel," IEEE Trans. Sustain. Energy, vol. 7, no. 4, pp. 1421-1429, 2016. [CrossRef]
18. V. Karthikeyan, R. Gupta, "Varying phase angle control in isolated bidirectional DC-DC converter for integrating battery storage and solar PV system in standalone mode," IET Power Electron., vol. 10, no. 4, pp. 471-479, Mar. 2017. [CrossRef]
19. M. Tariq, A. I. Maswood, C. J. Gajanayake, A. K. Gupta, "Aircraft batteries: current trend towards more electric aircraft," IET Electr. Syst. Transp., vol. 7, no. 2, pp. 93-103, 2017. [CrossRef]
20. J. Hamman, F. S. van der Merwe, "Voltage harmonics generated by voltage -fed inverters using PWM natural sampling," IEEE Trans. Power Electron., vol. 3, no. 3, pp. 297-302, 1988. [CrossRef]
21. H. Vahedi, K. Al-Haddad, H. Y. Kanaan, "A new voltage balancing controller applied on 7-level PUC inverter," IECON Proc. (Industrial Electron. Conf., pp. 5082-5087, 2014. [CrossRef]
22. R. Errouissi, A. Al-Durra, S. M. Muyeen, "Design and Implementation of a Nonlinear PI Predictive Controller for a Grid-Tied Photovoltaic Inverter," IEEE Trans. Ind. Electron., vol. 64, no. 2, pp. 1241-1250, Feb. 2017. [CrossRef]

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