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LOGIC THRESHOLD FOR MICRORING RESONATOR-BASED BDD CIRCUITS: PHYSICAL AND OPERATIONAL ANALYSES

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ABSTRACT
Moore's Law has been the fuel of expansive innovation in computing. The chip industry kept the Moore's law extant for almost four decades. However, the halt of the rapid progress of the silicon technology is incipient by reason of the physical limitations. Emerging computing proposals suggest several alternatives to current computing paradigms and technology-bases. The photonic circuitry is one of the most promising candidates with its high operation speed, energy efficient passive components, low crosstalk and appropriateness for parallel computation. Among various approaches to photonic logic, microring resonator-based Binary-Decision Diagram (BDD) architectures have a special place due to their small circuit footprint. However, the physical limitations imposed on their logic implementation has not been studied in depth to enable design of efficient circuits. In this paper, we study the physical structure and operational details of a microring resonator-based Half-Adder (HA) circuit and outline the conditions under which the performance and accuracy of information processing is compromised due to its physical characteristics. Our analyses significantly contribute to determining key physical features and operations concerning logic implementation of microring resonator based BDD HA, which informs the future design and operational optimization of the microring resonator-based BDD logic circuits.

Keywords: *Binary Decision Diagrams, Ring Resonators, Optical Processing, Photonic Logic*

1. INTRODUCTION

The performance of electronic technologies has improved exponentially with the shrinking of device sizes. Transistor-based circuits are limited by the bandwidth limitations caused by the silicon electronics and the printed metallic tracks. In addition, the increased heat generation caused by the denser designs leads to the inefficient operation of the transistors. Hence, the trend in the reduction of the size has come to an immediate halt in the recent years as the computer industry proposed multicore architectures with optical interconnects to create a parallelism of systems (Hardesty, 2009; Miller, 2010a).

The desire to continue the scaling of computing systems at thousand-fold pace in every 10 years without an increasing cost has driven a strong demand in the search of new technologies. Alternative proposals for the transistor technology have been made using carbon nanotubes (Bachtold *et al.*, 2001; Tans *et al.*, 1998; Aly *et al.*, 2015), graphene like 2D materials (Chhowalla *et al.*, 2016; Sordan *et al.*, 2009), spintronic materials (Pesin and Mac Donald, 2012; Gardelis *et al.*, 1999), novel technologies using quantum computing (Ladd *et al.*, 2010), neuromorphic computing (Shastri *et al.*, 2018; Woods and Naughton, 2012) and photonics (Rios *et al.*, 2015; Rios *et al.*, 2018; Stegmaier *et al.*, 2017; Cheng *et al.*, 2018; Lin *et al.*, 2012; Chattopadhyay, 2013; Fushimi and Tanabe, 2014). In the last decades, optics proved itself to be the best way of delivering data due to its high energy efficiency, rapid information transmission, low crosstalk and parallelism. However, optics can offer beyond communication with its energy efficient, low heat generative components and the intrinsic nature of optics allows fast and low energy computation compared to electronics (Caulfield and Dolev, 2010). Thence, photonics is one of the strongest candidates to replace the transistor technology. All-optical switching allows bypassing the optics to electronics conversions and vice versa. In addition, many pre- and post- processors have been proposed recently (Larger *et al.*, 2012; Paquot *et al.*, 2012) such as vector matrix multiplier, which reduced the computation time from $O(N^2)$ to $O(N)$ (Woods and Naughton, 2012).

In order to make a universal logic gate, a device needs to offer fan-out and bistability therefore logic level restoration, infinite cascadibility and input-output isolation (Miller, 2010b). In the BDD architecture, the use of Y-splitters can allow the architecture to have a fan-out property. Similarly, mergers allow the electromagnetic field to be superposed, therefore they provide a fan-in property, which do not exist in electronics (Caulfield and Dolev, 2010). Without the using the fan-in property, microring resonator logic circuits can allow us to make reversible operations, in which one can reconstruct the inputs from the outputs. Although most of the photonic devices do not offer bistability, there are some promising examples of demonstration of bistability using chalcogenide phase-change materials in refs. (Rios *et al.*, 2015; Rios *et al.*, 2018; Stegmaier *et al.*, 2017; Cheng *et al.*, 2018). The BDD half-adder structure in ref. (Lin *et al.*, 2012) does not offer complete bistability, the resonant condition being not completely volatile allows the microring resonator to bypass this problem in video processing applications. Another constraint in the design of the logic circuits is the device footprint. Most photonic devices having large footprint compared to electronics can be overcome by the design of 3D structures.

In the design of optical logic circuits, there are other candidates that offer switching, i.e. Mach Zehnder interferometers and photonic crystals. Although the Mach Zehnder interferometer offers switching capability, it is not preferable in the design of logic circuits because of its large footprint, reduced switching and true volatility of the state. Moreover, however, the photonic crystals are able to offer bistable switching and small footprint (Notomi *et al.*, 2005), their high scattering losses make them energy inefficient for logic applications.

A variety of materials have been used in the design of microring resonators (Wu *et al.*, 2016; Tazawa *et al.*, 2006; Guarino *et al.*, 2007). Because of the high index difference between the silicon and silicon-oxide (or air) light is confined well in the resonators, therefore the silicon microring resonators can have small footprints. In addition, the production techniques for silicon electronics are well developed. Hence, we use silicon wafer in order to be compatible with the current CMOS technology and small footprint (Bogaerts *et al.*, 2005; Green *et al.*, 2007; Fedeli, *et al.*, 2010; Gunn, 2006a; Gunn, 2006b; Bogaerts *et al.*, 2012).

The silicon-based photonic technologies are high in demand as they are constructed using widely known structures in well-established facilities. However, alternative architectures are introduced to perform logic operations using silicon-based photonic devices. This emerging trend raises questions around the physical constraints and performance limitations of these optical systems. To this day, although the physics of a single microring resonator is studied in refs. (Hammer *et al.*, 2004; Bogaerts *et al.*, 2006; Heebner *et al.*, 2004), very few attempts have been made to study the physical and operational details of photonic logic circuits. In this paper, we address this issue by using circuit designed in ref. (Lin *et al.*, 2012) as an illustrative example laying out the physical design relation between the resonators and the constraints it enforces to perform a logic operation.

BDD architecture allows the systems to be designed in a more scalable way compared to the conventional CMOS architectures, which are growing exponentially. For example, CMOS half-adder has 5 NAND gates, BDD NAND gate has 2 switching nodes and half-adder has 3 switching nodes.

This paper is organized as follows; we first introduce the fundamental principle of the BDD architecture and explain its microring resonator-based realization. In the next section, we perform extensive physical analyses on the BDD HA, discussing the transmission properties of the system and explain the interference phenomenon and the asymmetries it introduces. Later, we comment on the logic threshold, revealing the conditions under which accurate computation can be performed. Finally, we conclude by closing remarks and comments on our future work.

2. MICRORING RESONATOR IMPLEMENTATION OF BDD ARCHITECTURE

In this section, we explain the physical characteristics and operation dynamics of Binary Decision Diagram (BDD) based logic circuits. The BDD logic is an

alternative approach for performing Boolean logic operations that provide a compact representation allowing higher capacity for scaling with the increasing complexity of operations. The BDD architecture first has been proposed by Akers (1978), and refined by Bryant (1986). It is an alternative computation technique to the traditional computation techniques using Karnaugh Maps and algebraic manipulations (Akers, 1978; Bryant, 1986; Lin *et al.*, 2012). There are various physical realizations of this abstract computational model including Single Electron Tunneling (SET) Transistor Technology (Asahi *et al.*, 1997), quantum computing (Yoshikawa *et al.*, 2002), mirrors (Chattopadhyay, 2013), and optical microring resonators (Lin *et al.*, 2012). In this paper, we focus on physical realization of BDD architecture using microring resonator logic circuits.

The microring resonators have been introduced in ref. (Marcatili, 1969) and its theory has been developed by (Hammer *et al.*, 2004; Bogaerts *et al.*, 2006; Heebner *et al.*, 2004; Little *et al.*, 1997). Here, in this paper, we analyze the physical responses of multi-microring resonator devices both analytically and numerically.

Assume we have a Boolean function of n variables from $x_1, \ldots, x_n$ making the inputs of the function. In the binary decision mechanism, the signal is processed through serial switching nodes. In Fig. 1, a single BDD node is shown (left). At the node we test the variable x_i and depending on $x_i = 0$ or $x_i = 1$, the control signal coming from the incident (root) is sent to one of the two leaves. And the signal is sent to the roots testing the variable x_{i+1}. This serial switching mechanism enforces one to control each and every layer of computation with a different parameter. In order to process the information, these parameters should be independent. Fig. 1 (right) depicts the microring resonator realization of a BDD node. The microring resonator is an optical traveling wave resonator made of one or two straight waveguides called bus waveguides and a circular or a racetrack shaped waveguide.

There is a control signal is sent through the incident port and the light propagating in the ring interferes with itself, therefore creates discrete constructive resonance conditions and if the second bus waveguide exists, some portion of the light is transmitted to the drop port in the certain wavelengths. The selection of the wavelengths is done in the directional couplers. Directional couplers allow the resonator to have two fundamental modes, i.e., symmetric and asymmetric modes that can be seen in Fig. 1 (right). All the modes are the superposition of these modes. Changing the optical pathlength of the ring by changing the index of the ring externally allows us to do the switching.

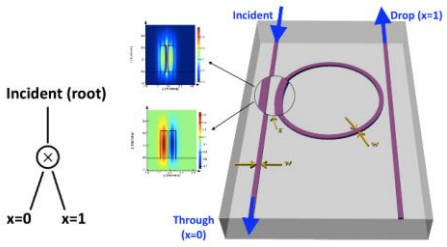
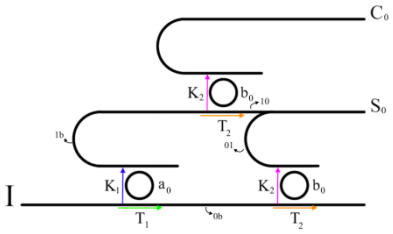


Fig. 1. Symbol of the BDD switching node (left), schematic diagram of a switch using ring resonator on SOI wafer (right) (Yakar *et al*. 2019).

3. PHYSICAL ANALYSIS OF MICRORING RESONATOR-BASED BDD HALF-ADDER

The BDD based microring resonator circuits are proposed as energy efficient alternatives in photonic logic. In this section we develop a thorough physical analysis of this emerging computing approach using the microring resonator based BDD Half Adder circuit proposed in ref. (Lin *et al.*, 2012). To the best of our knowledge, Wada's proposal is the first application of microring resonator based realization of BDD, and the analyses presented in this paper lead the way for developing efficient strategies to build new BDD circuits using microring resonators.

The BDD half adder circuit is depicted in Fig. 2 (left). The control signal is sent through the port I and tested in the resonator controlled by the variable a_0 and two resonators controlled by the variable b_0. Variables a_0 and b_0 can be temperature, voltage or light intensity. The variables are able to change the effective indices of the rings, therefore changing the transfer functions of the field amplitudes T_1, T_2, K_1 and K_2. In resonators the light splits into two waveguides with different proportions determined by the variables a_0 and b_0. In the S_0 port there are two possible paths, i.e., light going to the drop port of the resonator one, taking $1b$ waveguide and going to the through port of the upper resonator then taking 10 waveguide and light going to the through port of the resonator controlled by parameter a_0, taking $0b$ waveguide and going to the drop port of the upper resonator then taking 01 waveguide. The fields are superposed in the merger before S_0 port. The optical pathlength difference in the two different optical paths changes the transmission spectrum hence the optical pathlength difference is an important parameter in the analysis of the system. The truth table of the half-adder is shown in Fig. 2 (right). The inputs $\{a_0 b_0\} = \{01, 01\}$ are mapping to the same output, hence the effect of the 01 and 10 inputs should be symmetric to conduct a logic operations.



a_0	b_0	S_0	C_0
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Fig. 2. Schematic diagram of BDD half-adder is shown (left). The transfer functions of the amplitudes have been shown with T_1, T_2, K_1 and K_2. The waveguide names are denoted as $0b, 1b, 01$ and 10. S_0-port denotes the sum bit and C_0-port denotes the carry bit. I denotes the port where the signal in incident is sent. The truth table of half-adder is shown (right). a_0, b_0 are the inputs and S_0 denotes the sum bit and C_0 denotes the carry bit.

In this section, we first calculate the transmission characteristics of the S_0 port analytically, and discuss the critical conditions where these characteristics have implications for logic operations. We provide the effect of the temperature change and the optical pathlength differences and demonstrate the optimized cases for symmetric physical operations.

In the BDD half-adder in Fig. 2, the field that is resonant to the ring a_0 goes to the upper guide and its phase evolves as it goes through the waveguide. Then, it goes through the second ring and its phase evolves again. The field that is not resonant to the ring a_0 goes through a similar process. And these two fields are superposed before arriving to the port S_0. These two fields can be represented as B^{10} and D^{01} respectively. B^{10} and D^{01} can be represented as

$$D^{01} = e^{-i\Phi_{01}} K_2\, e^{-i\Phi_{0b}}\, T_1 = e^{-i(\Phi_{01}+\Phi_{0b})} e^{ip_{01}}\, |D^{01}| \quad (1)$$

$$B^{10} = e^{-i\Phi_{10}} T_2\, e^{-i\Phi_{1b}}\, K_1 = e^{-i(\Phi_{10}+\Phi_{1b})} e^{ip_{10}}\, |B^{10}| \quad (2)$$

where Φ_{01}, Φ_{0b}, Φ_{10} and Φ_{1b} are the phase changes in the waveguides are depicted in Fig. 2. The total phase delays represented by p_{01} and p_{10}, introduced at the rings and the couplers at the top of Fig. 2.

The fields are superposed before arriving the S_0 port. Assuming the recombiner is symmetric, the theoretical total field becomes

$$S_0 = \frac{D^{01} + B^{10}}{\sqrt{2}} \quad (3)$$

The single recombiner is simulated using Lumerical varFDTD shown in Fig. 3. The transmission response of two beams confirms our assumption for $1.55\mu m$, so we can claim the fields are superposed with equal weight up to this point. The simulations performed here are two-dimensional FDTD with effective-index method which may yield higher energy losses. In order to increase the accuracy of energy calculations three-dimensional simulations can be performed.

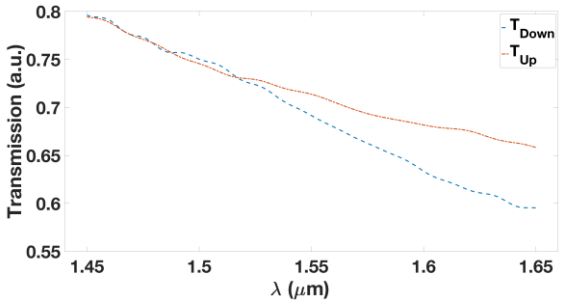


Fig. 3. Transmission spectrums of recombiner is simulated in Lumerical MODE solutions. The simulation is run for two different beams sent from two different arms separately. T_{Up} (orange, dashed-dotted) line represents the case for the beam sent from the top arm and T_{Down} (blue, dashed) line represents the beam sent from the bottom arm.

Plugging the above Eq. (1) and (2) into Eq. (3) and factoring out the phases of D^{01} reduces the equation into

$$S_0 = \frac{e^{-i(\Phi_{01}+\Phi_{0b})} e^{ip_{01}} \left(|D^{01}| + |B^{10}| e^{i\Delta\Phi} e^{i\Delta p}\right)}{\sqrt{2}} \quad (4)$$

So the transmission intensity becomes,

$$Tr = S_0^* S_0 = \frac{1}{2}\left(|D^{01}|^2 + |B^{10}|^2 + 2|D^{01}||B^{10}|\cos(\Delta\Phi + \Delta p)\right) \quad (5)$$

If we swap the input signals, i.e. $a_0 b_0 \rightarrow b_0 a_0$, it will lead $\Delta p \rightarrow \Delta p$ because the effect of the resonators in Eq. (1) and (2) are symmetric. In order the transmission spectrum to be symmetric, $\cos(\Delta\Phi + \Delta p)$ must be constant when input signals are swapped. So, $\Delta\Phi = 2\pi m$, where $m \in \mathbb{Z}$. That is why optical path length difference should be zero (or $2\pi m$) in order to have a constant spectrum when we interchange the input signals. In order to tune the rings and the couplers there are various effects used such as electro-optic effect and thermo-optic effect. However, if these effects are not local, the optical path length difference will depend on the light intensity or temperature profiles. Light intensity or temperature profiles must be known in order to minimize the optical path difference.

Although the circuit in Fig. 2 is asymmetric by means of inputs, the physical responses can be made symmetric as seen in Figs. 4 and 5. However, the switching energies from logic-0 to logic-1 and logic-1 to logic-0 are not going to be identical to each other. This phenomenon is also seen in electronics, i.e., in transistor based electronic circuits, energetic cost of transitioning from logic-0 to logic-1 and logic-1 to logic-0 is not identical due to physical effects such as charge sharing and parasitics.

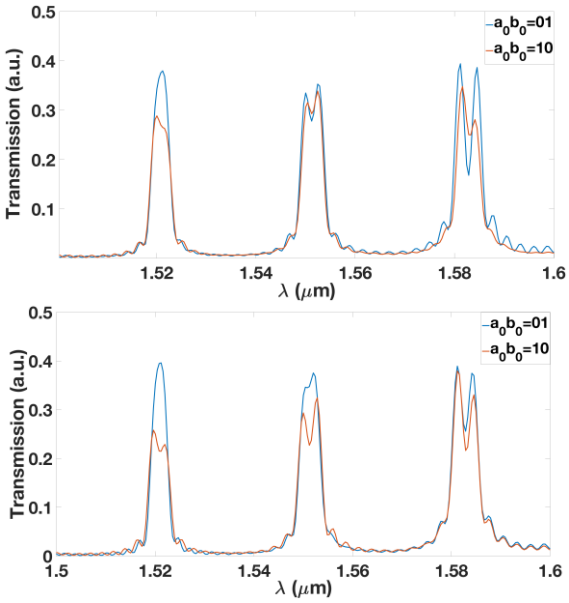


Fig. 4. Transmission spectrum of S_0 port at $1\ \mu m$ (top) and $1.05\ \mu m$ (bottom) difference in the waveguides for 01 and 10 signals with at $r = 2.7\ \mu m$, $g = 0.8\ \mu m$ at one ring at 300 K and the other at 315 K.

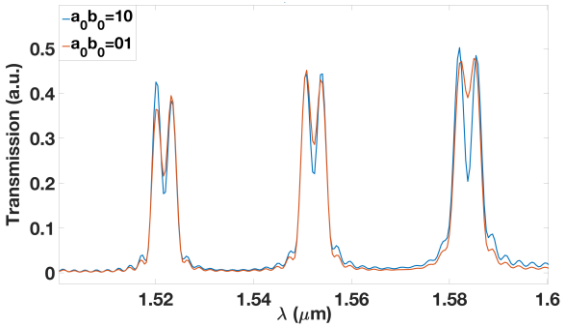


Fig. 5. Transmission spectrum of S_0 port at $r = 2.7\ \mu m$, $g = 0.8\ \mu m$ at one ring at $300\ K$ and the other at $340\ K$.

4. THRESHOLD FOR LOGIC OPERATION

In the previous section, we have discussed the role of the physical effects in performing logic operations. The analyses we have developed provide a clear picture on physical conditions that are required to obtain accurate outcome of computation. The physical states that are used to represent logic-0 and -1 states have to be distinguishable for information processing to happen with precision. In this section, we define the threshold for logic operations to take place accurately.

The crosstalk in the computation is not completely avoidable. Even if, a completely symmetric structure is designed, there may be some variations while the circuits are manufactured. Ring resonators are very sensitive to these variations. Thus, the response of the circuits may change significantly for a small change in the dimensions of the components. Although we cannot overcome these variations in production and tuning in without consuming too much energy, we may still continue to do the logic operation with a carefully chosen threshold.

Logic mapping makes one to be able to envisage the possible outputs and their corresponding inputs. While the device is operated the physical response of the designated inputs must give well-defined outputs and the output sets must be disjoint. When these conditions are satisfied, it is appropriate to define regions, i.e. envelope curves, to quantize the outputs. Therefore, one can define a threshold for the decision-making.

In the half-adder structure, we need to group the inputs $(a_0 b_0)$ as $\{00, 11\}$ and $\{10, 01\}$ while inspecting the S_0 bit in the Fig. 2 (right). We need to design the physical system so that the two groups of outputs, i.e. 0 and 1 state, are well defined and disjoint. When the two physical outputs have an intersection, the logic state will be indeterminate. If the envelope curves of two outputs are intersecting, there is a probability that the actual transmission curves of the manufactured system are intersecting because there can be some fluctuations because of the environment, production or tuning mechanism. In order to have a stable system, we need to separate the regions that are bounded by the envelope curves.

In Fig. 6 (top), physical response of inputs $a_0 b_0 = 11$ intersects the region bounded by S_0 Low and S_0 High. Hence, there is no threshold for logic for some optical pathlength. Due to some external effects or manufacturing, the device may not be able to conduct the logic operation. In the Fig. 6 (bottom), $1.793\delta\lambda$ shift of the resonances will create a threshold for logic operation at $1.55\ \mu m$. Here, the coefficient 1.793 is set based on the numerical calculation of the input-output mapping. It can be precisely formulated for based on the physics and operation of any given optical logic circuit.

So, if the shift of two peaks is more than $1.793\delta\lambda$, the outputs are well defined and disjoint. As we increase the shift of two resonant peaks more and more, the transmission responses of two logic outputs will be more and more away from each other. This is illustrated in Figs. 7 (top) and 7 (bottom). As can be seen in Figs. 6 (bottom), 7 (top) and 7 (bottom) the S_0 (Low) and S_0 (High) come closer to each other with the increasing shift between the resonances of two layers of switching nodes since transmission responses have a less effect on each other with the increasing shift of the resonant wavelengths. Hence, if we increase the switching energy, the importance of the phase modulation will decrease inasmuch as the crosstalk is lower. That means the phase sensitivity decreases.

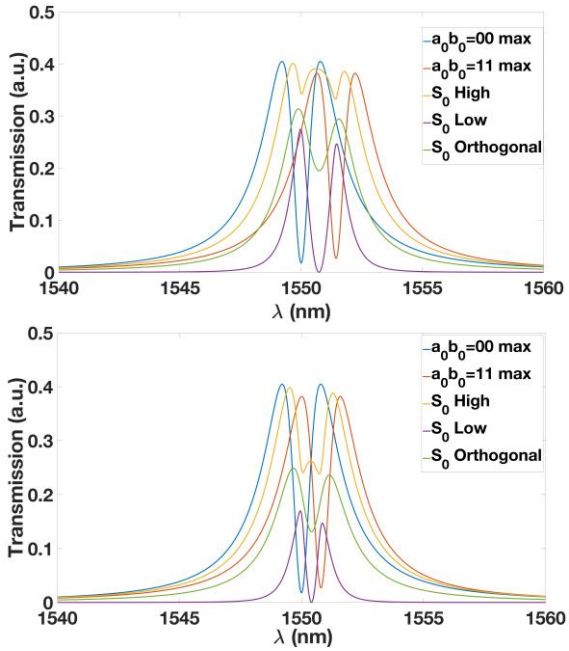
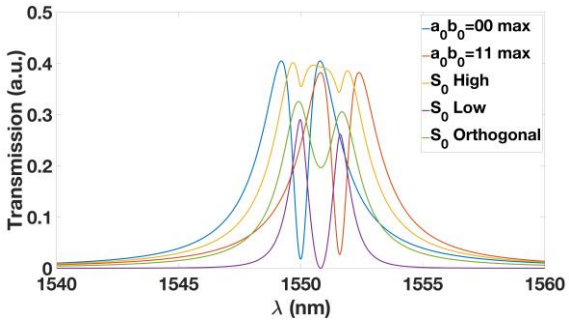


Fig. 6. The theoretical transmission response of the Half-Adder Structure with $|K_1| = 0.8$, $|K_2| = 0.75$, efficiency 0.85 and the distance between two resonances as $\delta\lambda$ (top) and $1.793\delta\lambda$ (bottom). Vertical axis denotes the transmission in the linear scale and the horizontal axis denotes the wavelength in nm.



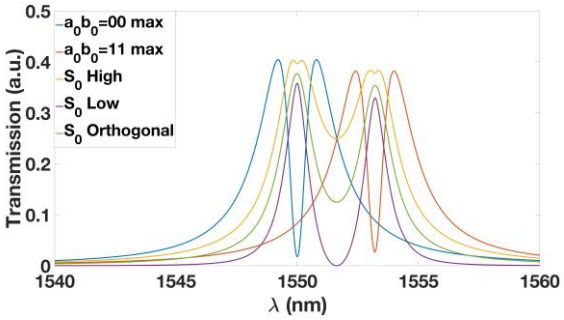


Fig. 7. The theoretical transmission response of the Half-Adder Structure with $|K_1| = 0.8$, $|K_2| = 0.75$, efficiency 0.85 and the distance between two resonances as $2\delta\lambda$ (top) and $4\delta\lambda$ (bottom). Vertical axis denotes the transmission in the linear scale and the horizontal axis denotes the wavelength in nm.

5. CONCLUSIONS

In this paper, we perform a physical analysis of the BDD half-adder with microring resonator switching nodes. The physical analyses we perform show that, the switching parameter (temperature, voltage etc.) and optical pathlength are crucial factors in the design of microring resonator logic circuits because of the interference phenomenon. The transmission response of the device is made symmetric by tuning the tuning parameter, waveguide lengths or a mixture of these. Because of the high sensitivity of the silicon microring resonators, a threshold for logic operation is set. When the waveguide lengths are not optimized the minimum distance of the two resonant at the S_0 port peaks should be $1.793\delta\lambda$, where $\delta\lambda$ is the half-width half-maximum in the transmission vs. wavelength graph.

Physical realizations of BDD architecture are presented using Single Electron Tunneling (SET) transistors (Asahi *et al.*, 1997), quantum computing (Yoshikawa *et al.*, 2002), mirrors (Chattopadhyay, 2013), and microring resonators (Lin *et al.*, 2012). Although the physical analyses of single microring resonators are done in refs. (Hammer *et al.*, 2004; Bogaerts *et al.*, 2006; Heebner *et al.*, 2004), analysis of BDD logic circuits are done and the physical limitations of the microring resonator based BDD half adder are found for the first time in this work. These analyses will shine light on the future designs and energy optimizations of other microring resonator based BDD circuits.

The theoretical analyses we perform here present guidelines in designing the optimum physical circuit structure as well as information dynamics that leads to minimum energy dissipation in microring resonator-based logic circuits. As a part of our future work, we aim to design and analyse other microring resonator-based BDD logic circuits with varying complexity to illustrate how the performance scale with size and how the energy dissipation varies based on structure and operation.

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