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A COMPREHENSIVE DETERMINING OF CAPACITANCE -VOLTAGE PARAMETERS OF ELECTRONIC DEVICES WITH METAL AND *p*-Si JUNCTION

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ABSTRACT

Al-*p*-Si-Al structures were fabricated and temperature dependent capacitance versus voltage measurements were performed in this study. The Al contacts were grown by the sputtering method and then capacitance-voltage characteristics of the devices were performed with forward and reverse biases. According to this measurements, the $C^{-2}-V$ plots were conducted. With the help of those calculation, the barrier height vs temperature ($\Phi_{CV}-T$), the carrier concentration vs temperature (N_A-T) and the depletion width vs temperature ($w-T$) graphs were plotted. In conclusion, it has been seen that the Φ_{CV} and w decreased, and N_A almost remained constant with increasing temperature.

Keywords: Heterojunctions, Capacitance-Voltage, Barrier Height

1. INTRODUCTION

The devices with metal-semiconductor junctions are one of the important electronic circuit components in the electronic industry. These devices are commonly made by using metals like Ni, Au, Al etc. and semiconductor substrates like Si, GaAs, InP etc. [1 - 2]. The interface between the metal/semiconductor (MS) shows a rectifying property and this is a very critical point in industries like optoelectronic and switching technology [3]. In this interface layer there exists a barrier height (BH) and the characteristics of the semiconductor device are generally depend on this diode parameter [4]. Today, Schottky barrier formation at the MS junction still atracts attention in the field of semiconductor devices [5].

In the literature there are variety of examples of experimental studies of barrier heights in MS systems. Among the Schottky barrier height (SBH) measurement methods, the capacitance–voltage (C–V) method is one of the most convenient and common method, by which the built-in potential V_{bi} can be drived from the extrapolation of the intercept in the x- axis, which is "voltage", in the straight line of C^{-2} - V curve [6]. In order to perform this extrapolation, the carrier concentration inside the structure is usually accepted to stay stable. Besides, in other cases – namely in the cases of unstable doping concentration, which may be the result of ion embedding, diffusion of carriers, unexpected impurities [7 - 8] or tendency to change in the temperature [9] - this method is not suitable, since the C^{-2} - V curves show nonlinear characteristics. According to some reports in the literature, this method was still applied in a range around 0 V in order to eliminate those undesired consequences [9 - 11]. However, when zero bias temperature dependent barrier heights are tried to be calculated from C^{-2} - V measurements, it is seen that the value of the barrier height changes with temperature gradient and this situation is generally attributed to the change in the crystal form at the MS interface [12 - 13].

The purpose of this paper is to determine and interpret the temperature dependent change of characteristics metal-Si device parameters such as the barrier height Φ_{CV}, the carrier concentration N_A and depletion width w, and furthermore the temperature dependent change of C–V and C^{-2}–V curves.

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Another important parameter at the MS contacts is the carrier concentration and under temperature gradient it is expected to be constant because of the linearity of C^{-2}–V curve [14]. However it may demonstrate a deviation from the linearity especially at low temperatures [15], and may decrease sharply. On the other hand, the depletion width at the MS contact is expected to be decreased by increasing carrier concentration [6, 16]. In this paper, we report a MS device fabrication and the SBH, carrier concentration and the depletion region width from *C*–*V* measurements.

2. MATERIALS AND METHODS

According to the Si wafer cleaning procedures in the literature [17], the semiconductor crystal - Si - was chemically dipped in CP-4 ($HF:CH_3COOH:HNO_3$; 1:1:2) solution at least 3 min initially, and then was exposed to $HF:H_2O$ (1:15) mixture to eliminate the oxidized layer on the substance surface. After this cleaning procedure a tiny Al film was groved on the matt surface of *p*-Si by thermal evaporation method. The Al coated *p*-Si substrate was annealed at 570 °C for 3 min under the gas flow of argon inside a furnace. Then, Al was evaporated on the shadow mask with holes (about 1 mm) and dot Schottky junctions were fabricated on the front of *p*-Si as seen from the figure 1. By those procedures, the Al/p-Si/Al Schottky diodes were formed.

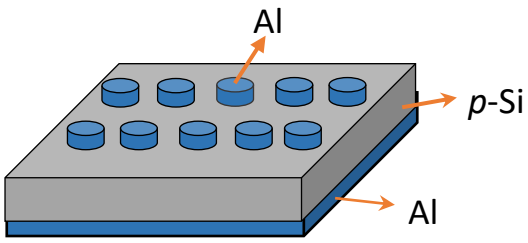

Figure 1. (Color online) The illustrative model of the Al/p-Si/Al diodes

The *C*–*V* measurements of fabricated metal –Si rectifying device was conducted through ARS 4K closed cycle helium (He) cryostat, which has LakeShore 330 temperature controller with 0.2 K step, between 40-320 K temperatures using Boonton 72B capacitance meter. The depletion capacitance calculations were achieved from the following formula [6, 21];

$$\frac{1}{C^2} = \frac{2\left(\Phi_{CV} - V_p - V\right)}{q\varepsilon_s N_A A^2} \tag{1}$$

In equation (1), Φ_{CV} is the barrier height according to *C*–*V* measurements and V_p stands for the difference electrical potential between the Fermi level and the valance band maximum in the neutral region of *p*-type semiconductor and it is expressed by the equation

$$V_p = kT\ln\left(\frac{N_v}{N_A}\right) \tag{2}$$

where N_v is the state density in the valance band [6, 20] and it is calculated using the carrier concentration N_A, which can be drived from the slope of the linear C^{-2} - V plot at each measurement temperature. The carrier concentration N_A can be attained from the derivative of equation (1) as follows;

$$N_A = \frac{2}{q\varepsilon_0 A^2}\frac{dV}{d(C^{-2})} \tag{3}$$

$(\Phi_{CV} - V_p) = V_{D0}$ in equation (1) gives the diffusion potential, V_{D0}, at the zero bias and it can be calculated from the extrapolation of the linear part of C^{-2}–V curve to the V axis. So we may give the equation (1) as;

$$\frac{1}{C^2} = \frac{2(V_{D0} - V)}{q\varepsilon_s N_A A^2} \tag{4}$$

In this simplest form of depletion layer capacitance per unit area formula, the expression in the numerator can be written as $2(V_{D0} + V)$ according to the applied voltage. Also, ε_s is the permittivity of the semiconductor, q is the electronic charge and A is the diode area in equation (1). According to those formulas, the capacitance to voltage (C-V), C^{-2} to V, Barrier height to temperature (Φ_{CV}-T), carrier concentration to temperature (N_A-T) and depletion width to temperature (w-T) plots were conducted.

3. RESULTS AND DISCUSSION

Figure 2 demonsrates the experimental *C-V* measurement results of the Schottky rectifier junction with a structure of Al-*p*-Si-Al in the temperature range of 40-320 K with 10 K steps. The *C-V* measurements were made at high frequency of 500 kHz, to prevent the contribution of the interface state charges and trap levels to the diode capacitance [6,9,16]. Therefore, this anomalous behavior observed in C-V results of Schottky diodes (SDs) has been generally ascribed to the presence of interface layer effects and series resistance R_S (between the space charge region and the Al contact) of the neutral region of the semiconductor body [23-28]. On the other hand, the series resistance R_S also plays an important role while shaping the *C-V* characteristics of the SDs, and causes them to be different from those that would be expected [23-28].

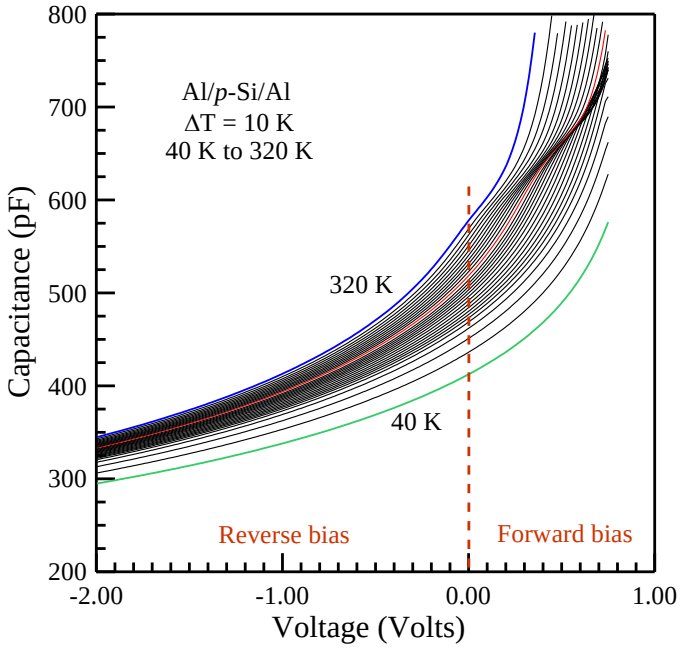

Figure 2. (Color online) Forward and reverse bias capacitance-voltage characteristics for the Al/*p*-Si/Al diode with steps of 10 K at 500 kHz

It has been stated in some investigations that there exists an abnormal peak in forward *C-V* characteristics [23-28]. The origin of such peak has been referred to the interface states by Ho et al. [23], and to the series resistance effect by Chattopadhyay et al. [25-28] and Chattopadhyay [28]. As expected, at high forward bias voltage there is always a deviation of the ideality in the *C-V* curves that has been definitely claimed to be the result of interfacial state density and series resistance in device.

That is, the presence of the R_S appears an anomalous in the forward bias *C-V* characteristics, and also turns out such a strange voltage dependence of the capacitance. Therefore, the forward bias capacitance measurements were made up to 1.0 Volt. The reason for this is not to observe the capacity peak which appears from the series resistance effect and interface states at high voltages.

The C^{-2} to *V* plot at reverse and forward bias at each temperature is shown in the Fig. 3. The C^{-2} to *V* curves at reverse bias at each temperature especially are used to determine the parameters such as the barrier height, carrier concentration, diffusion potential and depletion width. As seen from the figure, at reverse bias portion of C^{-2} to *V* curves at each temperature, the graph shows almost a linear behavior. However at about zero bias there exist a fluctuation and deviation from linearity in the graph. This may be the result of the carrier concentration behavior [22].

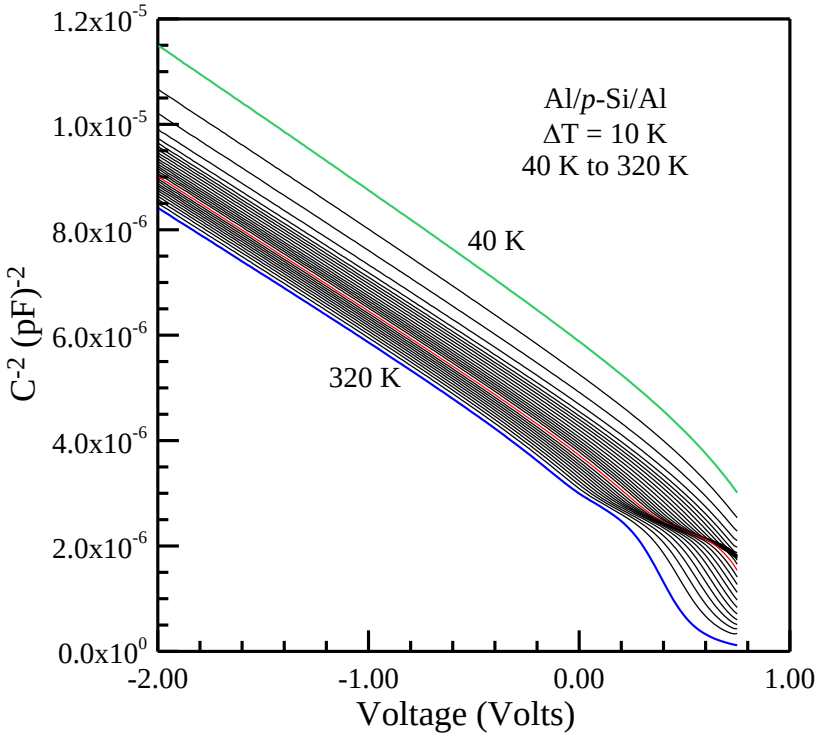

Figure 3. (Color online) Forward and reverse bias C^{-2} - *V* characteristics for the Al/*p*-Si/Al diode with steps of 10 K at 500 kHz

Barrier heights of the device according to varying temperature is given in the Fig. 4. If a barrier height is temperature depended – like our samples – it can be expressed as:

$$\Phi_{CV}(T) = \Phi_{CV}(T = 0) - \alpha T \tag{5}$$

Where $\Phi_{CV}(T = 0)$ is the BH at zero temperature and α is the temperature coefficient of the barrier hegiht [3]. Since α is the slope, it can be calculated from the graph and it is 0.00153 V/K. Φ_{CV} can be calculated by a simple modulation in the expression:

$$(\Phi_{CV} - V_p) = V_{D0} \tag{6}$$

$$\Phi_{CV} = V_{D0} + V_p \tag{7}$$

with the help of eqn. (2).

$$\Phi_{CV} = V_{D0} + kT\ln\left(\frac{N_v}{N_A}\right) \text{ [6, 21]} \tag{8}$$

The values of Φ_{CV} in Fig. 4 was calculated from eqn. (8) and the graph was plotted according to these values. As can be seen from Fig. 4, According to the fit equation Φ_{CV} = 1.94 -0.00153T eV to the partion in 100 K-320 K range of the curve, Φ_{CV} at zero temperature is 1.94 eV. Here, α is the temperature coefficient.

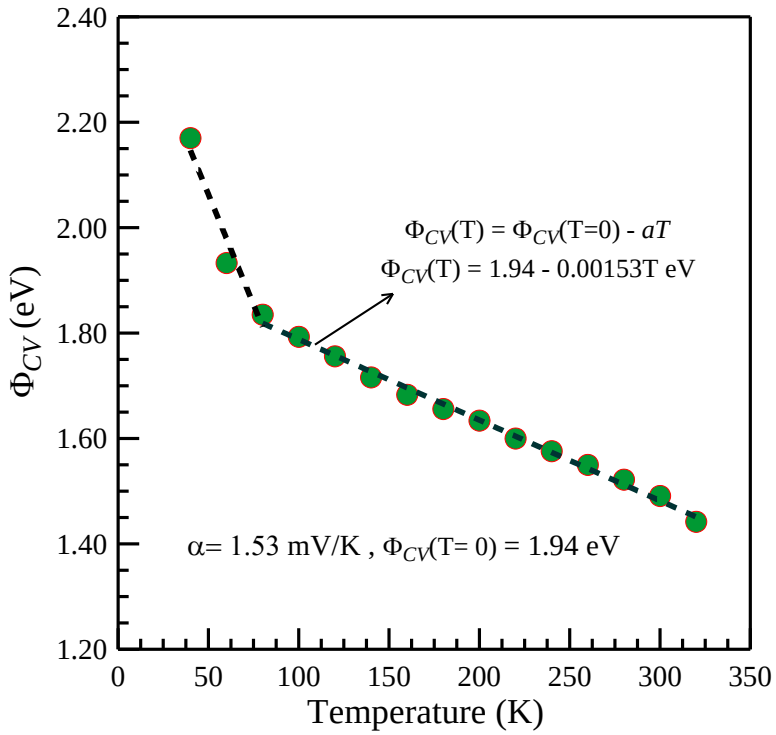

Figure 4. (Color online) Barrier height versus temperature plot from the C^{-2} - V curves for the Al/*p*-Si/Al diode

In figure 4, the temperature constant of the BH, that were attained from the experimental results, is seen as α = -1.53 meV/K for the Al/*p*-type Si SD and this is too far from the temperature coefficient value - which was -0.24 meV/K - of the energy gap for Si given in ref. [29] and [30] from temperature coefficient of the barrier height reported for Si semiconductor by some authors [20,30, 32]. For example, it was stated that the BH temperature coefficient value is -0.121 meV/K for PtSi/*p*-Si by McCaffrty et al. [20]. Also by Aboelfotoh and Tu [31] the so called values are found in the range of (-0.128) - (-0.147) meV/K for Ti/*p*-Si and $TiSi_2$/*p*-Si and by Karatas et al. it was -0.247 meV/K for hydrogen terminated *p*-type Si. Those differences can be attributed to the formation of an oxide layer between Si and Al metal. Known conventionally, there exists an oxide region on a Si surface regardless of wafer cleaning processes whether it was etched with diluted HF or not [33-37]. Furthermore, the Si surface is usually coated with a thin insulating layer, if Si wafers are polished by

ordinary methods and etched by chemicals, and if the metal is evaporated in a traditional vacuum chamber under a pressure of almost 10^{-5} torr. The thickness of this oxide layer may be between 10 and 30 Å depending on the Si wafer preparation process. Interface layers may also be encountered in relation to the exposure of water or vapour onto the surface of the wafer before placing the evaporation chamber [25-27,33-39]. The Metal-Si contacts fabricated under those conditions are not perfect neighbouring contacts because of the insulating interfacial layer in the order of atomic dimensions [25-27,33-39]. For a satisfactory insulating layer, the interface states are in steady contact with the semiconductor and they do not keep in touch with the metal [25-27,33-39]. Therefore, the dielectric constant value (ε_i) of the interfacial layer should not be very different from the value for bulk SiO_2 [25-27,33-39].

Also, one can see figure 4 that the barrier height decreases with the increasing temperature. This characteristic is in close agreement with the results that were stated in the literature which says that the barrier height is inversely proportional to the temperature in Si [40, 41]. According to Aboelfotoh [40], Crowell et al. [41] and Cola et al. [42] this behaviour can be associated with the band gap of Si and the decrease in the carrier concentration around the space charge region [43].

The N_A against temperature plot is demonstrated in Fig. 5. As seen from the figure, the carrier concentration approximately shows a very slight increase from 320 K to 80 K and then decreases sharply.

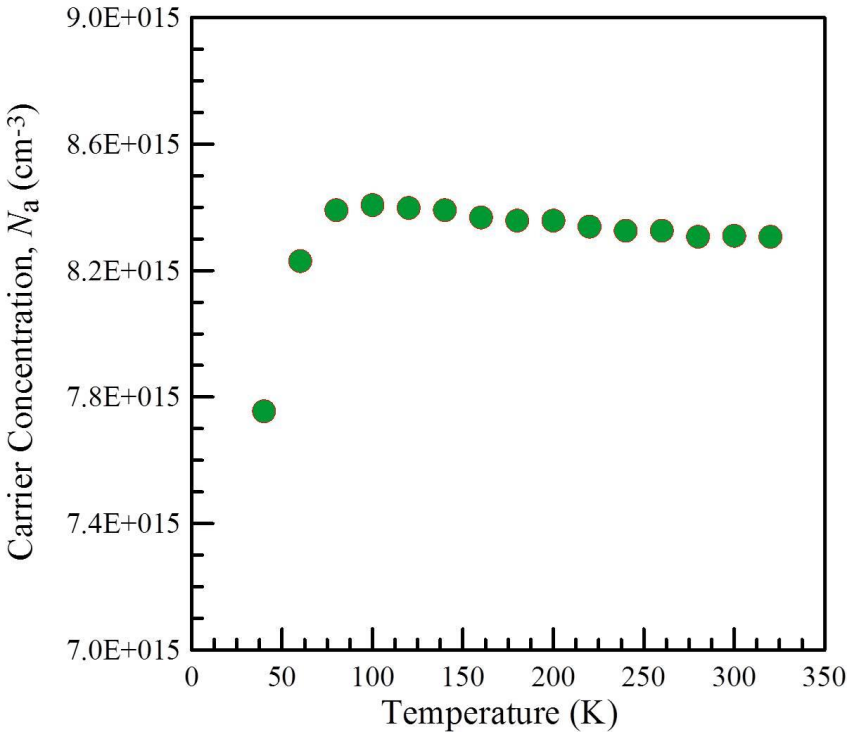

Figure 5. (Color online) Carrier concentration versus temperature plot from the C^{-2} - V curves for the Al/*p*-Si/Al diode

Finally the depletion width versus temperature graph can be seen from Fig. 6. From the graph it can be seen that the depletion width shows an almost lineer behavior from 320 K to 80 K, and then sharply makes a curvature and increases with a bigger slope. The sharp increase at 80 K may be attributed to the decrease in carrier concentration at this temperature.

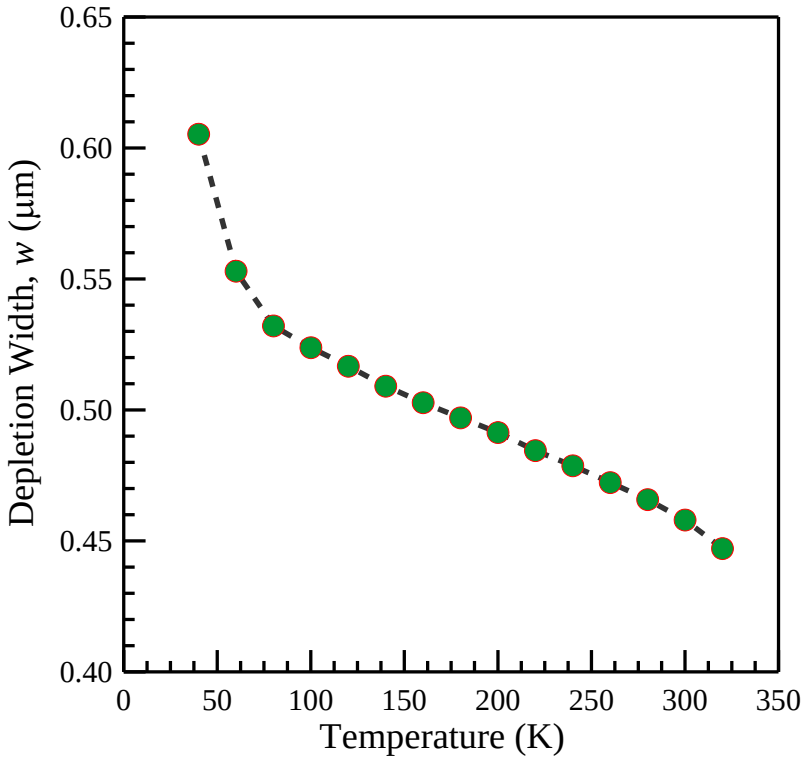

Figure 6. (Color online) Depletion width versus temperature plot from the C^{-2} - V curves for the Al/p-Si/Al diode

4. CONCLUSION

In this study, Al Schottky contacts were fabricated by the sputtering method over p-Si-Al substrates and forward and reverse bias temperature dependent capacitance versus voltage measurements were conducted. With the help of those measurements depletion layer, the capacitance were calculated and C^{-2} vs V graph was plotted. With basic calculations, Barrier height vs temperature (Φ_{CV} vs T), the carrier concentration vs temperature (N_A vs T) and the depletion width vs temperature (w vs T) graphs were done. In conclusion it has been seen that - with increasing temperature - the Φ_{CV} decreases, N_A remains constant and w decreases.

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