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A Ladder Multilevel Inverter Topology with Reduction of On-state Voltage Drop

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ABSTRACT

In this paper, a generalized symmetrical multilevel inverter namely ladder multilevel inverter (LMI) is proposed. The LMI can generate DC voltage levels and voltage harmonic similar to other topologies with less number of switches and gate drivers. In addition, as compare to traditional multilevel inverter, LMI has less on-state voltage drop and conduction losses, because three switches are turned on at any given time. The proposed topology results in reduction of installation area and cost and has simplicity of control system. This converter has been used in a dynamic voltage restorer (DVR). The operation and performance of the proposed LMI has been verified by experimental and simulation results. The simulation results show its capability in voltage generation and voltage sag compensation.

Keywords: Ladder multilevel inverter, Symmetrical cascade, Reduction of on-state voltage drop

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1. INTRODUCTION

In recent years, power electronics engineers have paid great attention to multilevel inverters as a new kind of power converter. Most multilevel inverters have an arrangement of switches and capacitor voltage sources. By a proper control of the switching devices, these can generate stepped output voltages with low harmonic distortions [1]-[3]. These multilevel inverters are widely used in manufacturing factories and acquired public recognition as one of the new power converter fields because they can overcome the disadvantages of traditional inverters. Multilevel inverters can be divided into three remarkable topologies: diode-clamped [4]-[6], flying capacitors [7]-[9], and cascaded H-bridge cells with separate DC sources [1], [9], [10]. In addition in recent years, many topologies have been suggested to multilevel converter with a low number of switches and gate driver circuits [11].Compared with the traditional two-level voltage inverter, the main advantages of the multilevel inverter are a smaller output voltage step, lower harmonic components, a better electromagnetic compatibility and lower switching losses. The main disadvantages of the multilevel inverter are the use of a larger number of semiconductors and a complex control circuitry and needing the equilibrating of the voltage at the boundaries of capacitors [1], [9], [12],[13].

The modulation methods used in multilevel inverters can be classified according to switching frequency. A very popular method in industrial applications is the classic carrier based sinusoidal pulse width modulation (SPWM) that uses the phase shifting technique to reduce the harmonics in the load voltage[14],[15]. Other methods that work with low switching frequencies generally perform one or two commutations of the power semiconductor switches during one cycle of the output voltages, generating a staircase waveform. Representatives of this family are multilevel selective harmonic elimination and space vector control[16], [17].

Modern industrial processes are based on a large amount of electronic devices such as programmable logic controllers and adjustable speed drives. Various power quality problems faced by these industrial and commercial customers. Custom power devices are introduced in the distribution system to deal with various power quality problems. Among various power quality problems, voltage sags are more serious as they can cause customer equipment to malfunction or a production shutdown. An effective way of controlling the sags is to inject power into the system using DVR. The DVR is the best suited to protect sensitive loads against voltage disturbances, where it can inject a controllable voltage in series with the supply voltage to keep the voltage constant at the load terminals [18]- [21].

This paper investigates the multilevel inverters and focuses on topologies where the input DC voltages are the same. These topologies are known as symmetrical multilevel inverters. When the number of levels increases, the difference between output waveform and reference sinusoidal waveform would be reduced. This paper proposes a novel topology for symmetrical multilevel inverter with reduced number of switches. In order to verify the capabilities of proposed inverters in injection of voltage, the proposed topology is used in DVR. The main purpose of this paper is reduction of the components of the multilevel inverters. Simulation results verify the theoretical consideration, too. The operation and performance of the proposed multilevel inverter has been verified on a single-phase nine-level multilevel inverter prototype.

2. PROPOSED MULTILEVEL CONVERTER

Fig.1 shows the basic structure of a LMI with *n* DC voltage source per phase. Depending on its switching state, the output voltage levels is obtained. The circuit consists of *n* DC voltage sources, *n* bi-directional switches and one H-bridge cell. The LMI converter requires bi-directional switches with capability of blocking voltage and conducting current in both directions. The common emitter anti-parallel IGBT with diode pair arrangement has been used in this topology. This bi-directional switch arrangement consists of two diodes and two IGBTs. This inverter has two parts: main switches (basic unit) and one H-bridge cell. Operation of LMI is the same as single phase H-bridge cell inverter [11]. Single phase H-bridge cell inverter can get zero level, input voltage and negative of input voltage in output. The basic unit produces waveform with one polarity in two half period. H-bridge cell inverses waveform in half period and produces zero level. So other polarity of waveform is obtained and sinusoidal waveform is produced. Zero level could be produced with H_1 and H_3 or H_2 and H_4. Since the DC voltage sources are the same, this multilevel inverter can be known as a ladder multilevel inverter. With suitable toggling of switches, a phase voltage waveform is obtained. The effective number of output voltage levels in ladder multilevel inverter is the same as symmetric cascade inverter and it is given by (1).

$$m = 2n + 1 \tag{1}$$

n is number of DC voltage sources. The maximum output voltage (V_{OMax}) of this new topology can be determined by:

$$V_{O\max} = V_1 + V_2 + \ldots + V_n \tag{2}$$

The two main components of the power losses in a switch are conduction losses and switching losses. Always, in each phase leg, a set of three switches is on at any given time so LMI has less on-state voltage drop and conduction losses of switches.

3. SWITCHING and OPERATION

The control of the new family of multilevel inverters is to choose a series of switching angles to synthesize a desired sinusoidal voltage waveform. In the following, a method is proposed for determination of switching angles to synthesize a desired sinusoidal voltage in the LMI. This method corresponds to pulse widths modulation (PWM).

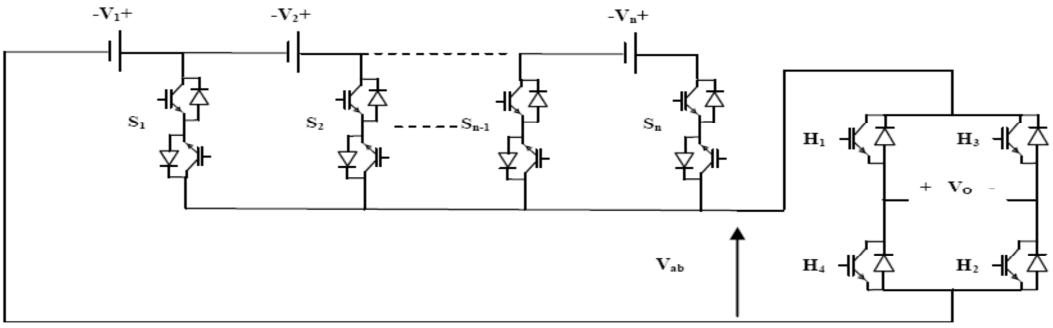


Figure 1. Proposed LMI

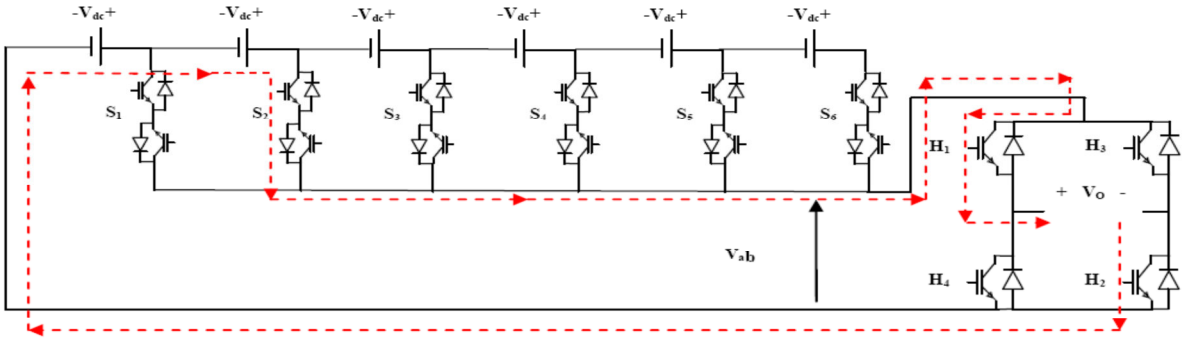
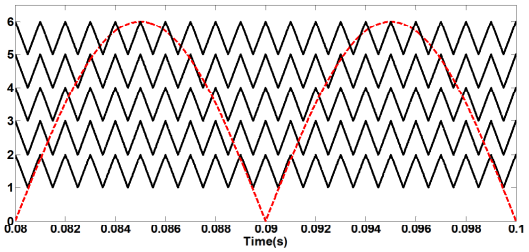


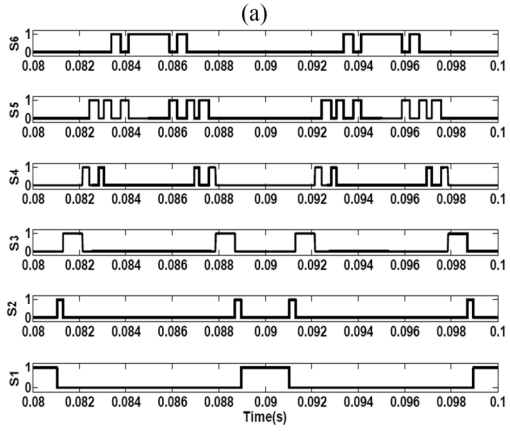
Figure 2. 13-level proposed symmetric multilevel inverter.

The principle of the proposed PWM is based on a comparison of among sinusoidal and absolute of sinusoidal reference waveform, with vertically shifted carrier waveforms. At each instant, absolute sine wave and sine wave are compared with carriers signal (triangular or direct line waveforms). To generate *m* levels, *(m-3)/2* carriers are needed. The member of this new family is the 13- level inverter shown in Fig. 2.

It is assumed that the DC voltage sources are all the same. The magnitude of each voltage sources (V_{dc}) is considered 1p.u. Operation of 13- level suggested inverter is shown in Fig.3. Modulation waveforms to switching for main switches that produces waveform with one polarity are shown in Fig.3(a). The carriers are triangular that are shifted vertically. They have the same amplitude and the same frequency. The sine reference wave has a frequency f_r and an amplitude A_r. f_r defines output frequency. Input signals of main switches gate in one period are shown in Fig.3(b). With this switching, input voltage of H-bridge cell (V_{ab}) that is shown in Fig.3(c) is produced. Modulation waveforms to switching H-bridge cell are shown in Fig.3(d).Fig.3(e) shows input signals of H-bridge switches gate. Switching function of H-bridge cell produces zero level and inverses waveform in half period to obtain output voltage. It is considered that the output voltage waveform shown in Fig.3(f) is a typical staircase 13- level waveform. Fig.3(g) describes the harmonic spectrum of output voltage. It can be observed that, presented structure is effective to obtain desired harmonic level. Total harmonic distortion (THD) in this case for output voltage is 10.17 percent.



(a)



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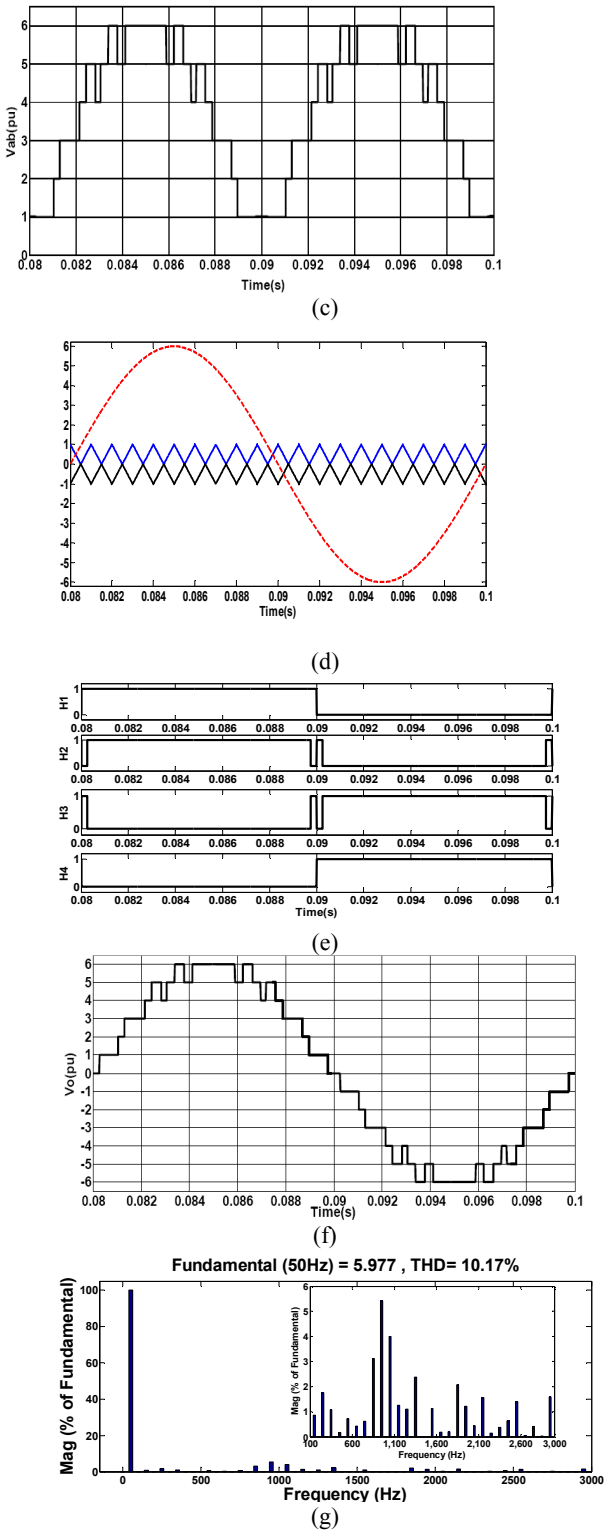


Figure 3. Operation of 13- level suggested topology (a) modulation signal of main switches (b) main switches gate signals (c) H-bridge input voltage (d) modulation signal of H-bridge (e) H-bridge gate signals (f) output phase voltage (g) Harmonic spectrum of output phase voltage.

4. COMPARISON OF THE LMIWITH CONVENTIONAL MULTILEVEL INVERTERS

In all well-known multilevel inverter topologies, the required number of power devices depends on the output voltage level. However, increasing the number of power semiconductor switches increases the inverter circuit size, cost, installation area and control complexity. The reliability of a system is indirectly proportional to the number of its components. Clamping diodes are not required in the FCMI and CMI, while balancing capacitors are not needed in the DCMI and CMI. Although the same number of main switches and diodes is needed in the DCMI, FCMI and CMI, the total numbers of components needed in these three topologies are totally different at higher voltage levels. The CMI requires the least number of total main components. In LMI, the number of switches is reduced and the devices can be switched at low frequency, therefore the inverters have higher efficiency. The main advantage of the proposed structure is generation of considerable number of DC voltage levels with less number of switches. Although this topology requires multiple DC sources, in some systems they may be available through renewable energy sources such as photovoltaic panels or fuel cells or with energy storage devices such as capacitors or batteries. Minimum harmonic distortion can be obtained by controlling the conducting angles at different inverter levels. Switching algorithm is easy and not complex.

The number of components needed in each system is firstly compared. Table I compares the main power component requirements per three phases among three conventional and proposed multilevel inverters, where *m* is the number of voltage levels. From Table 1, M.D indicates to main diodes, C. D and B.C indicate to clamping diodes and balancing capacitors, respectively. Each switch requires one gate driver. Reduction of gate driver is obtained with reduction of switches number. Table 2 compares the switches requirements per three phases among three conventional and LMI. Fig.4(a) shows the total required components in the multilevel inverters as a function of the number of voltage levels. In the entire voltage range, to synthesize the same number of voltage levels, LMI requires the least number of total main components. Fig.4(b) shows the required components compression between CMI and LMI. In LMI that has been shown in Fig. 1, S_1 and S_n can be selected unidirectional instead bi-directional switches. This topic can be reduced number of IGBTs.

In LMI shown in Fig. 1, always three switches must be turned on in different modes of converter operation. These three switches include one bi-directional and two uni- directional switches that are on at any given time.

Table 1. Comparison of power component requirement.

	DCMI	FCMI	CMI	LMI
IGBTs	6(m-1)	6(m-1)	6(m-1)	3(m+3)
Sources	(m-1)	(m-1)	(3/2)(m-1)	(3/2)(m-1)
M. D	6(m-1)	6(m-1)	6(m-1)	3(m+3)
C. D	6(m-2)	0	0	0
B. C	0	(3/2)(m-1)(m-2)	0	0
Total	19m-25	$(1/2)(3m^2+17m-20)$	(27/2)(m-1)	(1/2)(15m+33)

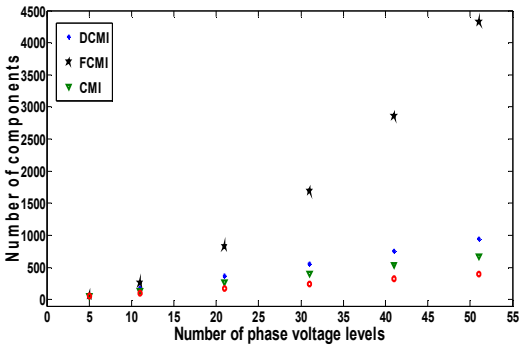
Table 2. Comparison of power switches requirement.

Inverter	DCMI	FCMI	CMI	LMI
Switches	6(m-1)	6(m-1)	6(m-1)	3(m+7)/2

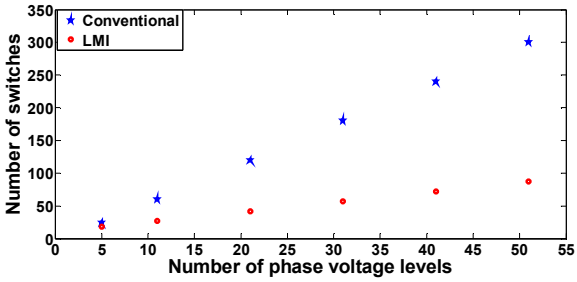
In conventional multilevel inverters, number of on state switches is different with notice to produced voltage levels(*m*) or number of DC sources(*n*). Imagine on-state voltage drop of one IGBT is considered V_D, Table3 compares the on-state voltage drop of switches requirements per single phases among three conventional inverters and LMI. In conventional inverters byincrease voltage levels, on-state voltage drop is increased but in LMI is constant.

Table 3.Comparison of on-state voltage drop

Multilevel	Conventional	LMI
on-state voltage drop	(m-1) V_D	$4V_D$



(a)



(b)

Figure 4. Number of components required in (a)the multilevel converters (b) the only CMI and novel topology.

5. CASE STUDY

Custom power devices are introduced to deal with various power quality problems faced by industrial and commercial customers. These power quality problems could range from simple flicker to long duration power interruptions. Among various power quality problems, voltage sags are more serious. The voltage sags could last as little as a few cycles, still can affect several sensitive loads such as adjustable speed drives and programmable logic controllers. An effective way of controlling the sags is to inject power into the system using DVR. The DVR is device used to guard sensitive loads against voltage disturbances such as voltage sag and swell, where it can inject a controllable voltage (amplitude, frequency and phase shift) in series with the supply voltage to keep the voltage constant at the load terminals [18]-[21]. The basic configuration of the case study is described in Fig.5. The technique of output feedback control is incorporated to determine the switching actions of the inverters. The measured voltages are the inputs to the disturbance identification unit, which gives signals to the control unit. The control unit generates the voltage references. The voltage references are used to generate the modulating signals for the switches of converter. The required active power

to compensate the voltage disturbances is provided by energy storage element (batteries).

The series connection can be performed by transformers. The transformers not only reduce the voltage rating of the inverters but also provide isolation between the inverters and the AC system. In the DVR based LMI, the transformers can be eliminated. The suggested inverter used in DVR does not need any coupling series transformer and has lower cost, smaller size, higher performance and efficiency.

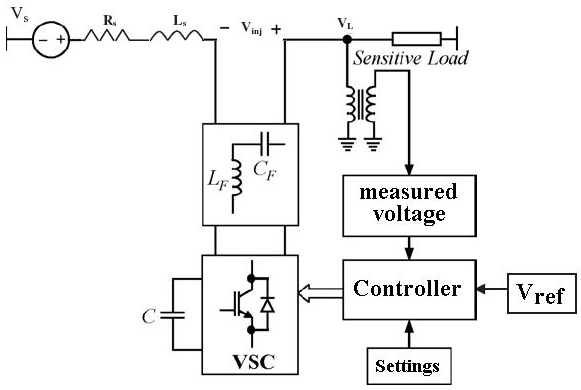


Figure 5. Block diagram of a DVR connected to sensitive load.

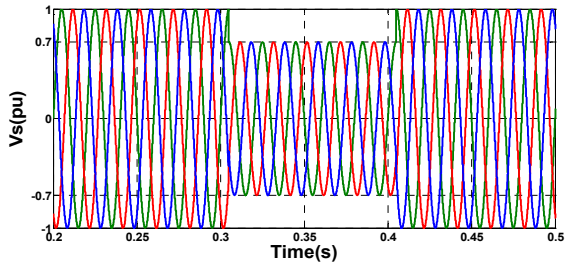
6. SIMULATION RESULTS

To examine the performance of the proposed multilevel inverter in the generation of a desired output voltage, a prototype has been simulated that results have been shown in before parts, also a DVR system as shown in Fig. 5 has been modelled by MATLAB/SIMULINK to study the capability of suggested converter. The system parameters are listed in Table 4. A three-phase 13-level inverter based on the proposed topology according to that one shown in Fig. 2 is simulated and used. In this case, the direct axis, quadratic axis, and zero sequence quantities for three-phase sinusoidal signals (load and reference voltage) are computed by Park transformation [21]. Then the dq load voltages are compared by reference signals and error signals enter to PI controllers. Next the PI controller outputs are transformed to three-phase sinusoidal abc voltage terms and used to generate appropriate DVR gate pulses. To most description refer to [21].

Table 4: Parameters of Simulation

Parameters	Value
Source voltage ($V_{L\ L}$)	400V
DC source	20 V
Power frequency	50 Hz
Load	12.08+ i 9.424778

In case of normal operation conditions, the load voltage is equal to 1 p.u and almost the DVR output voltage is zero. During the voltage disturbance, the DVR output voltage changes to keep the load voltage at 1p.u as in normal operation conditions. It is assumed that during t=0.3048sto t=0.4048sa disturbance in the supply voltage is occurred. Fig. 6 shows the supply voltage, the DVR injection voltage, the load voltage and load current for a case with a 0.3 pu balance three-phase voltage sag which has happened at t=0.3048s. It can be seen that for normal operation conditions DVR output voltage is near zero. However, during the voltage sag DVR injects series voltage so that the load voltage is maintained the same as pre sag. Fig. 7 shows the DVR injection voltage before LC filter for phase 'a'. Harmonic spectrum of injected voltage and calculation of harmonic magnitudes by MATLAB/SIMULINK software are shown in Fig. 8. It is considered that the proposed LMI generates near-sinusoidal (staircase) output voltage and as a result very low harmonic distortion is obtained. THD is 7.65 percent in Fig. 8.



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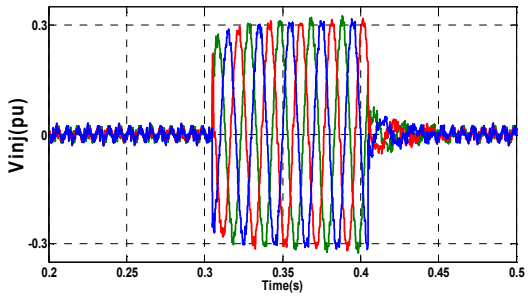

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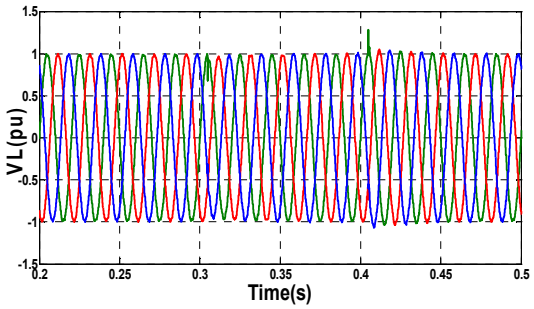

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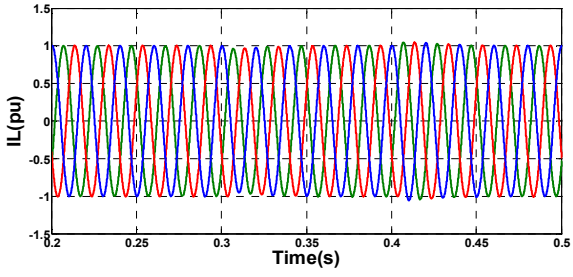

(d)

Figure 6. (a) Supply voltage, (b) the DVR injection voltage, (c) the load voltage and (d) the load current for three-phase balanced voltage sag.

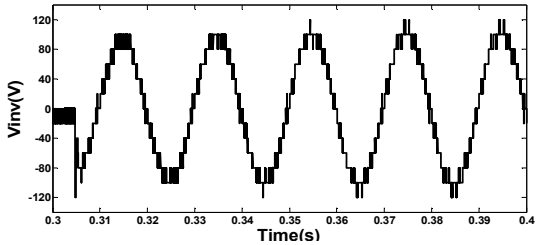

Figure 7. Injected voltage before LC filter for phase 'a' in voltage sag state.

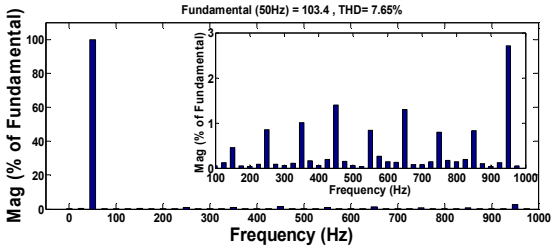

Figure 8. Harmonic spectrums of injected voltage before LC filter for phase 'a' in voltage sag state.

7. EXPERIMENTAL RESULTS

In order to validate the operation of proposed multilevel inverter, nine-level multilevel inverter base on LMI structure that is shown in Fig. 9 is implemented in the laboratory. The overall structure of the experimental set-up is shown in Fig. 10. The main power circuits consist of DC voltage sources, switches and R-L load. The inverter DC sources are supported by separately batteries. The DC sources were supplied by four battery sources that they have a voltage of 10 V. This multilevel generates staircase waveform with maximum 40 V and 50 Hz. The common MOSFET with internal anti-parallel diodes has been used in prototype. The bi-directional switch arrangement consists of two diodes and two MOSFETs. The MOSFETs are the types IRFP460 with voltage and current ratings equal to 500V and 10 A, respectively. The ATMEGA32-8PT microcontroller by ATMELL company has been used to generate the switching patterns. There are several modulation strategies for multilevel inverters. In experimental prototype, the fundamental frequency switching technique has been used [16], [17]. Table V shows the ON switches lookup table. The load is a series R-L with magnitudes 4.5 Ω and 36 mH, respectively. The internal resistance of the inductor is 0.5 Ω.

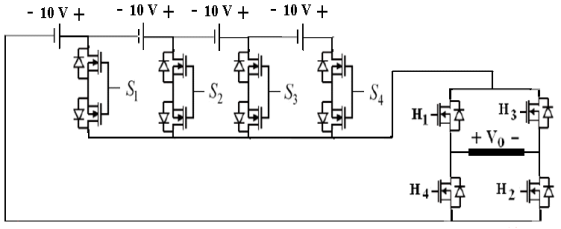

Figure 9. Circuit of nine-level LMI.

Table 5. Lookup Table of Switching

On switches	Vo(V)
S_4 H_1 H_2	40
S_3 H_1 H_2	30
S_2 H_1 H_2	20
S_1 H_1 H_2	10
H_1 H_3 or H_2 H_4	0
S_1 H_3 H_4	-10
S_2 H_3 H_4	-20
S_3 H_3 H_4	-30
S_4 H_3 H_4	-40

Fig. 11 shows the measured output voltage. This is a 50 Hz staircase waveform with amplitude 40 V. The measured output voltage and current have been shown in Fig. 12. As it can be seen, the results verify the ability of proposed inverter in generation of desired output voltage waveform.

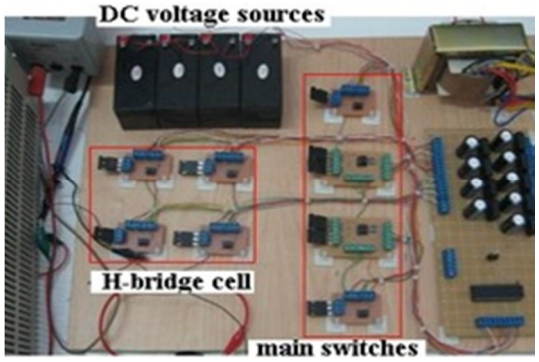

Figure 10. Experimental set-up

Figure 11. The output voltage, 20 V/DIV

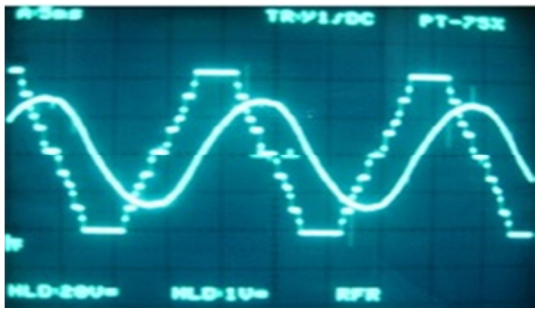

Figure 12. Measured output voltage, 20 V/DIV and resistant voltage (load current), 1*10 V/DIV

CONCLUSION

In this paper a new ladder multilevel inverter has been proposed. The suggested topology needs less switches and gate driver circuits. Therefore, the proposed topology leads to reduction of installation area and cost and has simplicity of control system. Also, in each phase leg of LMI, a set of three switches is on at any given time so LMI has less on-state voltage drop and conduction losses of switches. Based on presented switching algorithm, the multilevel inverter generates near-sinusoidal output voltage and as a result, very low harmonic distortion. The inverter used in DVR does not need any coupling series transformer and has lower cost, smaller size, higher performance and efficiency. Simulation and experimental results verify the validity of the presented idea.

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