

A New Single-Source Cascaded Semi-Bridge Inverter Topology Suitable for Distributed Generation Systems

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ABSTRACT

This paper proposes a single-source cascaded semi-bridge topology so called SSCSB employing one DC input power source and low-frequency single-phase transformers. SSCSB has a two-stage design that includes an input stage and an output stage. The input stage consists of H-bridge voltage source converter. In the output stage, there is a converter, which converts the AC voltage from the input stage to AC sinusoidal voltage. This stage consists of series connected semi-bridge inverters units that use single-phase transformers for isolation and voltage transformation. The proposed circuit configuration can reduce a number of switches and DC source compared with traditional cascaded H-bridge multilevel inverters using separate DC source. Furthermore, it is suitable for applications in the area of distributed generation systems, e. g., solar-cell or fuel-cell in combination with battery energy storage. In this paper, two algorithms for determination of turn's ratio of transformers and switching have been presented, too. To verify the performance of the proposed approach, computer-aided simulations have been provided using MATLAB/ SIMULINK.

Key words: *cascaded semi-bridge, Low frequency transformer, Single DC Source, Distributed Generation.*

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1. INTRODUCTION

Multilevel inverters are increasingly gaining importance for industrial and utility applications due to their numerous inherent beneficial features [1, 2]. Multilevel converters are able to generate output voltage waveforms consisting in a large number of steps. In this way, high voltages can be synthesized using voltage sources with lower levels, with the additional benefit of a reduced harmonic distortion and lower dv/dt in the output voltages. These features have made multilevel converters suitable either for medium-voltage high-power motor drives or for low-voltage high-efficiency conversion systems. Multilevel converter is one of the power electronic converters that have been used in distributed generation (DG).

DG powered by micro sources such as fuel cells, photovoltaic panels and micro turbines, have been gaining popularity among the industry and utilities due to their higher operating efficiencies, improved reliabilities, and lower emission levels. Integrating these generating sources into the existing power system grid, known as distributed energy resources, can provide a more reliable and better quality power to consumers [3-5]. The energy sources used in DG systems usually have different output characteristics and the electricity obtained from these energy sources is normally unregulated and is not in a suitable form to be directly connected to the grids or to the loads for this reason power electronic converters are usually employed to connect these energy sources to the grid or to the loads [6, 7].

Several multilevel inverter topologies have been introduced in the last years, the most important of them being the diode-clamped (DCMI) [8-10], the flying-capacitor (FCMI) [11], and the cascaded H-bridge converter (CMI) [12-14]. The DCMI uses capacitors in series to divide up the DC bus voltage into a set of voltage levels. A FCMI uses a ladder structure of DC capacitors; as a result the voltage on each capacitor differs from the next capacitor. In the FCMI topology, an unacceptable amount of capacitance is required for high voltage levels. The CMI synthesizes a desired voltage from several independent sources of DC voltages. The full-bridge topology with four switches is used to synthesize a three-level voltage. The CMI requires the least number of total main components even though the CMI needs more DC-link capacitors as compared to those needed in the DCMI. Packaged circuit layout is possible in CMI topology, because each level has the same structure, and there aren't extra clamping diodes or voltage-balancing capacitors in CMI circuit, which are required in the DCMI and the FCMI. The number of output voltage levels can then be easily adjusted by changing the number of full bridge inverters.

The main disadvantages of the multilevel inverter are the use of a larger number of semiconductors and a complex control circuitry and needing equilibrate of the voltage at the boundaries of capacitors. One particular disadvantage is the great number of power semiconductor switches needed. Although low voltage rate switches can be utilized in a multilevel inverter, each switch requires a related gate driver circuits. This may cause the overall system to be more expensive and complex. So, in practical implementation, reducing the number of switches and gate driver circuits is very important. Voltage and current ratings of the switches play important roles on the cost and realization of the

multilevel inverter. Peak inverse voltage (PIV) of switch is main parameter that affects on cost of switch.

CMI can operate as symmetric or asymmetric converter [14]. To provide a large number of output steps without increasing the number of DC voltage sources and semiconductor switches, asymmetric multilevel converters (AMC) can be used but PIV of switches in AMC is higher than switches in symmetric multilevel converters. Recently, several multilevel inverter topologies have been developed. Novel topologies of cascaded multilevel inverters using a reduced number of switches, insulated gate driver circuits and voltage standing on switches are proposed in [15-20]. In [15, 16] novel configuration of cascaded multilevel inverters have been proposed. The suggested topologies need fewer switches and gate driver circuits but they require multiple DC sources and some switches of suggested topologies have high PIV. In order to increase the steps in the output voltage, a new topology is recommended in [17], which benefits from a series connection of sub-multilevel converters that uses of bi-directional switches and in [18], the optimal structures for this topology are investigated various objectives such as minimum number of switches and DC voltage sources and minimum standing voltage on the switches for producing the maximum output voltage levels. These topologies require multiple DC sources and some switches of suggested topologies have high PIV. To reduce the number of independent DC sources, methods namely cascaded-transformer-based multilevel inverters were introduced in [19, 20].

Operation of multilevel inverters depends on modulation methods. There are several modulation strategies for multilevel converters. The modulation methods used in multilevel inverters can be classified according to switching frequency. According to its switching frequency they can be classified as: fundamental switching frequency and high switching frequency [21, 22]. A very popular method is the classic carrier based sinusoidal pulse width modulation (SPWM) that uses the phase shifting technique to reduce the harmonics in the load voltage. Multilevel carrier based SPWM uses several triangular (or direct lines) carrier signals, which can be modified in phase (phase shifted SPWM) and or vertical position (level shifted SPWM) in order to reduce the output voltage harmonic content [23-25].

In this paper, an isolated cascaded multilevel inverter is proposed which employs one single DC input power source, isolated single-phase low-frequency transformers and bi-directional switches. The proposed topology is called Single-Source Cascaded Semi-Bridge i.e. SSCSB because uses of single DC source and semi of H-bridge. By the proposed circuit configuration, a number of switches and DC sources can be reduced, compared with traditional cascaded H-bridge multilevel inverters. PIV of switches in proposed structure is low. Existence of transformers gives more flexibility to inverter. Transformers provide isolation between power source and load and voltage transformation. Capacitors, batteries, and other DC voltage sources can be used as the voltage sources of the proposed inverter. Therefore, the SSCSB can be applied to grid connected photovoltaic, fuel cell and etc systems. SSCSB can operate as symmetric or asymmetric converter. In some systems such as power delivery of renewable energy sources, dynamic voltage restorer (DVR), active power filters and etc proposed inverter

may be available. SSCSB is a suitable power electronic interface between renewable energy sources and load or grid, with the capabilities of voltage regulation and galvanic isolation between renewable energy sources and load or grid. This object is studied in this paper as case study. Switching algorithm is like SPWM but reference wave forms are sin wave and absolute of sin wave. At each instant, absolute sin wave and sin wave are compared with carriers signal (direct lines). To verify the performance of SSCSB, computer-aided simulations carried out using MATLAB/ SIMULINK.

2. PRESENTED TOPOLOGY

Figure 1 shows a typical circuit diagram of SSCSB with single power source, which is the object of this paper.

As can be seen from Figure 1, this is a two-stage design that includes an input stage and an output stage. The bi-directional switches with capability of blocking voltage and conducting current in both directions are needed in SSCSB. There are several arrangement can be used to create such a bi-directional switch.

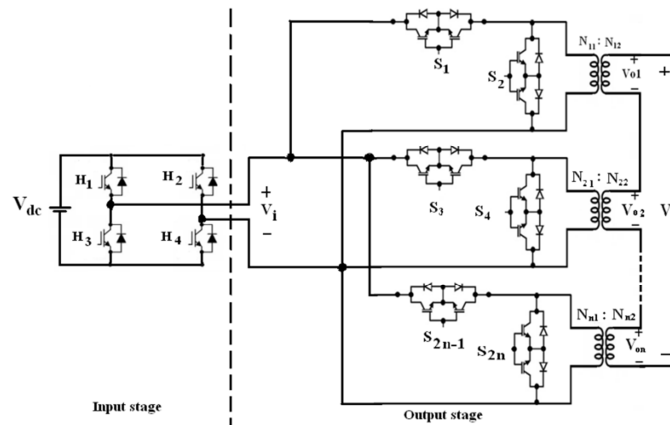


Figure 1. Circuit diagram of proposed DC/AC converter (SSCSB).

The common emitter anti-parallel IGBT with diode pair arrangement and one type gate driver circuit have been shown in Figure 2. In the input stage, there is a single-phase low frequency converter, which converts the input DC voltages to AC voltage with fundamental frequency. The input stage consists of H-bridge voltage source converter. The DC voltage from the input power source is fed to the H-bridge- converter and is modulated to a fundamental frequency square voltage. The H-bridge topology with four switches is used to synthesize a three-level square-wave output voltage waveform. Table 1 indicates the values of H-bridge for states of switches H₁-H₄. Then the square voltage is provided to the output stage. From positive part of output voltage of H-bridge converter is used as DC sources in half period and from negative part of output voltage is used as DC sources in second half period. Zero level can be used in some structures that would be explained in the following

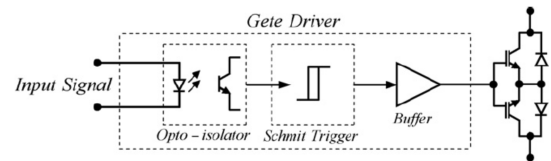


Figure 2. Bi-directional switch and one type gate drive

In the output stage, there is a converter, which converts the AC voltage from the input stage to AC sinusoidal voltage. This AC/AC converter has two part, bi-directional switches and single phase transformers. The AC/AC converter made up from some basic units. Figure 3 shows the suggested basic unit for a sub-multilevel AC/AC converter. The basic unit consists of an AC voltage source, two switches S₁ and S₂ and single phase transformer. Table 1 indicates the values of V_{O1} for states of switches S₁ and S₂. The basic unit shown in Figure 3 can be cascaded as shown in Figure 1. The output voltages of basic units are cascaded through the secondary of the transformers.

Table 1. Values of V_{O1} for states of switches S_1 and S_2

state	Values of V_i	Switches state		V_{O1}
		S_1	S_2	
1	V_{dc}	on	off	$\frac{N_{11}}{N_{12}} V_{dc}$
2	V_{dc}	off	on	0
3	$-V_{dc}$	on	off	$-\frac{N_{11}}{N_{12}} V_{dc}$
4	$-V_{dc}$	off	on	0

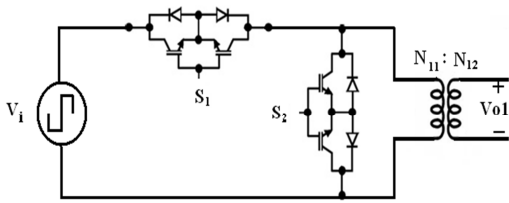


Figure 3. Suggested basic unit for a sub-multilevel inverter.

The H-bridge cell produces voltage with two polarities in two half period and output voltage of H-bridge cell or zero voltage is given to transformers by bi-directional switches. Careful to Table 1, symmetry voltage levels are produced by same switches. Zero level could be produced with H-bridge cell or bi-directional switches.

Output phase voltage of proposed inverter is achieved by summing the output voltages of basic units. Output phase voltage of is obtained by:

$$V_O = V_{O1} + V_{O2} + \dots + V_{On} \tag{1}$$

The maximum of output phase voltage is:

$$V_{O_{max}} = \sum_{i=1}^n \frac{N_{i2}}{N_{i1}} V_{dc} \tag{2}$$

The amplitude of the output voltage is determined by the input DC voltage source and turn ratio of the transformers. This topology requires one DC source and it may be available in some systems such as STATCOM, active power filter and etc that use DC-link capacitor. For example, one active power filter has been designed based on cascaded multilevel

converter in [26]. The cascaded topology requires a separate DC-link capacitor for each cell, requiring a complex control strategy to regulate the voltage across each capacitor but SSCSB has one DC-link capacitor and control of one DC-link capacitor is simple in application as active power filter. This topology has much significance for higher rated converters used for high or medium voltage distribution system, as they require transformers to increase the inverter output voltage at the desired level. In some systems such as power delivery of renewable energy sources, DVR and etc, SSCSB may be available.

In SSCSB, the number of switches is reduced and each switch requires one gate driver. Reduction of gate driver is obtained with reduction of switches number. One type of gate driver circuit has been shown in Figure 2.

Voltage and current ratings of the switches in a multilevel inverter affect on the cost and realization of the multilevel inverter. In the cascaded H-bridge multilevel inverters, the voltage standing on switches or PIV for switches is given by the following equation:

$$PIV_{sw,i} = V_i \tag{3}$$

$PIV_{sw,i}$ is switch PIV that put on in i th H-bridge cell and V_i is voltage sources of i th H-bridge cell. In asymmetric state, DC voltage sources of all H-bridge cells are not the same so switches PIV in different H-bridge cells are not the same and PIVs are affected by DC sources selection algorithms. In SSCSB, switches PIV in asymmetric state are the same as symmetric state and are given by:

$$PIV_{sw} = V_{dc} \tag{4}$$

SSCSB can operate in symmetric or asymmetric state to obtain uniform step voltage. In SSCSB to obtain asymmetric multilevel converters turn ratio of transformers are selected in

different value. Several strategies can be used for determination of transformers turn ratio in SSCSB. In the following, we propose two different methods for determination of turn ratio of transformer which are used in the proposed multilevel inverter. In the first method all turn ratio of transformers in Figure 1 are the same and in the second method to obtain uniform step AMC, the turn ratio of the transformers are proposed to be chosen according to a geometric progression with a factor of two.

If all turn ratios of transformers are the same, the inverter is known as symmetric multilevel inverter. The maximum number of phase voltage levels is given by:

$$m = 2n + 1 \tag{5}$$

n, m are the number of transformer and the maximum number of levels of phase voltage, respectively. The maximum output voltage is:

$$V_{O_{max}} = nV_{dc} \tag{6}$$

If all turn ratios of transformers are the same the structure of SSCSB that is shown in Figure 1 can be changed as Figure 4. In the structure that has been shown in Figure 4 number of switches has reduced. The number of switches is given by (7) and (8):

$$SW = 2n + 2 \tag{7}$$

$$SW = m + 1 \tag{8}$$

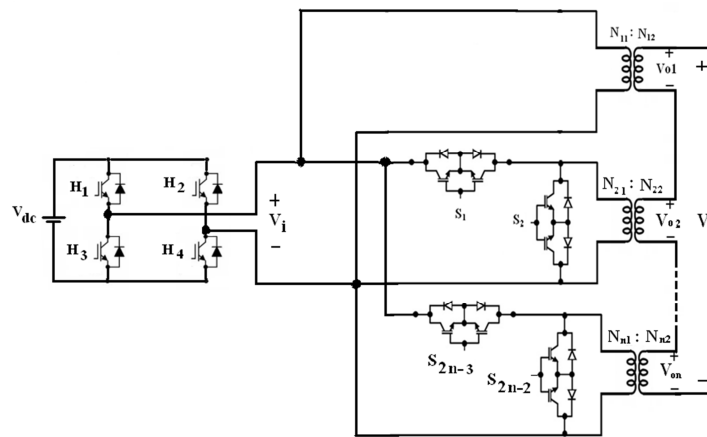


Figure 4. Structure of SSCSB in symmetric state.

The second method for determination of the turn ratio of the transformers is in progression with a factor of two (Binary).

$$N_{i1} = p \quad N_{i2} = q \quad i = 1, 2, \dots, n \tag{9}$$

$$N_{i2} = 2^{i-1}q \quad i = 2, 3, \dots, n \tag{10}$$

Maximum number of output voltage levels and maximum output voltage are:

$$m = 2^{n+1} - 1 \tag{11}$$

$$V_{O_{max}} = (2^n - 1)V_{dc} \tag{12}$$

In the asymmetric SSCSB the number of switches is given by:

$$SW = 2n + 4 \tag{13}$$

$$SW = 2 \frac{\text{Ln}(m+1)}{\text{Ln}2} + 2 \tag{14}$$

In asymmetric state the input stage of SSCSB can be changed as Figure 5. By this structure the number of switches has reduced. The number of switches is given by (15) and (16):

$$SW = 2n + 2 \tag{15}$$

$$SW = 2 \frac{\text{Ln}(m+1)}{\text{Ln}2} \tag{16}$$

In recent years, multilevel inverter and its modified control schemes using cascaded transformers have been presented to obtain high quality output voltage with minimized number of DC sources and switching devices [19, 20]. These multilevel inverters can be used in symmetric or asymmetric states. Asymmetric multilevel inverters increase the number of output voltage levels based on the different turn ratio of the cascaded transformers.

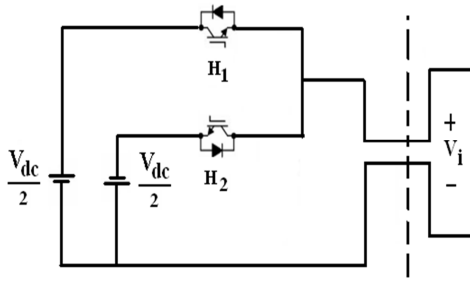


Figure 5. Second structure of input stage in asymmetric state.

However, the different turn ratio of cascaded transformers means the unbalance of power distribution, different

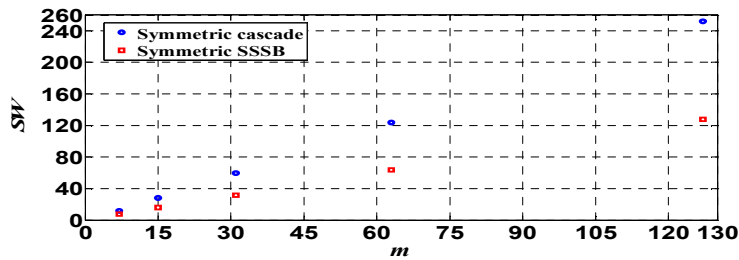
saturation conditions of the transformers and difference of power ratings of switching devices [20].

In asymmetric multilevel inverters geometric progression with a factor of two or three are two famous methods that the DC voltages sources or turn ratio of cascaded transformers are proposed to be chosen according to their [15, 17-20].

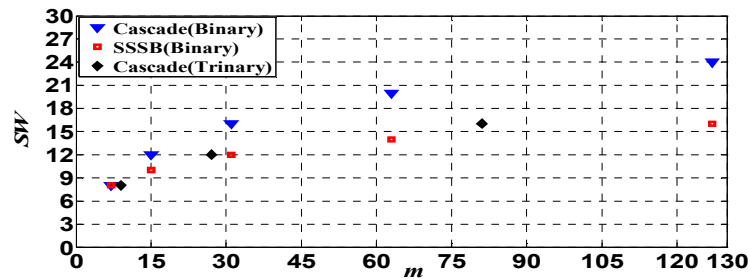
Table 2 shows a comparison of the number of switches between cascaded transformer-based multilevel inverters topology [19, 20] and SSCSB in the symmetric and asymmetric states when inverters produce m levels voltage. Table 2 shows that the suggested topology needs fewer switches in order to generate the same levels of output voltages. Figure 6 shows a comparison of the number of switches between the cascaded-transformer-based multilevel inverters and suggested SSCSB according to Table 2.

Table 2: Comparison of switches number.

	cascaded transformers			SSCSB	
	Symmetric	Binary	Trinary	Symmetric	Binary
SW	$2(m - 1)$	$4 \frac{\text{Ln}(m+1)}{\text{Ln}2} - 4$	$4 \frac{\text{Ln}(m)}{\text{Ln}3}$	$m + 1$	$2 \frac{\text{Ln}(m+1)}{\text{Ln}2} + 2$



(a)



(b)

Figure 6. Comparison of switches number, (a) symmetric state and (b) asymmetric state.

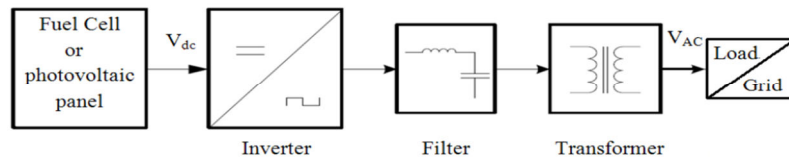


Figure 7. Power delivery in FC system.

3. SSCSB and DISTRIBUTED GENERATION

Distributed Generation powered by micro sources have been gaining popularity among the industry and utilities due to increased energy utilization, global pollution awareness and improved reliabilities. Among the micro source, fuel cells and photovoltaic panels are attractive due to their modular, efficient, and environmentally friendly performance [15]. Since the fuel cells and photovoltaic panels deliver DC power, it must be inverted and stepped-up to be able to use for applications. A suitable power electronic interface is required between fuel cells and photovoltaic panels with load or grid, with the capabilities of voltage regulation and galvanic isolation between fuel cells and photovoltaic panels and load or grid. In this paper, voltage of fuel cells and photovoltaic panels has been supposed constant DC voltage. The SSCSB can be used in energy conversion according to this strategy. Step-up voltage and galvanic isolation between DC source and load or grid are given by transformers that have been used in SSCSB structure and voltage regulation achieve by proper switching and regulation turns ratio of transformers. SSCSB can be replaced instance of inverter, filter and transformer in Figure 7. If number of voltage levels increased, filter can be eliminated in system.

4. SIMULATION RESULTS

Two types of SSCSB have been simulated with MATLAB/SIMULINK. To examine the performance of the

proposed multilevel inverters in the generation of a desired output voltage, prototypes are simulated that results are shown in two parts. The detailed system as shown in Figure 1 and Figure 4 has been modeled to study the operation of SSCSB. In this section, the modulation method of the proposed inverter is explained on the 7 and 15-level inverter, too. According to algorithms of determination turn ratio of transformers, simulations have two part, symmetric state and asymmetric state. The multilevel inverters feeds R-L load. The load is a series R-L with magnitudes 24.16Ω and 60mH, respectively. The voltage of DC power source is 50 V.

4.1. Symmetric State

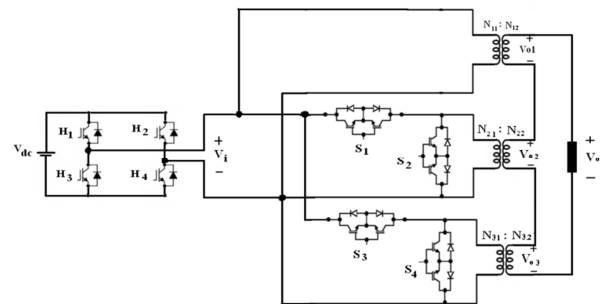


Figure 8. SSCSB with three single-phase transformers in symmetric state.

Table 3. Look-up table of a 7-level inverter.

State	High Switching pulse	Level	ON switches
1	P ₃	+3 V _{dc}	H ₁ , H ₄ , S ₁ , S ₃
2	P ₂	+2 V _{dc}	H ₁ , H ₄ , S ₁ , S ₄
3	P ₁	+ V _{dc}	H ₁ , H ₄ , S ₂ , S ₄
4	Z	0	H ₁ , H ₂ , S ₂ , S ₄
5	P ₁	- V _{dc}	H ₂ , H ₃ , S ₂ , S ₄
6	P ₂	-2 V _{dc}	H ₂ , H ₃ , S ₁ , S ₄
7	P ₃	-3 V _{dc}	H ₂ , H ₃ , S ₁ , S ₃

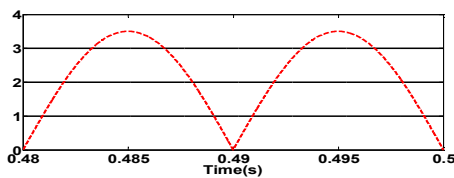
Figure 8 shows SSCSB with three single phase transformers. The turn's ratios of transformers are the same and converter is symmetric.

Operation of 7-level inverter is shown in Figure 9. Modulation waveforms for switching for the proposed topology are shown in Figure 9(a) and 9(b). The principle of the modulation is based on a comparison of a sinusoidal reference and its absolute waveforms, with vertically shifted carrier waveforms. The carriers are direct lines that are shifted vertically. The frequency of sine reference defines output voltage frequency. The frequency of sine reference is 50 Hz. The principle of switching H-bridge is described in Figure 9(b) with under conditions:

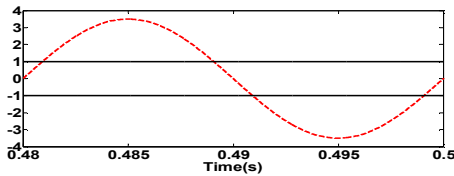
Condition 1: $\sin \text{ wave} \geq 1$, then H_1 and H_4 are turned on.

Condition 2: $\sin \text{ wave} \leq -1$, then H_2 and H_3 are turned on.

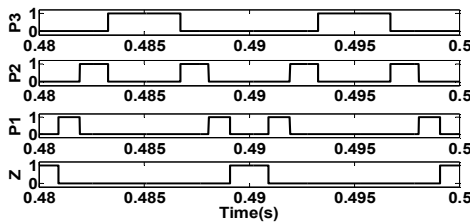
Condition 3: $-1 < \sin \text{ wave} < 1$, then H_1 and H_2 are turned on and zero level can be produced.



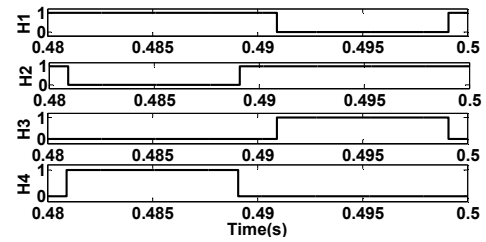
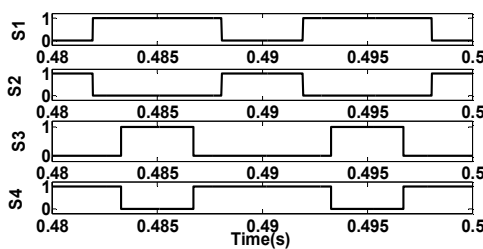
(a)



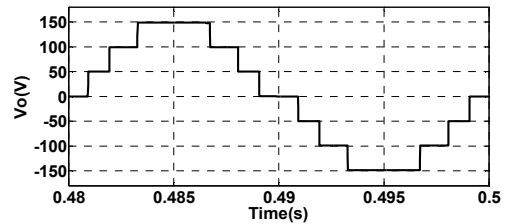
(b)



(c)



(d)



(e)

Figure 9. Operation of 7-level SSCSB (a) modulation signal of bi-directional switches (b) modulation signal of H-bridge cell (c) Switching pulses (d) gates signals (e) output phase voltage.

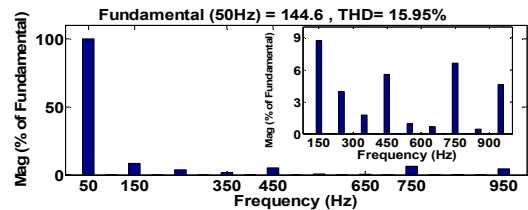


Figure 10. FFT analysis of output voltage.

Switching pulses are produced from comparison among absolute of sine wave and carriers as shown in Figure 9(a). For example:

If $2 \leq \text{absolute of sin wave} < 3$, then P_2 is produced.

Switching pulses are shown in Figure 9(c). Gate signals of H-bridge cell and bi-directional switches are shown in Figure 9(d). These gate signals are generated with notice to lookup Table. 2 that shows ON state switches. Output voltage is shown in Figure 9(e). FFT analysis of output voltage is shown in Figure 10. Total harmonic distortion (THD) has been calculated 15.95% by MATLAB/SIMULINK.

4.2. Asymmetric State

Figure 11 shows SSCSB with three single-phase transformers that using transformers with turn ratio of binary algorithm ($\frac{N_{11}}{N_{12}} = 1, \frac{N_{21}}{N_{22}} = 2$ and $\frac{N_{31}}{N_{32}} = 4$), 15-level inverter can be obtained. By controlling the switching of the SSCSB, 15 discrete voltage levels (from $-7V_{dc}$ to $7V_{dc}$) can be generated. Operation of 15-level inverter is shown in Figure 12.

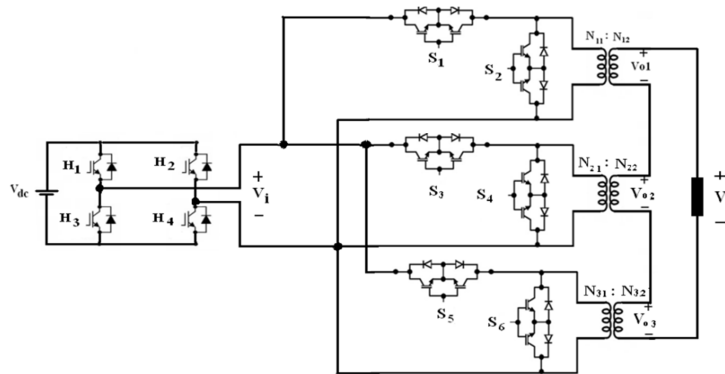


Figure 11. SSCSB with three single-phase transformers in asymmetric state.

Table 4. Look-up table of 15-level inverter.

State	High Switching pulse	Level	ON switches
1	P ₇	+7 V _{dc}	H ₁ , H ₄ , S ₁ , S ₃ , S ₅
2	P ₆	+6 V _{dc}	H ₁ , H ₄ , S ₂ , S ₃ , S ₅
3	P ₅	+5 V _{dc}	H ₁ , H ₄ , S ₁ , S ₄ , S ₅
4	P ₄	+4 V _{dc}	H ₁ , H ₄ , S ₂ , S ₄ , S ₅
5	P ₃	+3 V _{dc}	H ₁ , H ₄ , S ₁ , S ₃ , S ₆
6	P ₂	+2V _{dc}	H ₁ , H ₄ , S ₂ , S ₃ , S ₆
7	P ₁	+V _{dc}	H ₁ , H ₄ , S ₁ , S ₄ , S ₆
8	Z	0	H ₁ , H ₄ , S ₂ , S ₄ , S ₆
9	P ₁	- V _{dc}	H ₂ , H ₃ , S ₁ , S ₄ , S ₆
10	P ₂	-2 V _{dc}	H ₂ , H ₃ , S ₂ , S ₃ , S ₆
11	P ₃	-3 V _{dc}	H ₂ , H ₃ , S ₁ , S ₃ , S ₆
12	P ₄	-4V _{dc}	H ₂ , H ₃ , S ₂ , S ₄ , S ₅
13	P ₅	-5 V _{dc}	H ₂ , H ₃ , S ₁ , S ₄ , S ₅
14	P ₆	-6 V _{dc}	H ₂ , H ₃ , S ₂ , S ₃ , S ₅
15	P ₇	-7 V _{dc}	H ₂ , H ₃ , S ₁ , S ₃ , S ₅

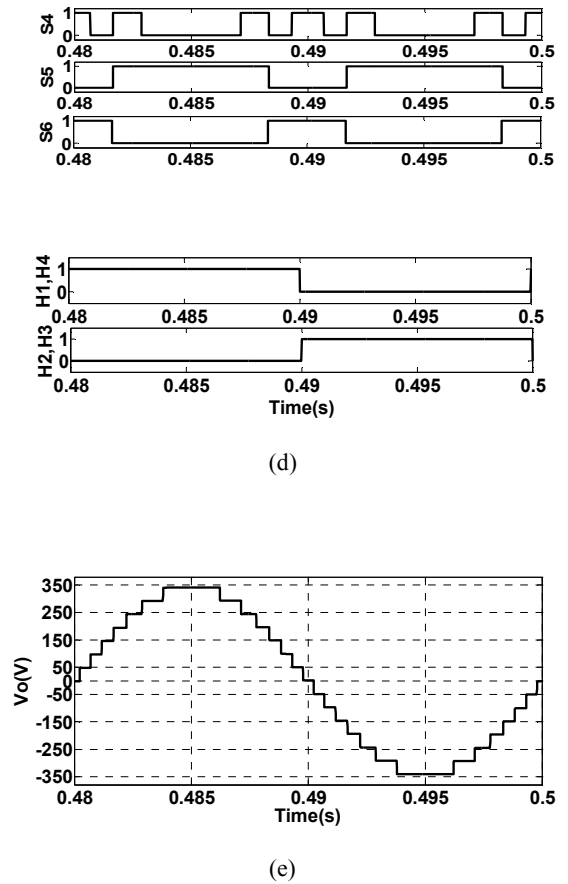
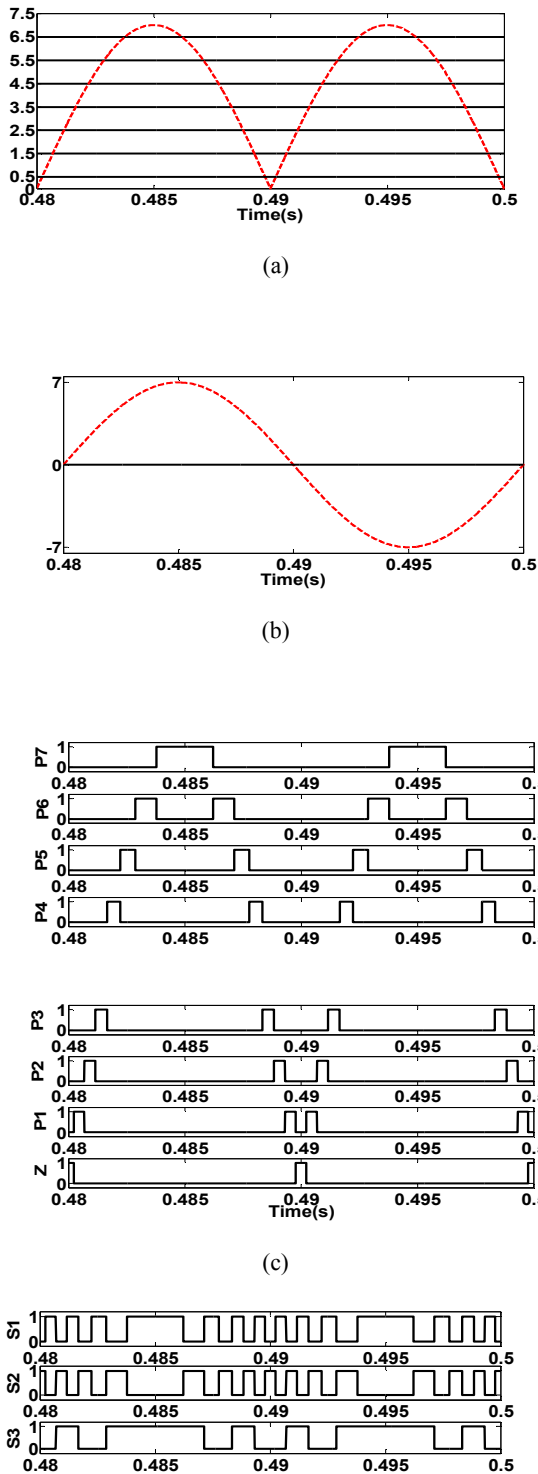


Figure 12. Operation of 15-level SCSB (a) modulation signal of bi-directional switches(a) modulation signal of H-bridge cell (e) Switching pulses (d) gates signals (e) output phase voltage.

Figure 13. FFT analysis of output voltage.

The principle of switching H-bridge is described with under conditions:

Condition 1: $\sin \text{ wave} \geq 0$, then H_1 and H_4 are turned on.

Condition 2: $\sin \text{ wave} < 0$, then H_2 and H_3 are turned o

Zero level isn't produced by H-bridge cell and it's created by bi-directional switch.

Switching pulses are produced from comparison among absolute of sine wave and carriers as the same symmetric state. Table 4 shows the ON switches lookup table of 15-level inverter. FFT analysis of output voltage is shown in Figure 13. It is considered that THD is 5.38%. The multilevel converter generates staircase (near-sinusoidal) output voltage and as a result, very low harmonic distortion.

CONCLUSION

This paper proposed a cascaded multilevel inverter employing low-frequency single-phase transformers, bi-directional switches and a single DC input power source. The proposed circuit configuration can reduce a number of DC sources. The suggested topology needs less switches and gate driver circuits. Based on presented switching algorithm, the SSCSB inverter generates staircase output voltage and as a result, very low total harmonic distortion is obtained. The proposed structure may be available in some system same as power delivery in renewable energy sources. Simulation results show that the proposed inverter can produce the desired output voltage.

REFERENCES

- [1] Lai, J. S. and Peng, F. Z., "Multi-level converters—A new breed of power converters", *IEEE Trans. Ind. Appl.*, 32 (1997) 509–517.
- [2] Rodriguez, J., Lai, J.S. and Peng, F.Z., "Multilevel Inverter: A Survey of Topologies, Controls, and applications", *IEEE Trans. on Industrial Electronics*, 49(4):724-738, (August 2002).
- [3] Hajizadeh, A. and Golkar, M. A. ., "Intelligent Power Management Strategy of hybrid Distributed Generation System", *International Journal of Electrical Power and Energy Systems*, 29: 783–795, (2007).
- [4] McDermott, T. E. and Dugan, R. C., "Distributed generation impact on reliability and power quality indices", Conf. Rec. *IEEE Rural Electric Power - D3-D3_7*, (2002).
- [5] Bojoi, R., Cerchio, M., Gianolio, G., Profumo, F. and Tenconi, A., "Fuel Cells for Electric Power Generation: Peculiarities and Dedicated Solutions for Power Electronic Conditioning Systems", *EPE Journal*, 1(16): 44-45, (2006).
- [6] Blaabjerg, F., Chen, Z. and Kjaer, S. B., "Power electronics as efficient interface in dispersed power generation systems", *IEEE Trans. on Power Elect.*, 5(19): 1184-1194, (2004).
- [7] Daher, S., Schmid, J. and Antunes, F. L. M., "Multilevel inverter topologies for stand-alone PV systems", *IEEE Trans. Industrial Electronics*, 55(7): 2703-2712, (July 2008).
- [8] Marchesoni, M. and Tenca, P., "Diode-clamped multilevel converters: A practicable way to balance DC-link voltages", *IEEE Tran. Ind. Electron.* 49(4): 752–765, (August 2002).
- [9] Chen, A. and He, X., "Research on hybrid-clamped multilevel-inverter topologies", *IEEE Trans. Ind. Electron.*, 53(6): 1898–1907, (December 2006).
- [10] Bendre, A., Venkataramanan, G., Rosene, D. and Srinivasan, V., "Modeling and design of a neutral-point voltage regulator for a three-level diode-clamped inverter using multiple-carrier modulation", *IEEE Trans. Ind. Electron.*, 53(3): 718–726, (Jun 2006).
- [11] Wilkinson, R. H., Mouton, H. D. T. and Meynard, T. A., "Natural balance of multicell converters", *IEEE-PESC*,: 1307-1312, (2003).
- [12] Corzine, K., "Operation and Design of Multilevel Inverters", *Developed for the Office of Naval Research*, December. 2003.
- [13] Peng, F. Z., McKeever, J. W. and Adams, D. J., "Cascade multilevel inverters for utility applications", *IEEE-IECON*, 437–442, (1997).
- [14] Rech, C. and Pinheiro, J. R., "Hybrid Multilevel Converters: Unified Analysis and Design Considerations", *IEEE Trans. Ind. Electron.* 54: 1092-1104, (2007).
- [15] Babaei, E. and Hosseini, S. H., "New cascaded multilevel inverter topology with minimum number of switches", *Energy Conversion and Management*, 50: 2761-2767, (2009).
- [16] Banaei M. R. and Salary, E., "New multilevel inverter with reduction of switches and gate driver", *Energy Conversion and Management*, 52(11): 1129-1136, (2011).
- [17] Babaei, E. and Hosseini, S. H., Gharehpetian, G.B., Tarafdar Haque, M. and Sabahi, M., "Reduction of dc voltage sources and switches in asymmetrical multilevel converters using a novel topology", *Electric Power Systems Research*,:1073-1085, (2007).
- [18] Babaei, E., "Optimal Topologies for Cascaded Sub-Multilevel Converters", *Journal of Power Electronics*, 10(3): 251-261, (May 2010).
- [19] Barcenas, E., Ramirez, S., Cardenas, V. and Echavarria, R., "Cascaded multilevel inverter with only one dc source", *VIII IEEE Inter. Tech. Proc. CIEP*,: 171-176, (2002).
- [20] Park, S. J., Kang, F. S., Cho, S. E. Moon, C. J. and Nam, H. K., "A novel switching strategy for improving modularity and manufacturability of

- cascaded-transformer-based multilevel inverters”, *Electric Power Syst. Res.*, 74: 409–416, (2005).
- [21] Leon, J. I., Vazquez, S., Kouro, S., Franquelo, L. G., Carrasco, J. M. and Rodriguez, J., “Unidimensional modulation technique for cascaded multilevel converters”, *IEEE Transactions on Industrial Electronics*, 56(8): 2981–2986, (August 2009).
- [22] Rodriguez, J., Kouro, S., Rebolledo, J. and Pontt, J., “A reduced switching frequency modulation algorithm for high power multilevel inverters”, *Power Electronics Specialists Conference, PESC. IEEE 36th*, :867–872, (June 2005).
- [23] Hava, A. M., Kerkman, R. J. and Lipo, T. A., “Carrier-based PWM-VSI Over modulation Strategies: Analysis, Comparison, and Design”, *IEEE Transactions on Power Electronics*, 13(4): 674-689, (July 1998).
- [24] McGrath, B. P. and Holmes, D.G., “Multicarrier PWM Strategies for Multilevel Inverters”, *IEEE Trans. Ind. Electron*, 49(4): 858-867, (August 2002).
- [25] Liu, H., Tolbert, L. M., Khomfoi, S., Ozpineci, B. and Du, Z., “Hybrid cascaded multilevel inverter with PWM control method”, *IEEE Power Electronics Specialists Conference 2008*, : 162-166, (June 2008).
- [26] Zhoua, G., Wub, B. and Xuc, D., “Direct power control of a multilevel inverter based active power filter”, *Electric Power System Research*, 77: 284–294, (2007).