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Research Article

Effect of measurement frequency on admittance characteristics in Al/*p*-Si structures with interfacial native oxide layer

Muhammed Can OZDEMIR[1], Omer SEVGİLİ[2], Ikram ORAK[2], Abdulmecit TURUT[3]

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[1]*Department of Nanoscience and Nanoengineering, Institute of Graduate Education, Istanbul Medeniyet University 34700, Istanbul, Turkey*

[2]*Vocational School of Health Services, Bingöl University, 12000, Bingöl, Turkey*

[3] *Department of Engineering Physics, Faculty of Engineering and Natural Sciences, Istanbul Medeniyet University, 34700, Istanbul Turkey*

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*****Corresponding author e-mail: amecit2002@yahoo.com

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ABSTRACT

Al/*p*-Si/Al diodes with interfacial native oxide layer were formed. Their frequency induced admittance-voltage measurements were made. The frequency-dependent density distribution of interface states has been determined from the corrected characteristics by considering the series resistance effect which masks the interface trap loss. The majority carrier density corresponding to the depletion and inversion parts of the C^{-2}-V curve, was determined 1.82 x 10^{14} and 4.48 x 10^{14} cm^{-3} at 1000 kHz, respectively. The fact that the carrier density obtained from the inversion part of the plot is higher than that obtained from the depletion part can be related to the increase in the density of negative space charge in the depletion region.The value of Φ_{CV} was determined as 0.95 eV from the same plot. Interface state density decreased from 4.31 x 10^{12} $eV^{-1}cm^{-2}$ at 100 kHz to 7.30 x 10^{11} eV^{-1} cm^{-2} at 1000 kHz, because the interface charges do not follow the *ac* signal and do not contribute to capacitance values in high frequencies.

Keywords: Metal-semiconductor contacts, MIS diodes, interface states, capacitance characteristics, conductance characteristics.

Doğal oksit arayüzey tabakalı Al/*p*-Si yapılarda admittans karakteristikleri üzerine ölçüm frekansının etkisi

ÖZ

Arayüzey doğal oksit tabakalı Al/*p*-Si/Al diyotlar imal edildi. Onların frekans bağımlı admittans voltaj ölçümleri de yapılmıştır. Arayüz durumlarının frekans bağımlı yoğunluk dağılımı, ara yüzey tuzak kaybını maskeleyen seri direnç etkisi dikkate alınarak düzeltilmiş admittans datalarından belirlenmiştir. C^{-2}-V eğrisinin tükenim ve tersinim kısımlarına karşılık gelen çoğunluk taşıyıcı yoğunluğu 1000 kHz'de sırasıyla 1.82 x 10^{14} and 4.48 x 10^{14} cm^{-3} olarak belirlenmiştir. Eğrinin tersinim kısmından elde edilen taşıyıcı yoğunluğunun, tükenim kısmından elde edilen kinden daha fazla olması, tükenim bölgesindeki negatif uzay yükü yoğunluğunun artmasıyla ilişkilendirilebilir. Φ_{CV}'nin değeri aynı grafikden 0,95 eV olarak belirlenmiştir. Arayüzey hallerinin yoğunluğu 100 kHz'de 4.31 x 10^{12} $eV^{-1}cm^{-2}$ 'den 1000 kHz'de 7.30 x 10^{11} eV^{-1} cm^{-2}, ye düşmüştür, çünkü arayüzey yükleri *ac* sinyalini takip edememektedir ve yüksek frekanslarda kapasitans değerlerine katkıda bulunamamaktadır.

Anahtar Kelimeler: Metal-yarıiletken kontaklar, MIS diyotlar, arayüz halleri, kapasitans özellikleri, iletkenlik özellikleri.

1. INTRODUCTION

The quality and understanding of the metal/semiconductor (MS) devices such as bipolar transistors, photodiodes, rectifiers, MS field-effect transistors (MESFETs) and metal/oxide layer/semiconductor FETs (MOSFETs) depend on the electrical properties and the production of metal/semiconductor contacts. In general, in metal/insulating layer/semi-conductor (MIS) device fabrication, the rectifying contact metals may cause some damage onto the semiconductor substrate surface and thus an insulating or oxide layer deposition on the surface of substrate may prevent possible damage.[1-7]

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The available defects at the interfaces of metal-semiconductor (MS) or metal-insulating layer-semiconductor (MIS) or metal-oxide layer-semiconductor (MOS) structures are generally called the interface traps or states. The charges in the interface states can capture or emit electrons (holes), and thus interact with the conduction (valence) band of semiconductor. The interface state energy or density distribution can be estimated through the energy loss resulting from changes in their occupancy by small variations of gate voltage. Majority carriers are captured or emitted and subsequently changes in occupancy of interface trap and energy loss emerge. The energy lost during capture of the majority carriers is taken up by phonons, heating the lattice. This energy loss is measured as an equivalent parallel interface state conductance. In addition to an energy loss associated with capture and emission, interface traps also can hold a charge for some time after capture. That is, interface traps store charge. Therefore, there will be an interface state charge capacitance proportional to interface trap level density. The total energy loss depends on the interface trap density and its relaxation time.[1-11]

Herein, Al/SiO_2/*p*-Si/Al MIS diodes were fabricated. The SiO_2 native oxide has formed on the clean Si wafer surface exposed to clean room air. The capacitance-voltage (*C-V*) and conductance-voltage (*G-V*) characteristics of the MIS diode were measured at various frequencies. The interface state density depending on frequency was calculated from the corrected *C-V* and *G-V* characteristics taking into account the series resistance effect which masks the interface trap loss.[1-8] Intrinsic surface states existing at the semiconductor surface before rectifying metal contact have an important role in Schottky barrier formation. The dangling band of the Si surface can be saturated by the native SiO_2 thin layer. The termination with SiO2 thin layer causes the variety of notable properties of the silicon surface after exposing to clean room air. Electronically, it is significantly inactive with a largely reduced density of surface states in Si energy band gap.[4-10]

2. PREPERATION OF SAMPLES AND MEASUREMENTS

Al/SiO_2/*p*-Si/Al MIS diodes were prepared using *p*-type Si(100) with resistivity of 1-10 Ω-cm and average free carrier concentration of 2.28 x 10^{15} cm^{-3}. The low resistivity ohmic back contact to *p*-type Si(100) wafers was made using Al, followed at 570°C for 3 min under nitrogen gas. The native oxide layer on the clean front surface of the wafer with ohmic contact formed because the wafer was exposed to clean room air at room temperature before evaporating Al Schottky contacts. The front surface of pieces cut from the wafer with ohmic back contact was chemically cleaned using the RCA cleaning procedure and finally has been rinsed in de-ionized water for 30 s. Prepare RCA bath; 5 parts water (H_2O), 1 part 27% ammonium hydroxide (NH_4OH), 1 part 30% hydrogen peroxide (H_2O_2). Soak wafer in RCA-1 bath at 70°C for 15 min. DI rinse and blow dry. Clean up, dispose wastes (Werner Kern developed the basic procedure in 1965 while working for RCA, the Radio Corporation of America; The RCA Corporation is a major American electronics company, which is founded as the Radio Corporation of America in 1919).[11] The Schottky contacts have been formed onto the front surface of slices by evaporation of Al dots with diameter of about 1.75 mm (diode area = 2.41 x 10^{-2} cm^2). All evaporation processes were performed in a turbo molecular fitted vacuum coating unit at about 10^{-6} mbar. The *G-V* and *C-V* characteristics were measured by a HP model 4192A *LF* impedance analyzer, respectively, at room temperature and in the dark.

3. RESULTS AND DISCUSSION

3.1. Impedance characteristics of the diodes

Figures 1a and 1b represent the forward and reverse bias capacitance against voltage curves at various frequencies and 300 K. For the forward branch case of the MIS diode, a negative voltage is applied to the Al/SiO_2 side that is, to the gate metal, with respect to the *p*-Si/Al side, a negative charge will exist on the top of Al Schottky contact metal, and an electric field is induced into the *p*-Si semiconductor substrate. Thus, the majority carrier holes would experience a force toward the native oxide/semiconductor interface and an accumulation layer of holes at the native oxide/semiconductor contact corresponds to the positive charge on the bottom Al Schottky contact metal of the MIS capacitor. We will return to the descriptions of the capacitance-voltage characteristics later, that is, depletion region and inversion layer in the reverse branch of the MIS diode.

Figures 1a and 2 represent the forward and reverse bias *C-V* and *G-V* curves at various frequencies and 300 K. The formed accumulation region corresponds to the saturation region in about 7.5-10 V range at forward branch at 1000 kHz in Figure 1a. The capacitance value of Cox = 422 pF is the capacitance of the native oxide layer at 1000 kHz, and the thickness value of the oxide layer can be calculated using Cox value. The capacitance of the interfacial layer of a MIS diode is given in Eq. (1).

$$C_{0x} = \frac{\varepsilon_{0x}\varepsilon_0 A}{d} \qquad (1)$$

where ε_{0x} = 3.9 is the permittivity of the interfacial SiO_2 native oxide layer[12] and d is its thickness, respectively, ε_0 is the permittivity of free space and A is the area of Al Schottky contact.

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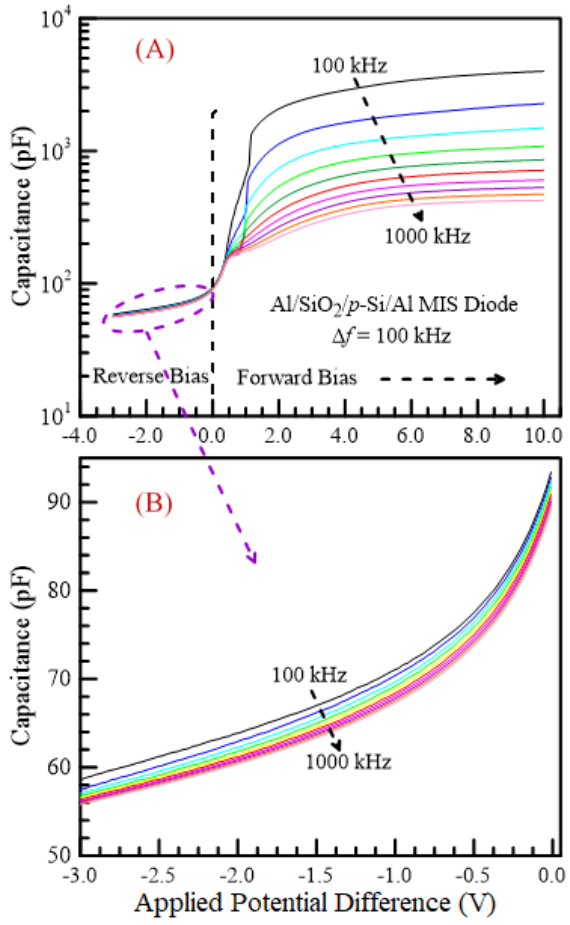

Figure 1. Frequency induced capacitance-voltage characteristics.

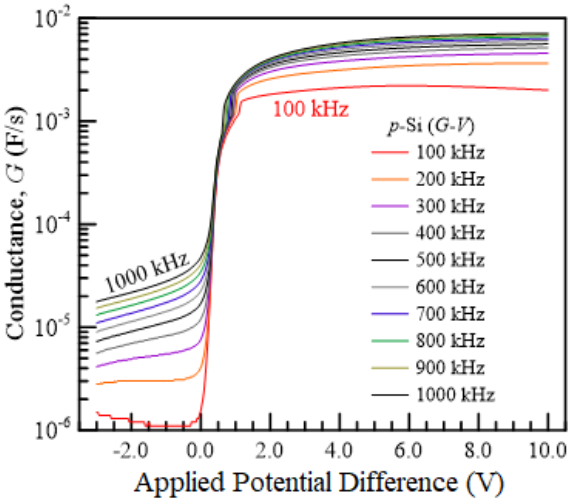

Figure 2. Frequency induced conductance-voltage characteristic.

A value of 65.80 nm for the thickness of the interfacial layer was found using C_{0x} value in Eq. (1).

However, due to the series resistance effect, we cannot obtain the actual value of the thickness. The series resistance can cause a serious error in the extraction of the interfacial properties. To avoid this error, a correction should be applied to the measured admittance before the desired information is extracted.[4,12] The series resistance R_S and interfacial layer capacitance C_{0x2} for the MIS structure can be calculated from Equations (2-4):[4]

$$R_s = \left[\frac{G_{ma}}{(wC_{ma})^2 + G_{ma}^2}\right] \quad (2)$$

$$C_{ma} = \frac{C_{0x}}{1 + (wR_sC_{0x})^2} \quad (3)$$

$$C_{0x2} = C_{ma}\left[1 + \frac{C_{ma}^2}{(wC_{ma})^2}\right] \quad (4)$$

where $w = 2\pi f$ is the angular frequency of the *ac* signal and f is the frequency in Hz or s^{-1}. C_{ma} = 422 pF and G_{ma} = 7.10 x 10^{-3} F/s are the measured conductance and capacitance in the strong accumulation region in Figures 1a and 2. Eq. (4) was obtained from Equations (2) and (3). The C_{0x2} and R_S values were found as 3448 pF and 123 Ω from Equations (2) and (4) for the accumulation region, respectively. This corrected capacitance value of C_{0x2} = 3448 pF is eight times larger than the capacitance value of C_{0x} = 422 pF. A corrected value of 8.06 nm for the thickness of the interfacial layer SiO_2 was obtained using value of C_{0x2} = 3448 pF in Eq. (1). As can be seen from explained above, the series resistance completely masks interface trap loss, and especially the equivalent parallel conductance is much more sensitive to the series resistance than capacitance. Therefore, it can be said that the correction made considering the series resistance is particularly important in conductivity measurements.[4,12,13-16]

The free carrier density was determined from the slopes of the C^{-2}-V curves obtained using Eq. (5) (Figure 3).

$$N_A = \frac{2}{q\varepsilon_s\varepsilon_0(dC^{-2}/dV)A^2} \quad (5)$$

Furthermore, the barrier height Φ_{CV} of the MIS diode from the C^{-2}-V curves can be determined using Eq. (6).

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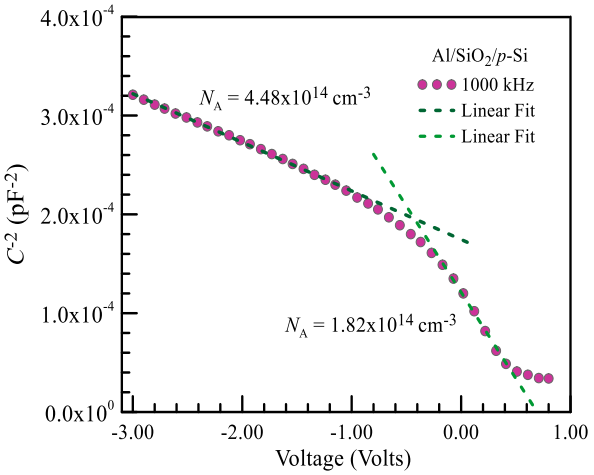

Figure 3. C^{-2} versus voltage curve at 1000 kHz and 300 K.

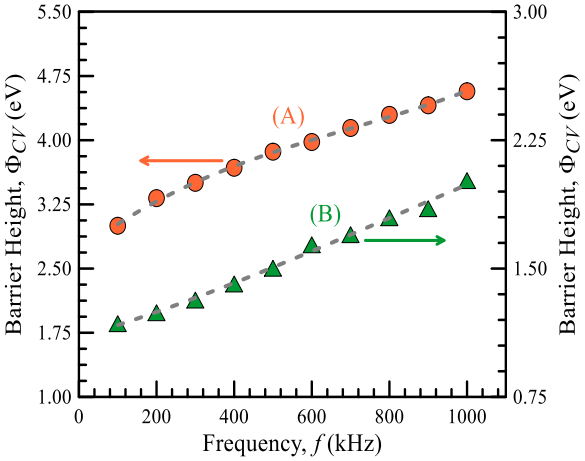

Figure 4. Barrier height versus frequency plot: a) The barrier height values from the C^{-2}-V curves corresponding to inversion region ranged from -1.0 V to -3.0 V of the C^{-2} - V curves at each frequency, b) The barrier height values calculated from the C^{-2}-V curves corresponding to the deplation region ranged from 0.0 V to -1.0 V at each frequency.

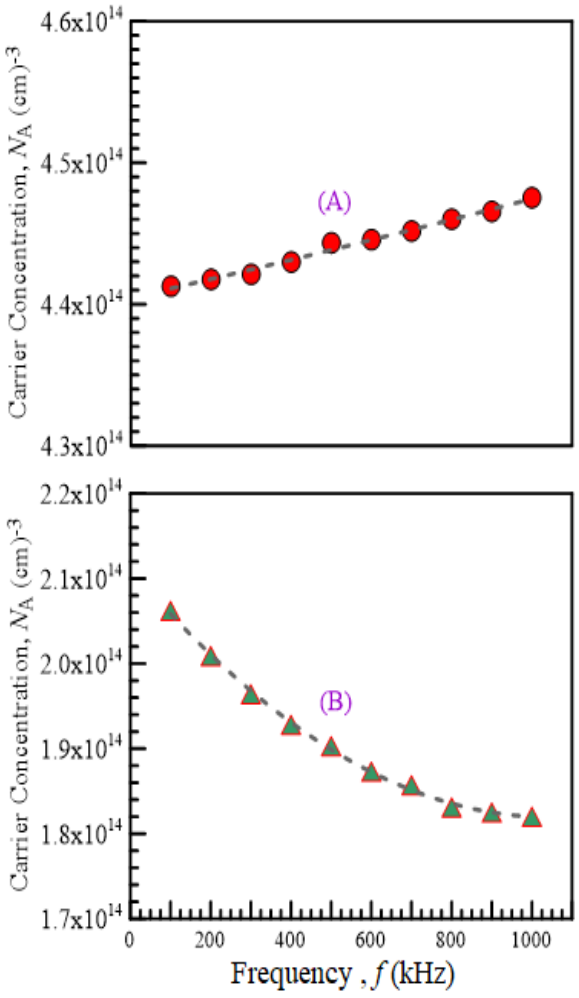

Figure 5. Carrier concentration versus frequency plots: a) from inversion region ranged from -1.0 V to -3.0 V of the C^{-2}-V curves at each frequency, b) from deplation region ranged from 0.0 V to -1.0 V of the C^{-2}-V curves at each frequency.

$$C^{-2} = \frac{2(V_{D0} + V_0)}{q\mathcal{E}_s\mathcal{E}_0 N_A A^2} \qquad (6)$$

where q is the electronic charge, $\mathcal{E}_s$ is dielectric constant of the semiconductor substrate, the diffusion potential is given by $V_{D0} = (\Phi_{CV} - V_p)$, V_p is the potential difference between Fermi level and the valance band maximum in the neutral region of p-type semiconductor in the energy band diagram of the metal/p-type semiconductor rectifying contact, and it is stated by Eq. (7).

$$V_p = kT\ln\left(\frac{N_V}{N_A}\right) \qquad (7)$$

where N_V = 1.04 x 10^{19} cm^{-3} is the state density in the valance band.[12]

Now let us consider the case when a still larger positive voltage is applied to the top metal gate of the MIS diode. A larger negative charge in the MIS diode indicates a larger induced space charge region. Thus, the surface of the p-type Si semiconductor is inverted from a p-type to an n-type semiconductor, and an inversion layer of electrons forms at the native oxide layer/semiconductor interface. This region corresponds to the part ranged from -1.0 V to -3.0 V of the C^{-2} - V curve in Figure 3. A majority carrier hole density of 4.48 x 10^{14} cm^{-3} was calculated from the inversion layer part of the C^{-2}-V curve using Eq. (5).

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Again, let us deal with the *C*-*V* and *G*-*V* curves in Figures 1a and 2, the reverse branch case of the MIS diode, when a positive voltage is applied to the Al/SiO_2 side, that is, to the gate metal, with respect to the *p*-Si/Al side; a positive charge will exist on the top Al Schottky contact (gate metal) in this case, majority carrier holes will experience a force away from the native oxide layer/semiconductor interface. As the holes are pushed away from the Al/SiO_2 interface, a negative space charge induced depletion region is created because of the fixed ionized acceptor atoms. The depletion region ranges from 0.0 V to -0.6 *V* in Figure 4 which shows C^{-2} versus *V* curve at 1000 kHz and 300 K. The majority carrier holes density of the *p*-Si substrate can be from the part corresponding to the depletion region of the C^{-2} - *V* curve. A carrier concentration value of 1.82 x 10^{14} cm^{-3} was calculated from this part of the C^{-2}-*V* curve from Eq. (5).

A value of 0.25 V for V_p was obtained from the equation above. For example, the value of Φ_{CV} can be determined from the fit to the linear C^{-2}-*V* curve corresponding to depletion region in (0.0 V) – (-0.6 *V*) range in Figure 3. Thus, the intercept of the linear C^{-2} versus *V* plot with *V* axis was obtained as $V_0 = V_{D0} =$ 0.70 V, and $\Phi_{CV} = (V_p + V_{D0}) =$ 0.95 V. This calculation was repeated for the linear C^{-2}-*V* curve corresponding to depletion and inversion region at each frequency and thus, Figure 4 is plotted.

For the MOS devices, corrected capacitance and equivalent parallel conductance at a given frequency can be written as follows:[4]

$$C_c = \frac{[G_m^2 + (wC_m)^2]C_m}{(wC_m)^2 + a^2} \quad (8)$$

$$G_c = \frac{[G_m^2 + (wC_m)^2]C_m}{(wC_m)^2 + a^2} = \frac{(wC_cR_s)^2}{1 + (wC_cR_s)^2} \quad (9)$$

where $a = G_m - [G_m^2 + (wC_m)^2]R_s$ and C_m and G_m are the capacitance and the equivalent parallel conductance measured across the terminals of the MOS capacitor at each frequency, that is, C_m and G_m values come from the experimental *C*-*V* and *G*-*V* curves in Figures 6 and 8. Figures 7 and 9 illustrate the corrected and non-corrected experimental forward and reverse bias *C*-*V* and *G*-*V* characteristics at 500 kHz frequency and 300 K temperature, as an example, respectively.

The R_s value from the accumulation region using Eq. (2) at each frequency is used in these calculations. The absence of a peak in the non-corrected *G*-*V* curves means that the series resistance produced the dominant loss and completely masked the interface trap loss. The series resistance effect are clearly apparent in Figures 7 and 9, and the greatest error in the capacitance occurs in accumulation and a portion of the depletion region.[4,12,13-17] As can be seen, it is not possible to neglect series resistance in each case. Therefore, the series resistance must be measured and applied as a correction to the measured admittance.[4,12,13-17]

The following Hill-Coleman equation[13] was used to determine the density distribution of the interface states,

$$N_{ss} = \frac{2}{qA}\frac{(G/\omega)_m}{\{[(G/\omega)_m/C_{ox2}]^2 + (1 - C_m/C_{ox2})^2\}} \quad (10)$$

where C_m and G_m/w are the measured or experimental capacitance and conductance peak values at given each frequency.

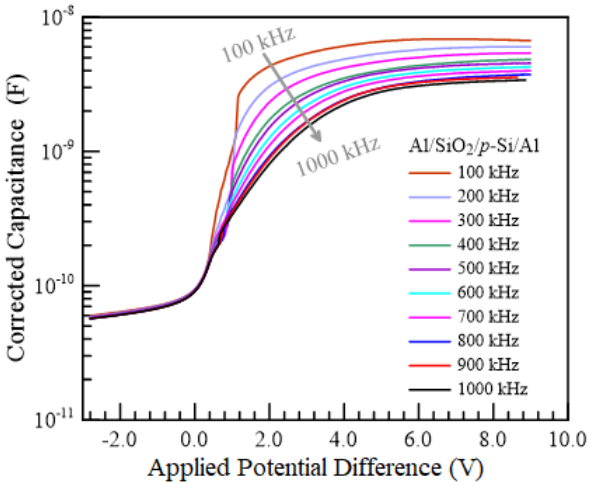

Figure 6. Corrected capacitance versus voltage curves at different frequencies and 300 K.

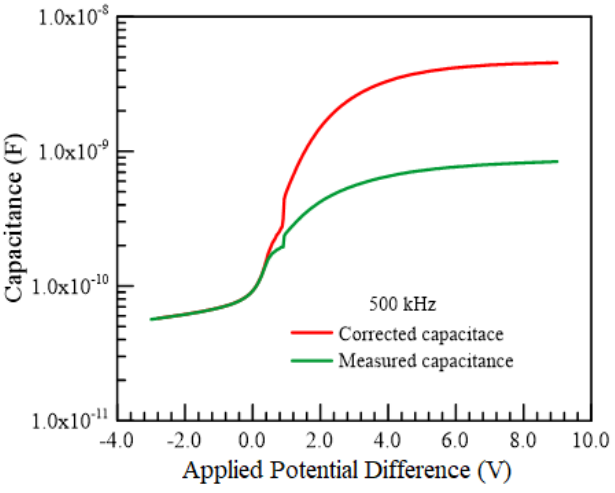

Figure 7. Corrected and uncorrected or measured capacitance versus voltage curves at 500 kHz and 300 K.

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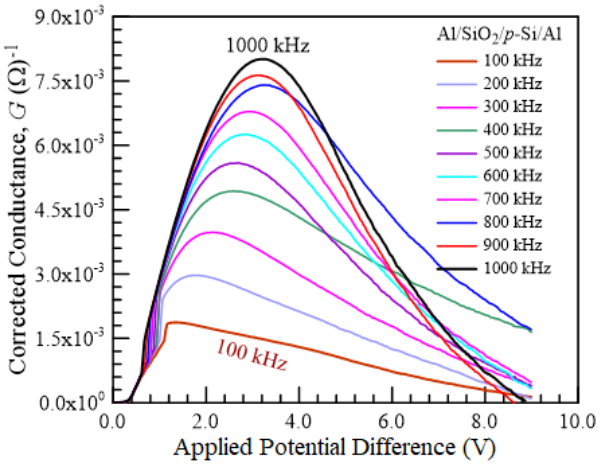

Figure 8. Corrected conductance versus voltage curves at different frequencies and 300 K.

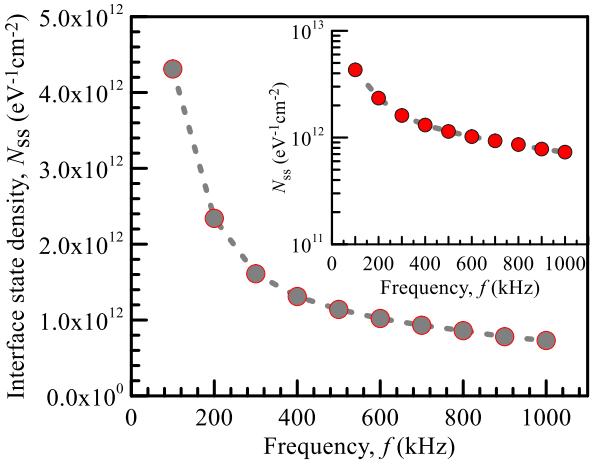

Figure 10. Interface state density versus frequency curves at 300 K, inset: The same plot is shown in semi-logarithmic scale.

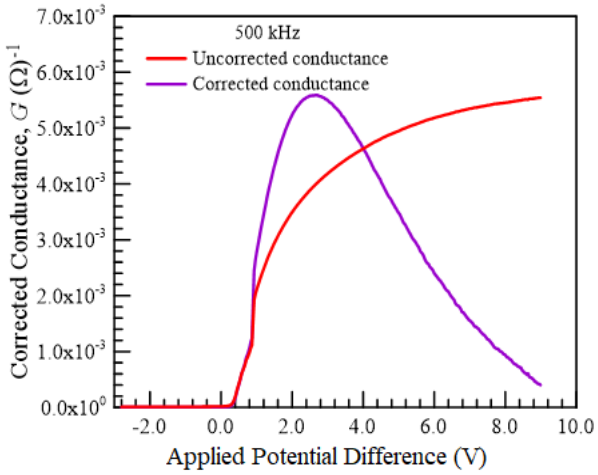

Figure 9. Corrected and uncorrected conductance versus voltage curves at 500 kHz and 300 K.

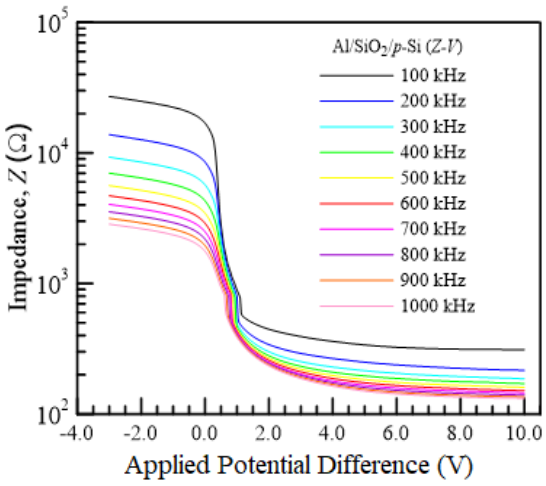

Figure 11. Frequency induced Impedance-Voltage characteristics of the diode.

The oxide layer capacitance C_{ox2} is the value calculated from Eq. (4). Frequency dependent interface state density distribution, N_{ss}, plot is presented in Figure 10 and it can be seen that the N_{ss} depends strongly on the frequency. As can be seen from Figure 10, the N_{ss} increases with decreasing frequency because it can follow the *ac* signal and it contributes capacitance values in low frequencies. It can be clearly from Figure 3 that the capacitance has higher value in lower frequency than that in the higher frequencies. Hence, this confirms that the high capacitance in lower frequencies can be attributed to excess capacitance resulting from the N_{ss} values.[4,12,13-17] Thereby, interface state density decreased from 4.31 x 10^{12} eV^{-1} cm^{-2} at 100 kHz to 7.30 x 10^{11} eV^{-1} cm^{-2} at 1000 kHz. Figure 11 illustrates frequency induced impedance (Z) versus voltage characteristics of the Al/SiO_2/*p*-Si/Al MIS diode. The impedance of a circuit is described as the ratio of the phasor voltage and the phasor current measured in ohms. We note that the impedance modulus is so high under reverse-bias. The impedance of the device increased with decreasing frequency at a given voltage.

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4. CONCLUSIONS

The majority carrier density corresponding to the depletion and inversion parts of the C^{-2}-V curve, at 1000 kHz, for the Al/SiO_2/*p*-Si/Al MIS diode has been determined 1.82 x 10^{14} and 4.48 x 10^{14} cm^{-3}, respectively. The fact that the carrier density from the inversion part becomes more than that from the depletion part may be attributed to increase of the negative space charge density in the depletion region due to the charges in the inversion region that the surface of the *p*-type Si semiconductor is inverted from a *p*-type to an *n*-type semiconductor. The value of Φ_{CV} can be determined a value of 0.95 V. With an increase in frequency, interface state density decreased from 4.31 x 1012 eV-1 cm-2 at 100 kHz to 7.30 x 1011 eV-1 cm-2 at 1000 kHz, since the interface charges cannot obey the ac signal and cannot contribute to capacitance values in high frequencies.

Conflict of interests

Authors declare that there is no a conflict of interest with any person, institute, company, etc.

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ORCID

https://orcid.org/0000-0002-4002-7967 (M. C. Ozdemir)

https://orcid.org/0000-0003-1740-1444 (O. Sevgili)

https://orcid.org/0000-0003-2318-9718 (I. Orak)

https://orcid.org/0000-0002-4664-4528 (A. Turut)