Model Predictive Control of an Indirect Matrix Converter with Active Damping Capability

M. GOKDAG and O. GULBUDAK

Abstract—**In this paper, a model predictive control (MPC) scheme is proposed to control indirect matrix converter (IMC), which is used for three phase-to-three phase direct power conversion without any intermediate energy storage component between them. The aim in the control of current source rectifier (CSR) stage of IMC is generally to have unity power factor with relatively low total harmonic distortion (THD). The aim in the control of voltage source inverter (VSI) stage is to be able to synthesize sinusoidal load currents with desired peak value and frequency. Imposed source current MPC technique in abc frame is used for the rectifier stage. An active damping technique without requiring the selection of an appropriate value for fictitious damping resistor is also included in the proposed control scheme in order to mitigate the resonance phenomenon of lightly damped input LC filter to suppress the higher order harmonics in supply currents. Load currents with desired peak and frequency are also obtained by imposing sinusoidal currents in abc frame. Two different cost functions are combined into a single cost function without any weighting factor since both error terms are in the same nature. The switching state that minimizes this pre-defined cost function among the 24-valid switching combinations of IMC is selected and applied to converter. The proposed model predictive control with active damping method shows a good performance in terms of THD levels in supply currents even at low current demands from supply side. The proposed strategy guarantees unity power factor operation and draws sinusoidal load currents at desired peak and frequency.**

Index Terms—**Indirect matrix converter, ac-ac power conversion, model predictive control, active damping.**

I. INTRODUCTION

MATRIX CONVERTER (MC) was introduced as an alternative to back-to-back (AC-DC-AC) converter which requires high energy storage components in the DC link prone to failure. The structure of the matrix converter which does not require any electrolytic capacitors allows it to operate with high reliability and high-power densities. The main advantages of the matrix converter can be listed as follows:

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MC inherently has bidirectional power flow, it is capable to simultaneously transform amplitude and frequency of the three-phase voltage system, sinusoidal input current and output voltage can be synthesized with suitable modulation techniques such as space vector modulation, and input power factor can be independently controlled. Because of these advantages, a great interest from academia and industry focused onto the application of matrix converters in order to realize highly compact three-phase AC drives for industrial and military systems [1], [2].

A sub-family of MCs is called as Indirect MC (IMC) having same advantages together with easier control and safe commutation and it was proposed in [3]. Main objectives in control of IMC is to obtain sinusoidal output currents and sinusoidal input currents with unity power factor. Modulation techniques, control strategies and the digital implementation of the PWM switching patterns were first research attentions on IMC [4]–[6]. Another research perspective on IMC was the reduction of the number of semiconductor switches used, and the family of sparse matrix converter was proposed [7].

In order to avoid relatively complex modulation techniques that can achieve unity power factor at input side and generate sinusoidal waveforms at load side, model predictive control technique can be a good candidate since it has simpler concept, better dynamic response, and easier implementation thanks to recent advancements in digital signal processor technologies [8], [9]. In [10]–[12] a model predictive control approach, whose cost function employs errors in output currents in αβ frame and input reactive power to meet power-factor performance objective, is proposed. The use of weighting factors in a tailored cost function is unavoidable since it contains different control objectives. In [10], the cost function is updated to include active damping term in order to alleviate the resonance phenomenon of the lightly damped input LC filter. The high-pass filtered active damping current term calculated in the dq synchronous frame from the filter capacitor voltages is somewhat scaled as an output current variable and then subtracted from the output current reference. As a result, the active damping term is indirectly included in the control scheme despite the cost of extra calculation for transformation. The best switching combination among the 24 switching states that gives positive voltage for dc link is selected and applied to converter for next sampling period. A dead time compensation approach is also taken into account to minimize the adverse effect of relatively late updated control signals due to long-lasting calculations [12]. In [13], same model predictive approach as in [10]–[12] is proposed for

four-leg IMC which is used to obtain secure operation for unbalanced load conditions. The predictive approach for four-leg IMC has 48 switching states to be searched.

In [14], in addition to conventional predictive approach for MCs, a cost term is added to cost function to reduce the number of commutations and consequently it decreases the switching losses. In [15], a method to decrease the computational burden of model predictive approach is proposed. This technique eliminates the prediction of three-phase currents at sampling instant (k+1), and reduces the number of reactive power predictions and cost function evaluation from 25 to 10.

In [16]–[18], imposed source current model predictive control is another approach which is used in grid-connected topologies to simultaneously control the input power demands and power factor objective. In this technique, grid side of the power stage is forced to have sinusoidal source currents synchronous or asynchronous according to the power factor demand. The complicated part of this approach is to generate sinusoidal current references which generally require additional PLL environments in hardware or software. These references and source current predictions based on input filter model are then employed in cost function to find best switching combination.

In [2], [19]–[21], predictive control strategies operating at fixed switching frequency of IMC are proposed in order to prevent resonances in the input filter of the matrix converter which is the result of variable switching frequency due to the use of conventional model predictive control. The technique is called as modulated MPC (M2PC) and the cost function is designed to choose optimal adjacent vectors and their corresponding duty cycles. It basically emulates the space vector modulation (SVM) using MPC. In [21], two methods were proposed. First one is the combination of predictive current control with reactive power minimization and active damping technique whereas the second one imposes a sinusoidal source current synchronized with grid voltage to minimize input instantaneous reactive power. The use of fixed switching frequency operation combined with these methods further enhance the performance on the mitigation of input filter resonance. In [20], an indirect approach for M2PC, where two separate cost functions are evaluated for rectifier and inverter sides individually and the use of weighting factors are avoided, is adopted whereas a single cost function to control the IMC is evaluated in [10]–[12].

Predictive approach based on direct power control which only employs active and reactive power errors in cost function can be used in various three-phase power converters without requiring sector information for related control variable in order to synthesize sinusoidal waveform with desired power factor [22]–[24]. In [9], a predictive power control of IMC with active damping is proposed for only resistive load conditions. The errors in load active power, load reactive power, and input reactive power at the instant of (k+2)th are employed in cost function by considering delay compensation. The use of weighting factor is avoided since the cost function employs objectives which have equal importance on the performance. The active damping technique is introduced to the control scheme by injecting related damping power terms to the load active power reference and input reactive power reference. In [22], Direct Power Control (DPC) with two-step prediction to compensate the control delay is used for active front end rectifier. A PI controller is used to generate input active power reference from the error of DC link voltage. In [23], a similar DPC approach is also applied to current source rectifier used in a battery charge application from three-phase grid. An active damping technique to mitigate input filter resonance is included in the control with a simple novel approach where high-pass filtered damping power term is injected into input active power reference.

In this study, a model predictive control approach with predictive active damping method is proposed to control IMC. No weighting factor is used for the reason that both error terms introduced in the cost function are in the same nature. For the rectifier stage, predictive approach based on imposed sinusoidal source currents is adopted and a novel active damping method, without requiring any pre-calculation of optimal fictitious damping resistor value, is included in the control of rectifier side. For inverter stage, the conventional predictive current control is used. The proposed control scheme is tested by using Matlab/Simulink and collected simulation data show that proposed control method provides reliable operation. Since MPC method has repetitive operations, it is well-suited to implement on a Field-Programmable Gate Arrays (FPGAs) which has pipelining capability. A scheme that shows how the algorithm can be implemented on an FPGA device is also presented.

When this study is compared with the similar counterparts from literature that focus onto any grid connected topology such as IMC and ac-dc current source rectifier with MPC approach, the main contribution of this paper is that, the proposed control method uses a unique direct technique which brings less extra computational burden for reducing THD at the input current. Against to that, [2], [19]–[21] propose modulated MPC emulating the SVM to suppress the input current pollution, and it increases the computational complexity since it requires the selection of optimal adjacent vectors and their corresponding duty cycles. When the computational burden increases, the sampling period increases, and as a direct consequence of that the available bandwidth decreases. In fact, the M2PC used in these studies does not include active damping. It only tries to bypass the problem by keeping the switching frequency away from the resonance frequency of the input filter. However, if any harmonic close to resonance frequency interferes into the system, the M2PC cannot damp it. The use of fixed switching frequency may also increase the switching losses when it is higher than the required, whereas MPC has variable switching frequency according to the operating conditions. While the techniques presented in [10], [23], [25] requires the selection of optimal value for fictitious damping resistor whereas the proposed damping technique in this study does not. In [10], [26], the damping current term is somehow translated into an output variable, and damping effect is obtained via the output

variables in an indirect manner by increasing the computation burden.

The outline of the paper is as follows. The IMC topology and system model are given in section 2. Complete control scheme of MPC is described in section 3. In section 4, reference generation block for supply current peak value is detailed and PI compensator design steps are explained. The details of novel active damping method are presented in section 5. An implementation scheme on how the proposed control is paralleled on an FPGA is provided in section 6. Simulation waveforms and several comparison results in terms of the important evaluation criteria, Total Harmonic Distortion (THD), under different operating conditions of supply and load current are provided in section 7. The study is concluded with section 8.

II. SYSTEM AND PREDICTION MODELS

A. Indirect Matrix Converter Topology

The IMC, shown in Fig. 1, is composed of bidirectional current source rectifier (CSR) and voltage source inverter (VSI) stages. The rectifier side is connected to the grid via a LC filter to prevent the interference of unwanted frequency harmonics to the utility and contains six bidirectional switches. The inverter stage is a full-bridge three-phase circuit whose output is connected to a three-phase RL load.

B. Rectifier Model

The current source rectifier has 9 switching states and three of them gives zero output voltage ($v_{DC}=0$), and another three of them provides positive dc link voltage ($v_{DC}>0$). Since the inverter side requires positive dc link voltage, only three switching combinations among nine switching states can provide positive dc voltage at any sampling instant. Valid switching states, corresponding input and output variables for rectifier side are provided in Table I.

The dc link voltage, v_{DC}, and input current of the rectifier, $\mathbf{i_i}$, are defined by (1) and (2).

$$v_{DC} = \begin{bmatrix} S_{r1} - S_{r2} & S_{r3} - S_{r4} & S_{r5} - S_{r6} \end{bmatrix} \begin{bmatrix} v_{ia} \\ v_{ib} \\ v_{ic} \end{bmatrix} \tag{1}$$

$$= \mathbf{T_{CSR}} \mathbf{v_i}$$

and

$$\begin{bmatrix} i_{ia} \\ i_{ib} \\ i_{ic} \end{bmatrix} = \begin{bmatrix} S_{r1} - S_{r2} & S_{r3} - S_{r4} & S_{r5} - S_{r6} \end{bmatrix}^T i_{DC} \tag{2}$$

$$\mathbf{i_i} = \mathbf{T_{CSR}^T} \mathbf{i_{DC}}$$

where $\mathbf{T_{CSR}}$ is the transition matrix between input and output of CSR.

C. Inverter Model

The voltage source inverter has 8 valid switching vectors, and two of them are zero vectors. Valid switching states and corresponding input and output variables for inverter side are provided in Table II.

TABLE I
RECTIFIER SIDE'S VALID SWITCHING STATES

#	S_{r1}	S_{r2}	S_{r3}	S_{r4}	S_{r5}	S_{r6}	i_{sa}	i_{sb}	i_{sc}	v_{DC}
1	1	0	0	0	0	1	i_{DC}	0	$-i_{DC}$	v_{ac}
2	0	0	1	0	0	1	0	i_{DC}	$-i_{DC}$	v_{bc}
3	0	1	1	0	0	0	$-i_{DC}$	i_{DC}	0	$-v_{ab}$
4	0	1	0	0	1	0	$-i_{DC}$	0	i_{DC}	$-v_{ac}$
5	0	0	0	1	1	0	0	$-i_{DC}$	i_{DC}	$-v_{bc}$
6	1	0	0	1	0	0	i_{DC}	$-i_{DC}$	0	v_{ab}

TABLE II
INVERTER SIDE'S VALID SWITCHING STATES

#	S_{i1}	S_{i2}	S_{i3}	S_{i4}	S_{i5}	S_{i6}	v_{uv}	v_{vw}	v_{wu}	i_{DC}
1	1	0	0	1	0	1	v_{DC}	0	$-v_{DC}$	i_{ou}
2	1	0	1	0	0	1	0	v_{DC}	$-v_{DC}$	$i_{ou}+ i_{ov}$
3	0	1	1	0	0	1	$-v_{DC}$	v_{DC}	0	i_{ov}
4	0	1	1	0	1	0	$-v_{DC}$	0	v_{DC}	$i_{ov}+ i_{ow}$
5	0	1	0	1	1	0	0	$-v_{DC}$	v_{DC}	i_{ow}
6	1	0	0	1	1	0	v_{DC}	$-v_{DC}$	0	$i_{ou}+ i_{ow}$
7	1	0	1	0	1	0	0	0	0	0
8	0	1	0	1	0	1	0	0	0	0
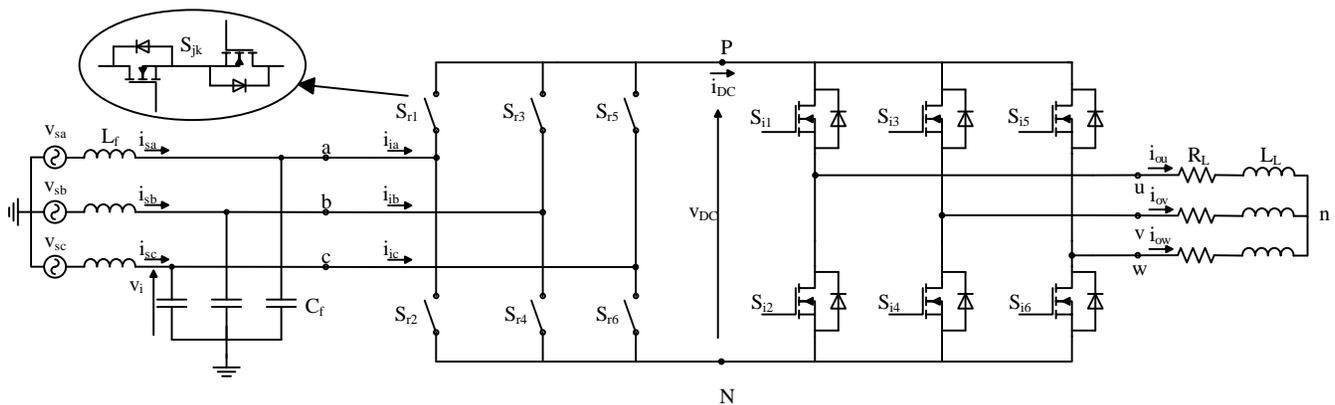
Fig.1. Indirect Matrix Converter
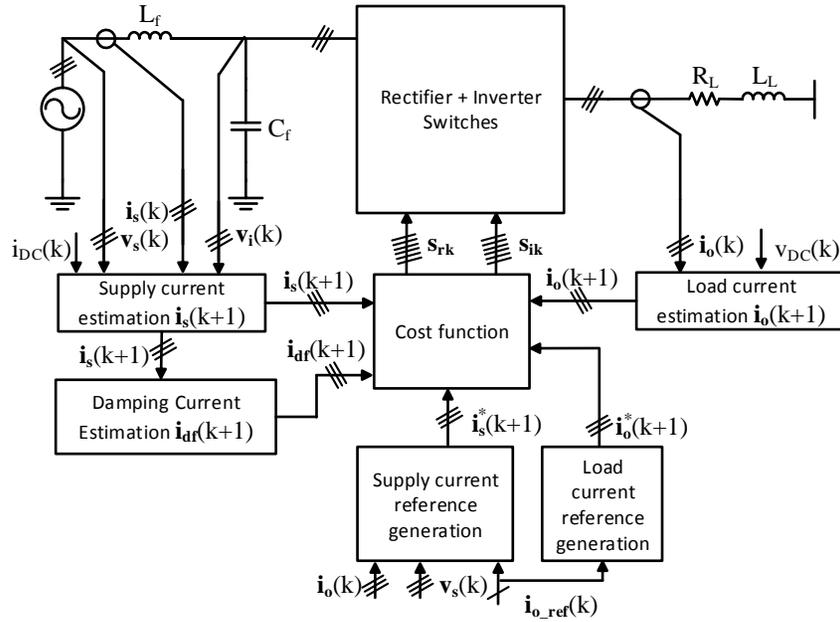
Fig.2. Model Predictive Control Scheme for IMC

The relationship between input and output current and voltage variables of VSI is defined in (3) and (4).

$$i_{DC} = \begin{bmatrix} S_{i1} & S_{i3} & S_{i5} \end{bmatrix} \begin{bmatrix} i_{ou} \\ i_{ov} \\ i_{ow} \end{bmatrix}$$
$$= T_{VSI} i_o$$

(3)

$$\begin{bmatrix} v_{oun} \\ v_{ovn} \\ v_{own} \end{bmatrix} = \frac{v_{DC}}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} S_{i1} & S_{i3} & S_{i5} \end{bmatrix}^T$$

$$v_o = \frac{v_{DC}}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} T_{VSI}^T$$

(4)

D. Prediction Model for Rectifier Side

In order to compensate the supply current error, the supply current must be predicted. In this regard, unity power factor is achieved. Input filter model of CSR is used to predict the supply current value at next sampling interval and the discrete model is defined in (5).

$$\begin{bmatrix} v_i(k+1) \\ i_s(k+1) \end{bmatrix} = \Phi \begin{bmatrix} v_i(k) \\ i_s(k) \end{bmatrix} + \Gamma \begin{bmatrix} v_s(k) \\ i_i(k) \end{bmatrix}$$

(5)

Supply current prediction, which will be used in the cost function, is based on (6).

$$i_s(k+1) = \Phi(2,1)v_i(k) + \Phi(2,2)i_s(k)$$
$$+ \Gamma(2,1)v_s(k) + \Gamma(2,2)i_i(k)$$

(6)

E. Prediction Model for Inverter Side

In order to control the output current, the discrete time model of load is required, and it is given by (7).

$$i_o(k+1) = i_o(k)\left[1 - \frac{R_L T_s}{L_L}\right] + \frac{T_s}{L_L} v_o(k)$$

(7)

III. MODEL PREDICTIVE CONTROL

The schematic illustration of the proposed MPC technique is depicted in Fig. 2. For the kth sampling instant supply voltages v_s, supply currents i_s, input filter capacitor voltages v_i and output load currents i_o are measured. The dc link voltage is predicted based on (1), and it is calculated for each switching vector of CSR side using input filter capacitor voltage measurements at k^{th} instant. If this predicted dc link voltage is positive, then related rectifier switching vector is evaluated for each switching combination of inverter side. Firstly, load currents are predicted based on (7) for each inverter switching vector by substituting the predicted dc link voltage. These load current estimations are used for cost function evaluation in (8). Secondly, the dc link current is predicted based on (3) for each inverter switching vector and then this dc link current prediction for related inverter switching vector is used to predict supply currents based on (6) for related rectifier switching combination. Then these supply current predictions evaluated in the cost function defined by (9). These two cost functions are combined into a single cost function as shown in (10).

$$g_1 = \sum_{j=u,v,w} \left| i_{oj}^*(k+1) - i_{oj}(k+1) \right|^2$$

(8)

$$g_2 = \sum_{j=a,b,c} \left| i_{sj}^*(k+1) - i_{sj}(k+1) \right|^2$$

(9)

$$g_{tot} = g_1 + g_2 \tag{10}$$

Once the cost function evaluation process is over for the inverter stage, whole operation is repeated for the next candidate dc-link voltage generated from rectifier stage. Basically, cascaded structure is considered for proper operation. The rectifier stage has 3 valid switching states that give positive dc link voltage and the inverter stage has 8 switching states and there are totally 24 switching combinations in the single step prediction horizon. The switching combination that provides minimum cost function value is picked and applied to IMC for the next time interval. The cost function includes current terms for supply and load sides and as a result no weighting factor is required to distinguish the control importance one over another.

IV. REFERENCE GENERATION AND COMPENSATOR DESIGN

The approach to generate supply currents synchronized with grid voltages is illustrated in Fig. 3 where $i_{o\_ref}(k)$ is the magnitude of load current reference. Measured three phase load currents are firstly transformed to dq frame and then the magnitude of rotating space vector is calculated. The error signal, which is difference between reference load current and measured load current, is fed into PI compensator and a constant multiplication factor, designated with m, is generated. This constant is then used to generate three phase supply current references by multiplying it with instantaneous grid voltages.

In order to design the controller, dynamic model of the plant is required, and it is derived by equating input power to output power with the assumption of a lossless converter. Another assumption in this derivation is that input filter has much faster dynamics than the load dynamics and hence its effect is neglected in plant modeling. Accordingly, (11) is obtained.
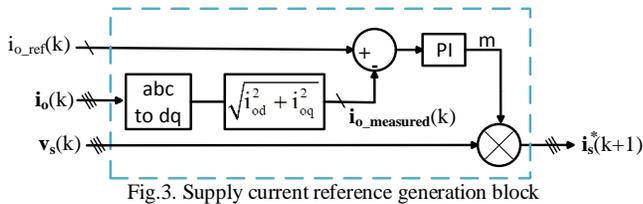
Fig.3. Supply current reference generation block

$$1.5V_S I_S = I_o^2 \left(R_L + sL_L \right) \tag{11}$$

After usual perturbation and linearization steps on (11), dynamic model can be expressed by (12). The open loop bode plot of dynamic model with the parameters; I_o=5A, V_S=311V, R_L=10Ω and L_L=10mH is given in Fig. 4.

$$\frac{\grave{U}{i_o}}{\grave{U}{i_s}} = \frac{1.5V_S}{2I_o(R_L + sL_L)} \tag{12}$$

A PI controller is designed by setting the cross-over frequency at 300 Hz and the phase margin to 67º. Bode plot of compensated loop gain is shown in Fig. 5. Frequency domain equation of PI compensator is given in (13) and discrete time domain equivalent, which is obtained by applying Forward Euler discretization, is given in (14).

$$C(s) = k_p + \frac{k_i}{s} \tag{13}$$

$$u(k) = u(k-1) + k_p e(k) + \left(k_i T_S - k_p \right) e(k-1) \tag{14}$$

where u is the output of the PI compensator and e is the input of PI compensator and the error in the control variable.

V. ACTIVE DAMPING METHOD

Lightly damped input LC filter of CSR causes unwanted harmonics generation. In particular, this issue appears when system harmonics around the resonant frequency from utility or rectifier itself is interfered to the filter. These harmonics pollute the grid currents and the harmonic level in the grid current can become unacceptable. A usual way to damp the resonance of LC filter is to add a resistor in parallel to filter capacitor at the expense of a drastic reduction in the efficiency. The function of this parallel resistor can be emulated by means of a technique called as active damping employed in the control scheme, and a damping effect can be obtained without disturbing the efficiency.

In this study a novel active damping method is proposed, and its conceptual scheme is illustrated in Fig. 6. The aim in active damping is to decrease the supply current harmonic contents. Thus, three phase supply currents can be directly
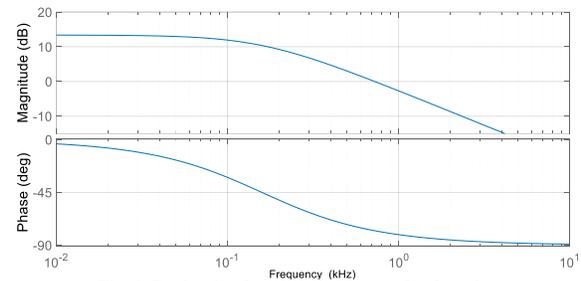
Fig.4. Bode plot for open loop transfer function
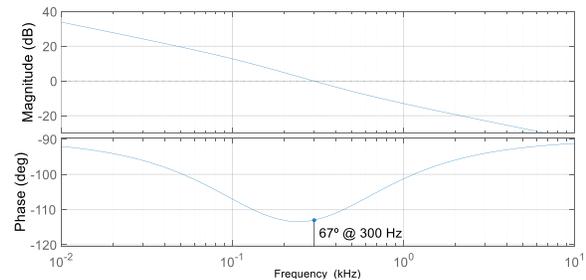
Fig.5. Bode plot for compensated loop function

Fig.6. Damping current estimation scheme

used in damping scheme instead of using input filter capacitor voltage with a suitable damping resistance value as have been widely adopted in literature [10], [23], [25]. Since the MPC technique has a predictive nature, predicted value of supply current $i_s(k+1)$ for next sampling interval is used in active

damping. These three phase currents include components located at fundamental grid frequency and higher frequencies. A High Pass Filter (HPF), whose transfer functions in continuous and discrete time domain are defined in (15) and (16) respectively, can be used to remove fundamental component and to obtain high frequency components which are responsible of supply current pollution. If these three phase currents $i_{df}(k+1)$ composed of high frequency components are subtracted from the supply current references, then this effectively reduces the magnitudes of high frequency harmonics in supply current and filter capacitor voltage. Accordingly, the cost function g_2 must be updated as shown in (17).

The design of HPF is essential in terms of filtering capability of high-frequency components to obtain a good damping effect. In order to alleviate fundamental component and allow to pass higher order harmonics, a first order HPF with a bandwidth of 500 Hz is used to generate filtered version of supply current predictions, $i_{df}(k+1)$.

$$HPF(s) = \frac{3.1831e-04s}{1+3.1831e-04s} \tag{15}$$

$$i_{df}(k+1) = 0.9372\, i_{df}(k) + i_d(k+1) - i_d(k) \tag{16}$$

$$g_2 = \sum_{j=a,b,c} \left| i_{sj}^*(k+1) - i_{dfj}(k+1) - i_{sj}(k+1) \right|^2 \tag{17}$$

VI. FPGA Implementation Scheme

A big disadvantage of model predictive control method is high sampling rate required to achieve robust operation. MPC contains large amount of control calculations and this causes

an issue in real-time implementation. To handle with high computational burden imposed by MPC algorithm, FPGA devices can be used to perform all control calculations in parallel. Since MPC contains independent math calculations for different switching combinations, these calculations can be implemented simultaneously. The main principle of FPGA-based MPC is that independent calculation blocks are concurrently performed in different FPGA areas by dividing the instructions processing cycle into distinct stages of processing. This significantly increases total bandwidth of the controller and whole control algorithm can be performed in a shorter time. The main idea of how paralleling the control calculation of the proposed method is shown in Fig. 7. The first step is to extract the required measurement from sensing board and these measurements are used to identify which rectifier switching combination provide dc-link voltage to the inverter stage. Second step is to move proper rectifier switching combination information to the buffer. After that, output load current is predicted for different inverter switching states. As can be seen from Fig. 7, instead of doing serial computation, independent prediction blocks are distributed to the different areas of the FPGA. This reduces the total execution time and provides higher control bandwidth. The next step is to predict the supply current for different selected rectifier state. The last step is to perform exhaustive search so as to obtain optimum control action for the next time interval.

This pipelining procedure can be implemented in cost-effective FPGA solutions, such as DEO-Nano Board from Terasic. The aforementioned board has Cyclone IV and 50 MHz clock speed. Since FPGA does not have fixed core
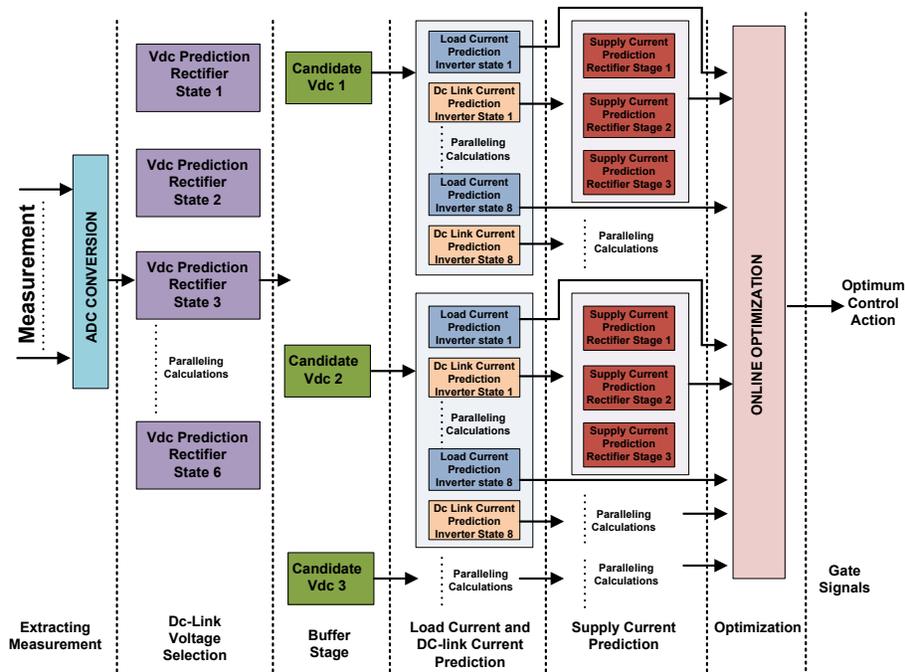
Fig.7. Parallel implementation scheme of the proposed control on a FPGA device

http://dergipark.gov.tr/bajece

TABLE III
APPROXIMATE TOTAL EXECUTION TIME FOR EACH STEP

Tasks	Clock Cycle	Execution Time (µs)
Extracting Measurement	4	0.08
DC-Link Voltage Selection	2	0.04
Buffer Stage	1	0.02
Load Current Prediction and Dc-Link Current Prediction	15	0.30
Supply Current Prediction	11	0.22
Cost Calculation	28	0.56
Optimization	37	0.74
Total	98	1.96

architecture, total performance can be calculated Clock SpeedxCore/(1 Clock Cycle). The effective core number depends on the pipelining stage that designed by the user. Approximate total execution time for each task is tabulated in Table III in case of fully pipelining architecture. Since data dependency occurs due to cascaded MPC block, there is a limit in decreasing the running time of proposed MPC algorithm. The values reported in Table III are extracted by performing VHDL design simulation using ModelSim ALTERA. The approximated values are measured from ModelSim ALTERA scope and state-machine cycles are observed by using the simulation tools.

VII. SIMULATION RESULTS

The proposed control scheme is validated by simulation work performed in Matlab/Simulink with parameters tabulated in Table IV.

Waveforms presented in Fig. 8 are obtained when a load current reference with a peak value of 10 A at 100 Hz is applied to the converter. Fig. 8a shows the supply voltage and current (x50) for phase-a and as it is observed from the figure that almost unity power factor for the grid side is achieved-with the proposed controller. Three-phase supply current references generated by the method depicted in Fig. 3 are shown in Fig. 8b. They are in phase with grid voltages as it is observed in Fig. 8a and supply currents track sinusoidal references as shown in Fig. 8c. Load current references and measurements are shown in Fig. 8d and load currents show a good performance in terms of reference tracking. Power components of supply side are also shown in Fig. 8e and reactive power component remains at zero as it is expected in unity power factor control. From Fig. 8 it can be concluded

TABLE IV
SIMULATION PARAMETERS

Parameter	Description	Values
T_S	Sampling Period	20 µs
R_L	Load Resistance	10 Ω
L_L	Load Inductance	10 mH
L_f	Input Inductance	400 uH
C_f	Input Capacitance	21 µF
R_f	Inp. Filt. Damp Resistance	0.5 Ω
V_s	Supply Peak Voltage	311 V
F_g	Supply frequency	50 Hz

that the proposed control gives enough flexibility to control the relatively complex IMC topology in terms of input power factor correction an output load current control.
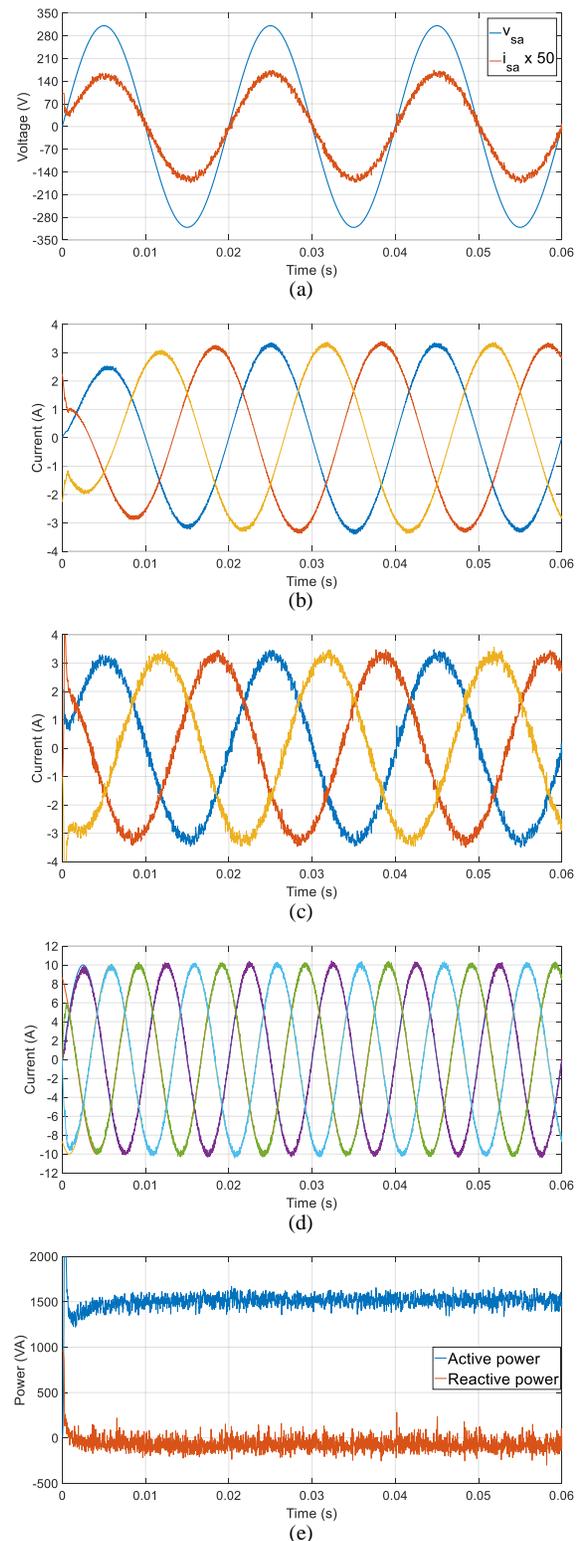
Fig.8. Waveforms for I_{o_REF}=10A @ 100 Hz; (a) Supply voltage and current (x50) for phase-a, (b) Three phase supply current references, (c) Three phase supply currents, (d) Three phase load current references and load currents, (e) Supply power components

TABLE V
THD RESULTS OBTAINED UNDER DIFFERENT CONDITIONS
APPROXIMATE

Sampling and load reference ↓	$I_{O\_REF} \to$ THD → Control↓	5A		10A	
		load 5A	supply 0.84A	load 10A	supply 3.26A
T_S=20μs Load ref. at 50Hz	without damping	3.03%	30.02%	1.59%	7.58%
	with damping	3.32%	16.21%	1.97%	5.46%
T_S=20μs Load ref. at 100Hz	without damping	2.90%	33.36%	1.63%	7.76%
	with damping	3.28%	15.23%	2.01%	5.58%
T_S=50μs Load ref. at 50Hz	without damping	8.28%	62.62%	5.22%	28.24%
	with damping	9.94%	42.31%	6.76%	23.88%

K_p=0.288, K_i=669.56

Table V compares the THD levels in supply current for different load current reference demands. The proposed controller achieves a good performance for THD levels in load currents with a sampling period of 20 μs. The THD in supply currents is generally problematic in the control of IMC especially at low current demands. For supply current peak value of 0.84 A, the THD is 30.02% and it reduces to 16.21% with the inclusion of proposed damping technique. For higher current level of supply, the THD value inherently decreases and active damping also reduces these THD values by around 2%. Activating the damping term in the proposed control causes a slight increment in THD of load currents, but it is in the range of acceptable levels.

Fig. 9 compares the supply current FFT analysis results with and without active damping for the case where reference load current of 5A at 100 Hz is applied to converter, and as a result

there is a supply current having a 0.84A peak value at 50 Hz. Inclusion of the active damping shows a considerable reduction in THD values especially for low current levels.

VIII.   CONCLUSION

This paper proposes a model predictive approach to control IMC topology. Following two goals are simultaneously achieved; unity power factor with relatively low THD for supply current and sinusoidal current with desired magnitude and frequency for three phase RL load. Magnitude of supply current reference is generated from the error in the magnitude of load current space vector by a PI compensator. Input filter model is used to predict future behavior of the supply current so as to control the rectifier stage. These current predictions in abc frame are then employed in the cost function. Active damping current term, which is obtained by high-pass filtering the supply current prediction, is also included into cost function of rectifier side to mitigate resonance phenomenon of input LC filter. Adding this damping term in the cost function helps to reduce harmonics in supply current. Conventional MPC approach, whose cost function employs load currents in abc frame, is adopted for the inverter side to synthesize sinusoidal current with desired peak value and frequency. In order to find best switching combination, a typical exhaustive search algorithm is performed for 24 different switching combinations. The one among these combinations minimizes the cost function is selected.

Fig.9. FFT analysis for supply current for I_{o_REF}=5A @ 100 Hz; (a) without active damping, THD=33.36% (b) with active damping, THD=15.23%.

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