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A SIMPLE APPROACH FOR MODELING THE INFLUENCE OF HOT-CARRIERS ON THRESHOLD VOLTAGE OF MOS TRANSISTORS

MOSFET'LERDE SICAK TAÞIYICILARIN EÞÝK GERÝLÝMÝNE ETKÝSÝNÝN MODELLENMESÝ ÝÇÝN YENÝ BÝR YAKLAÞIM

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ABSTRACT

Hot-carrier-induced degradation of MOSFET parameters over time is an important reliability concept in modern microcircuits. High energy carriers also called hot carriers are generated in the MOSFET by the large channel electric field near the drain region. The electric field accelarates the carriers to effective temperatures well above the lattice temprature. These hot carriers transfer energy to the lattice through phonon emission and break bonds at the Si/SiO_2 interface. The trapping or bond breaking creates oxide charge and interface traps that effect the channel carrier mobility and the effective channel potential.
Interface traps and oxide charge effect transistor performance parameters such as threshold voltage and drive currents in all operating regimes. In this paper, the influence of the hot carriers on the threshold voltage of MOS trasnsistors is examined experimentally. Using these experimental results a new method for representation of hot-carrier effect on the threshold voltage of MOS transistors is proposed.

Key words: *MOS transistor, Hot carriers, MOS models*

ÖZET

Bu çalýþmada, sýcak taþýyýcýlarýn N-MOS tranzistorlarýn eþik gerilimi üzerindeki etkileri incelenmiº veliteratürdeki çalýþmalara bir alternatif oluþturmak üzere, polinomsal eðri uydurmaya dayanan bir model önerilmiþtir. Önerilen yöntemde, belirli bir proses için tranzistorun sýcak taþýyýcýlardan ne þekilde etkilendiði baþta deneysel olarak belirlenmekte, bu davranýþa bir polinom uydurulmakta, elde edilen sonuçlar ayný proses yardýmýyla üretilecek tüm tranzistorlara uygulanabilmektedir.

Anahtar sözcükler: *MOS tranzistor,Sýcak Taþýyýcýlar, MOS modelleri*

1. INTRODUCTION

Hot carrier induced phenomena continue to create great interest because of their important role in device reliability[1-19]. High energy carriers also called hot carriers are generated in the MOSFET by the large channel electric field near the drain region. The electric field accelarates the carriers to effective temperatures well above the lattice temprature. These hot carriers transfer energy to the lattice through phonon emission and break bonds at the Si/SiO_2 interface. The trapping or bond breaking creates oxide charge and interface traps that effect the channel carrier mobility and the effective channel potential.

Interface traps and oxide charge effect transistor performance parameters such as threshold voltage and drive currents in all operating regimes. In determining the reliability of a MOS process, it is important to consider two prime factors, namely the gate oxide quality and the susceptibility of MOSFETs to hot carrier degradation. The gate-oxide thickness is one of the important scaling parameters for VLSI device design. A thinner gate oxide NMOS shows a smaller drain current degradation and a threshold voltage shift but a larger substrate current. For the prediction of the long term reliability of MOS devices, the study of hot-carrier effects is mandatory [18].

Several works were performed for investigation of hot-carrier effect on the performance of NMOS and PMOS transistors and for digital and analog cases [1-19]. It has been recognized that the degradation of NMOS transistors is caused by the interface state generation and electron trapping in the gate oxide from the hot-carrier injection. Reliability assurance of analogue circuits requires a largely different approach than for the digital case. The hot-carrier degradation of PMOS is investigated from the viewpoint of analogue operation [6,7,8,12,13]. In the mid eighties serious problems were discovered in connection with PMOS degradation. It was soon generally accepted that effects from injected and trapped electrons dominate the degradation behaviour.

In a recent work a method is presented that allows to quantify the effects of hot carrier degradation on analog CMOS circuits. Specific features of hot carrier degradation related to analog CMOS operation are discussed in detail. Single transistor stress experiments are defined monitoring analog operation and conclusions are drawn for the choice of analog hot carrier lifetime criteria. A general method is presented which establishes a relation between single transistor stress results and circuit parameter degradation [9].

One of the most important goals of hot-carrier considerations related to analog operation is to enable the prediction of circuit parameter degradation on the basis of simple, standard single transistor stress experiments.
The main difficulty in representation the influence of the hot-carriers on MOS transistor behaviour is the determination of the values for physical quantities [9,13].

Polynomial approximation is a well-known mathematical method, used often for representation of the behaviour of some physical systems where problems exist in describing it analytically. In this case, the polynomial approximation provides a solution to overcome these serious mathematical problems [20].

In this paper the deviation in the threshold voltage of the NMOS transistor is investigated in detail and a simple approach for modeling the influence of hot-carriers on threshold voltage of MOS transistors is proposed. The aim of this work is to suggest an alternative method to the existing models in the literature. The analytical model derived for the threshold voltage is based on observation of the MOS transistor behaviour manufactured with a specified process and applying the polynomial approximation on these observation results. The simple approach proposed is useful to predict the change in the threshold voltage for a specified stress-time. Therefore, the work also focuses on the transistor performances and hot-carrier reliability in NMOS transistors.

2. INFLUENCE OF HOT-CARRIERS ON THRESHOLD VOLTAGE OF NMOS TRANSISTOR, EXPERIENTAL RESULTS

Experiments were performed on NMOS test transistors fabricated in TUBITAK MAM-YITAL with 3µm technology. The dimensions of

these NMOS transistors were W=27µm, L=3µm. The test circuit to apply a stress on the MOS transistors is illustrated in Fig.1 which was realized with *semiconductor parameter analyser* HP4155. Applying a stress voltage of V_D=5V and choosing the gate biasing voltage as V_G=1V, V_G=1.5V and V_G=2V which correspond to subthreshold, linear and saturated operating regions respectively; the transfer characteristic of the test device was observed and recorded for a time period of 10 hours with a time step of 30 minutes, the experimental data obtained is used to determine the threshold voltage V_{th} [21,22].

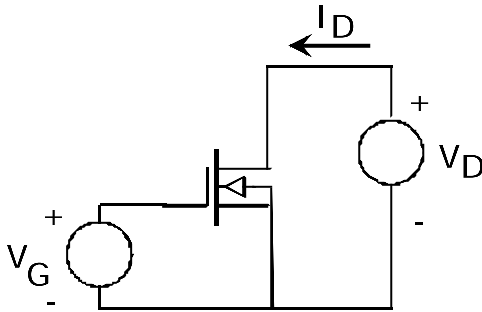

Fig.1. Test circuit to apply a stress on the MOS transistor realized with *semiconductor parameter analyzer* HP4155.

The same process is repeated on several samples of NMOS transistors with the same properties. Experimental results obtained for a stress voltage of V_D=5V and gate biasing voltages of V_G=1V, V_G=1.5V and V_G=2V are shown in Figs.2,3 and 4.

The MOS transistor behaviour illustrated in Figs.2,3 and 4 can be represented by using an adequate polynomial approximation as

$$V_{th}(t)=a_0+a_1t+a_2t^2+a_3t^3+a_4t^4+a_5t^5 \quad (1)$$

where a_i (i=1 to n) denote the polynomial coefficients and t is the stress time.

The polynomial coefficients are extracted by a MATLAB Program from the data given in Figs.2, 3 and 4 for different stress conditions and are shown in Table.1.

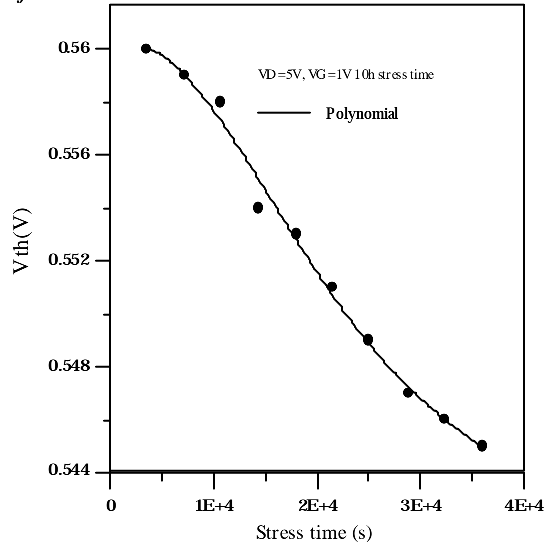

Fig 2. Time dependence of the threshold voltage (V_{th}) for a stress of V_D =5V, V_G = 1V

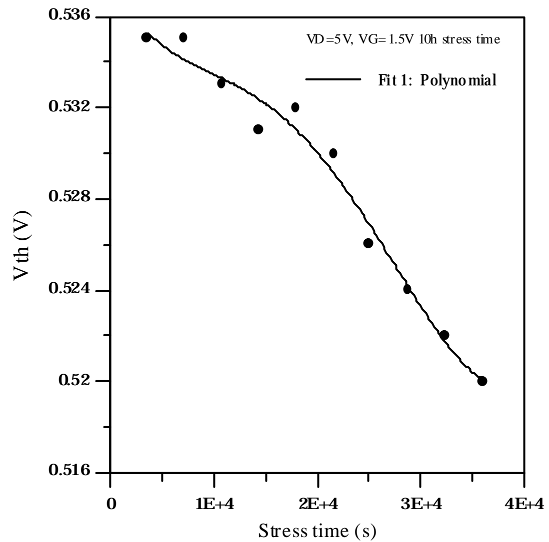

Fig. 3. Time dependence of the threshold voltage (V_{th}) for a stress of V_D =5V, V_G = 1.5V

Experimental results for different stress conditions are also summarized in the three dimensional plot of V_{th} = $V_{th}(V_G,t)$ illustrated in Fig.5.

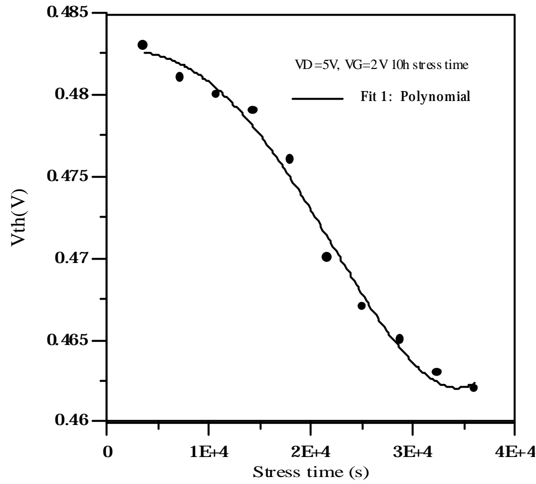

Fig 4. Time dependence of the threshold voltage (V_{th}) for a stress of V_D =5V, V_G = 2V

As it can be observed from Fig.5 the threshold voltage decreases with the stress time; furthermore V_{th} also decreases with the gate stress voltage V_G.

The relative changes in the drain current $\Delta I_D/I_D$ obtained experimentally for a) V_D =5V, V_G = 1V, b)V_D =5V, V_G = 1.5V c) V_D =5V, V_G =2V and given in Fig.6. As it can be observed from the figure, the relative change in the drain current $\Delta I_D/I_D$ increases with the stress time. Note from the figures that the polynomial approximation proposed predicts the behaviour of the MOS transistor adequately.

The same process is applied to another type of MOS transistors realized with a different technology. The model obtained is also found to be succesful in representing the device behaviour. As a result, one can conclude that the approximation proposed can be used for any MOS transistor independently from the manufactoring process and from the transistor dimensions.

The threshold voltage V_{th} is one of the most important parameters influenced by hot-carrier degradation and decreases with the stress time which results in an increase in the drain current as it can be observed from measurement data given in Figs. 2 to 6.

Table 1. The polynomial coefficients extracted from the data given in Figs.2, 3 and 4 for different stress conditions

	V_G=1V	V_G=1.5V	V_G=2V
a_0	0.559833	0.537667	0.48275
a_1	$2.862\text{x}10^{-7}$	$-8.871\text{x}10^{-7}$	$3.1984\text{x}10^{-11}$
a_2	$-6.92\text{x}10^{-11}$	$7.7\text{x}10^{-11}$	$-8.641\text{x}10^{-12}$
a_3	$2.132\text{x}10^{-15}$	$-3.522\text{x}10^{-15}$	$-1.542\text{x}10^{-15}$
a_4	$-2.082\text{x}10^{-20}$	$4.683\text{x}10^{-20}$	$3.73\text{x}10^{-20}$

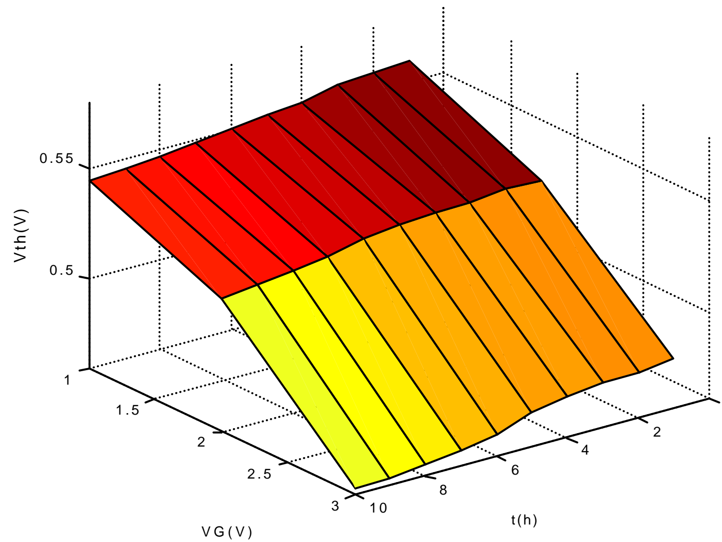

Fig.5. Dependence of the threshold voltage (V_{th}) on the gate voltage (V_G) and on the stress time (t)

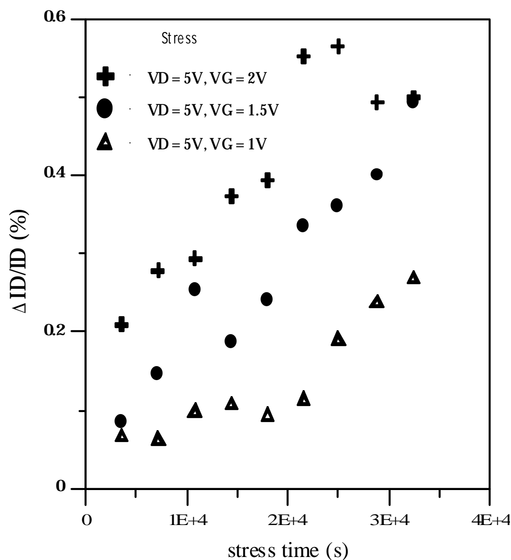

Fig..6. Dependence of relative change $\Delta I_D/I_D$ (%) in drain current on stress-time for a stress of a)V_D =5V, V_G = 1V, V_D =5V, b)V_G = 1.5V, c) V_D =5V, V_G = 2V

The increase in the drain current is especially important for MOSFET operation in analogue applications since it shifts the operating point of the transistor and changes fully the operating conditions of the corresponding building blocks [9,11,12]. Therefore it is useful to represent and incorporate this change in the threshold voltage in any circuit simulation program. Figure 7 illustrates a simple model to provide the representation of the hot-carrier effect on the threshold voltage V_{th} . Note that Eqn.1 is in the form of a power series and can converge for stress time values greater than the observation time;

therefore a long obsevation time is necessary to represent the device behaviour accurately.

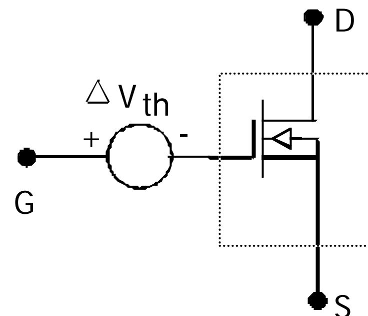

Fig. 7. Model to represent time dependent variation of threshold voltage V_{th} caused by hot-carrier effect

3. APPLICATION EXAMPLE

The advantages provided by the method proposed is demonstrated on an application example. The change in the threshold voltage caused by hot-carriers influences drastically the operating point of the MOS transistor in analogue building blocks. One typical example is the harmonic distortion properties of the active-loaded single stage amplifier shown in Fig.8

which is the most important building block of operational amplifiers, OTAs, audio amplifiers etc. where it is used as an intermediate stage. In recent works it was furthermore shown that the total harmonic distortion of this stage depends strongly on the operating point and at an special biasing point the total harmonic distortion crosses through a minimum point [23, 24]. The test circuit is an active-loaded MOS amplifier stage realized with TUBITAK 3μ technology with transistor dimensions W=27μm, L=3μm for NMOS. The load transistors were chosen as bipolar transistors to avoid any additional hot-carrier effect caused by PMOS load transistors.

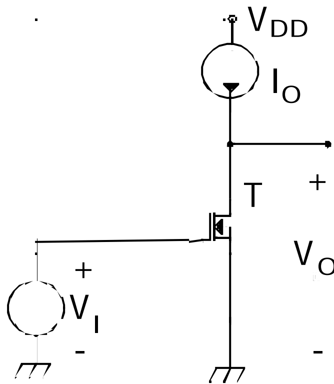

Fig.8. Single stage active-loaded MOS amplifier

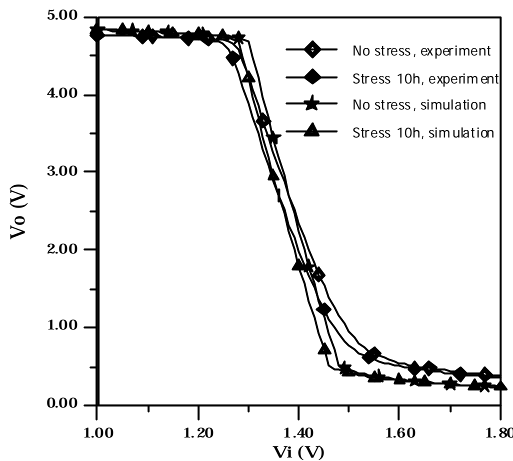

Fig.9. Experimental and simulated dependence of dc transfer curve on stress time.

Experiments were performed by using HP 4155 Parameter Analyzer. The supply voltage was V_{DD} = 5V. The operating point of the amplifier was chosen at V_O = 2.6V and I_O = 200μA. The threshold voltage before the stress is specified as V_{th}= 0.53V. The value of V_{th} decreases to V_{th} = 0.51V after a stress of 10 hours which can be also predicted by using eqn.1. The dependence of dc transfer curve on stress time is obtained experimentally and given in Fig.9. The mid-point of the transfer characteristic is specified as V_I = 1.38V and V_O = 2.75V. SPICE simulations result in a mid-point of V_I = 1.38V, V_O = 2.69V. After applying a stress of 10 hours the experimental mid-point is shifted to V_I = 1.38V,V_O = 2.24V. With the predicted threshold voltage of 0.51V SPICE simulations result in V_O = 2.3V for V_I = 1.38V. It can be clearly observed from the results in Fig. 9 that the method proposed is useful to predict accurately the shift in the operating point caused by the change in the threshold voltage due to the hot-carrier effect. Any shift in operating point influences the harmonic distortion porperties of the amplifier, which is demonstrated by SPICE simulations using an accurate MOSFET model. The model used for MOS transistors is proposed in earlier works and intended especially for accurate simulation of analogue building blocks [23-25]. The accuracy of the model was proven by measurement results. Simulation results yield the plot of THD against V_{OQ} shown in Fig.10. V_{OQ} is the operating drain-source voltage of the NMOS driver transistor. As it can be observed from Fig.10, at V_{OQ} = 2.8V the total harmonic distortion crosses through a minimum point of THD_{min} = 0.25%. Fig.12 and Fig.13 show that after a stress of 10 hours the operating point is shifted to V_{OQ} = 2.2V and the total harmonic distortion is increased to a much larger value of THD = 2% which demonstrates clearly the degradation in the amplifier performance.

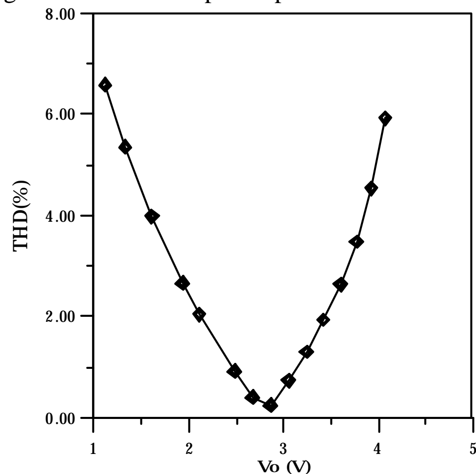

Fig.10. Dependence of total harmonic distortion of active-loaded amplifier stage on operating point.

4. CONCLUSION

In this paper, the influence of the hot carriers on the threshold voltage of MOS transistors is examined experimentally. Using these experimental results a new method for representation of hot-carrier effect on the threshold voltage of MOS transistors is proposed. The method is based on the polynomial approximation. The approximation proposed can be used for any MOS transistor independently from the manufacturing process and from the transistor dimensions; therefore it can be applied to any MOS transistor. A simple model is given to represent the hot-carrier effect on the threshold voltage V_{th}. The method and the model derived is especially useful to determine the change in the threshold voltage of the MOS transistors in analogue building blocks and to predict the operation reliability; therefore it provides new possibilities in the analogue IC design.

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