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COMPLEMENTARY PASS TRANSISTOR LOGIC SYNTHESIS WITH 123 DECISION DIAGRAM

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ABSTRACT

123 decision diagram is a very effective PTL synthesis tool based on binary decision diagram. It realizes a logic function using NMOS pass transistors with CMOS restoring buffers. In this paper the 123 decision diagram is applied to realize CMOS pass transistor logic circuits without restoring buffers. Cell circuits for the 4 bit adder is realized with the CMOS pass transistors using the 123 decision diagram and 4 bit adder is completed by combining the cells.

Keywords: *Pass Transistor Logic, 123 Decision Diagram, Adder Circuit, CMOS Circuit Design.*

1. INTRODUCTION

Pass Transistor Logic (PTL) circuits implement a logic function as a network of MOS transistors [1]. PTL circuits are well suited for pipelined circuits and they have enhanced performance over conventional CMOS circuits in terms of silicon area, speed and reduced power dissipation [1], [2].

General PTL design methods contain two different approach; transistor level synthesis based on decision diagrams [2] and library based synthesis. The transistor level PTL synthesis has more flexibility in circuit optimization however optimization of large network is difficult. The transistor based PTL has two different design methodology; those that use CMOS pass transistor (CPTL), and those that use NMOS PTL with CMOS restoring buffers [1]. The library based synthesis are generally limited to two-level synthesis then combination of these blocks realize the required function similar to AND/OR logic [1-4].

Binary decision diagrams (BDD) are data structures that represent Boolean functions [3], [5], [6]. Although BDDs have traditionally been viewed as purely behavioral entities, it is well known that they can represent trees of multiplexers due to the correspondence between their structure and Shannon decomposition [1], [7].

123 decision diagram is an efficient simplification and implementation of NMOS pass transistor circuits with CMOS restoring buffers [1].

In this paper the 123 decision diagram was applied to realize a full adder cell. The full adder cells were combined to build 4 bit adder CMOS pass transistor logic circuits without restoring buffers. Finally, the simulation results of the circuit were concluded.

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2. PTL AND THE 123 DD

PTL depends on controlling the gates of MOS transistors to conduct pass signals with respect to control signals. In Figure 1 an NMOS PTL schematic is shown.

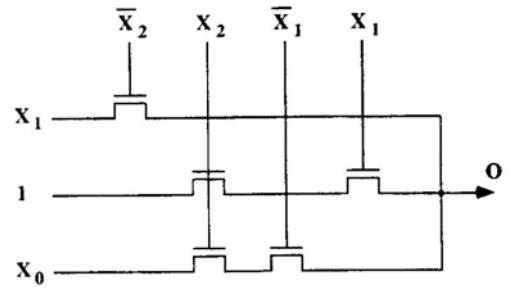

Figure 1. NMOS PTL circuit.

$$F = \overline{X}_1.X_2.X_0 + X_1.X_2 + X_1.\overline{X}_2 \qquad (1)$$

The function of Figure 1 is given in equation (1). The signals $X_1, 1, X_0$ are called as pass signals and $X_1, \overline{X}_1, X_2, \overline{X}_2$ are called as control signals. 123 decision diagram is proposed for top down design method. It directly gives the layout of the realized circuit. The 123 decision diagram contains simplification method which provides an optimized design method. Since it is adapted to the CMOS pass transistor circuits, the spontaneous layout drawing ability can not be used.

123 decision diagram has two components. One of them is hyper graph showing the connections of transistors and pass signals, the other one is a list showing the relations of the transistors [1]. The hyper graph allows 1, 2 or at most 3 connection edge for each node in the graph. And the name of the diagram has been coming from this property. Hyper graph elements are terminal nodes, non terminal nodes and node identities. The terminal nodes show external inputs to the designed chip and they are shown with the square. Nonterminal nodes contain transistor connections and shown with circles. Each node has a specific identity number. This number is obtained as multiplying node identity number of one upper level node by three and adding the edge value between the node and upper one. Only nonterminal nodes have node identities.

If two or more nonterminal nodes can be shown by dashed line this means hyper edge exist and these nodes can be connected to each other. All edge can have 0, 1 or 2 values. 0 and 1 values represent a MOS transistor, 2 value represents a metal connection [1].

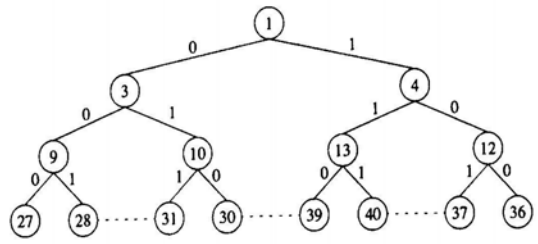

Figure 2. The hyper graph

In Figure 2, a hyper graph is shown. The dashed lines show a connection between the nodes. In Figure 3 the circuit schematic of this graph is shown. The 0 and 1 numbered edges in Figure 2 are shown with T_i transistors in Figure 3. The nodes numbered as 30 and 31 are children nodes of the node with number 10. Their values are obtained by multiplying grand node value by 3 and adding the edge values.

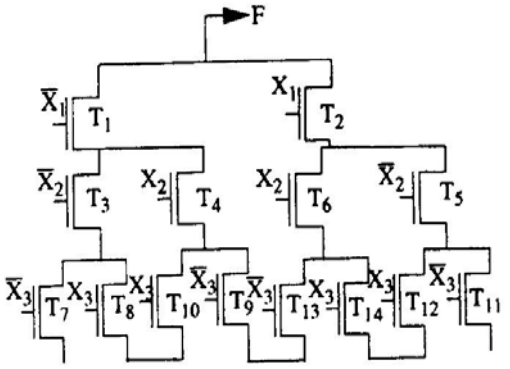

Figure 3. Circuit equivalent of Figure 2

Transformations and edge mergings are operations supplying the element composition and simplification in 123 decision diagram for circuit realization.To realize a decision diagram it has to be converted completely terminal nodes. Then circuit conversion of the circuit can be obtained [1].

3. THE APPLICATION CIRCUIT

A 4 bit full adder (FA) circuit was realized by the CMOS PTL. The 123 decision diagram hyper graph shown in Figure 5 was used for both sum and carry outputs. By converting this graph to the circuit equivalent, the 1 bit cells shown in Figure 6 and Figure 7 were obtained. Equation (2) shows the sum output of a full adder.

$$F = X_1.\overline{X}_2.\overline{X}_3 + \overline{X}_1.X_2.\overline{X}_3 + \overline{X}_1.\overline{X}_2.X_3 + X_1.X_2.X_3 \quad (2)$$

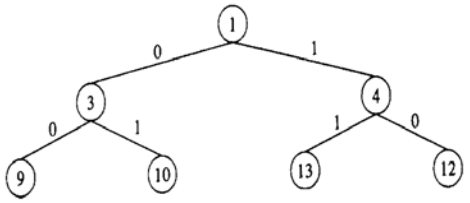

Figure 4. 123 decision diagram for both full adder blocks

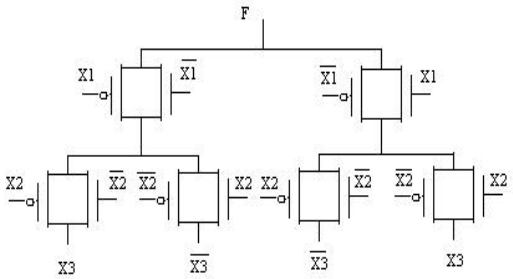

Figure 5. The summation unit

The circuit in Figure 6 realizes the function F in equation (2). The circuit in Figure 7 realizes the carry out equation (3) of a full adder.

$$C = X_1.X_2 + X_1.X_3 + X_2.X_3 \quad (3)$$

The variable X_1 represents A input, X_2 represents B input, and X_3 represents carry input (C_{in}) in Figure 8.

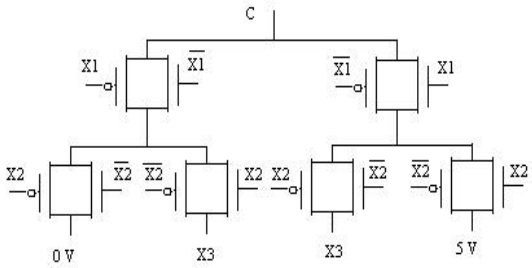

Figure 6. The carry out unit

Output of the Figure 7 is the carry out bit to enter next full adder block as carry in bit.

Combination of Figure 6 and Figure 7 build a 1 bit full adder circuit, and combination of four 1 bit full adders build 4 bit adder circuit as shown in Figure 8.

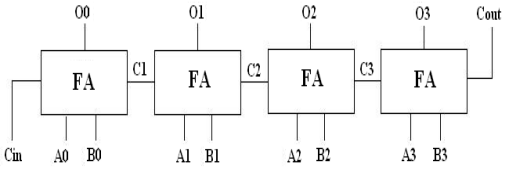

Figure 7. Combination of unit blocks

4. THE SIMULATION RESULTS

The designed circuit has YITAL 1.5 μ process parameters and simulated with Tanner Tools TSPICE. The input and output signals shown in Figure 8 are used with the same name. The most significant bits for inputs are A_3, B_3 and for outputs is O_3.Totally, 59 CMOS transistors were used. 11 of them were used as inverters. The following figures show the obtained simulation results.

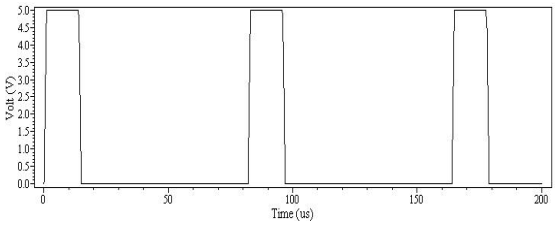

Figure 8. Carry-in (Cin) input signal

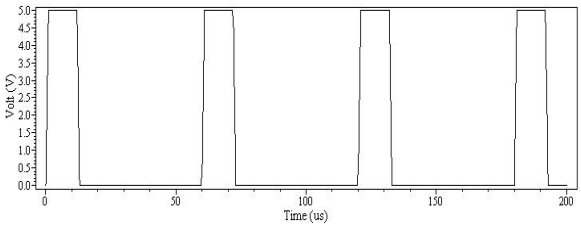

Figure 9. A0 input signal

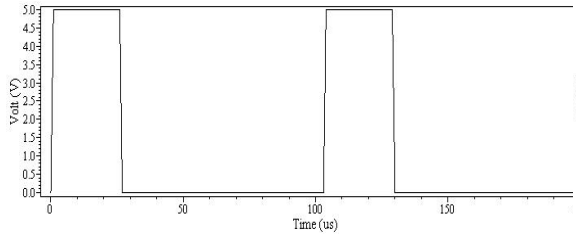

Figure 10. B0 input signal

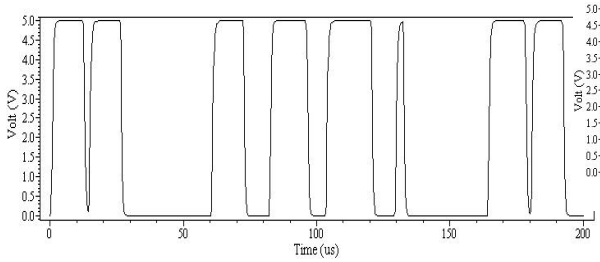

Figure 11. O0 output signal

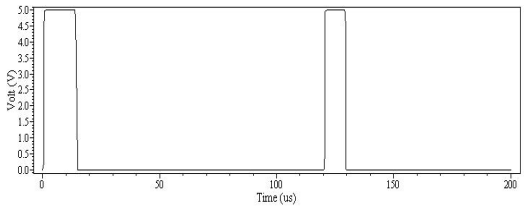

Figure 12. C1 internal carry out signal

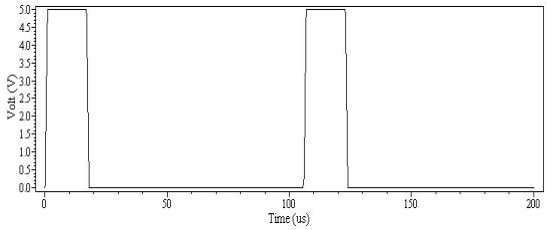

Figure 13. A1 input signal

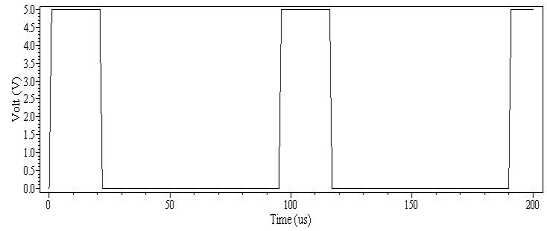

Figure 14. B1 input signal

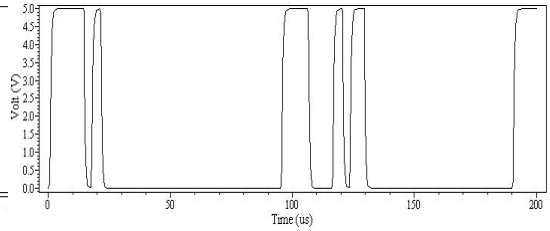

Figure 15. O1 output signal

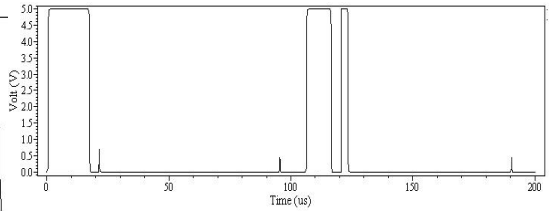

Figure 16. C2 internal carry out signal

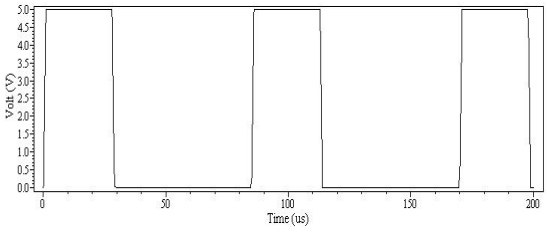

Figure 17. A2 input signal

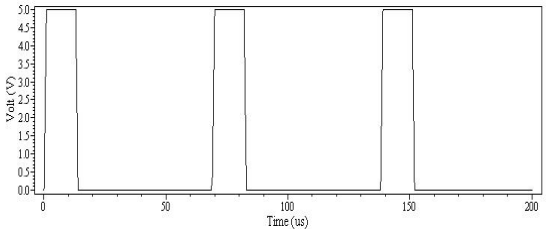

Figure 18. B2 input signal

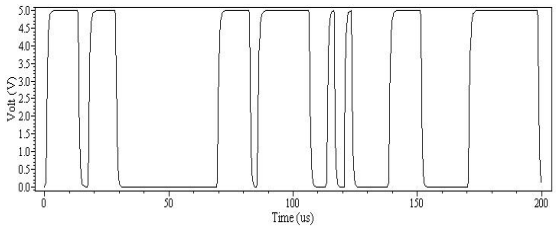

Figure 19. O2 output signal

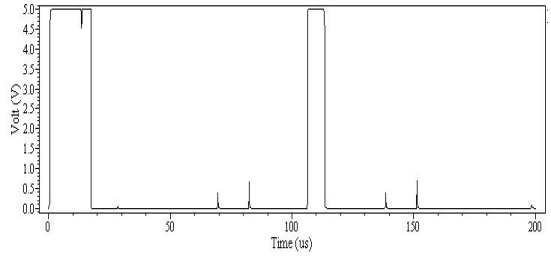

Figure 20. C3 internal carry out signal

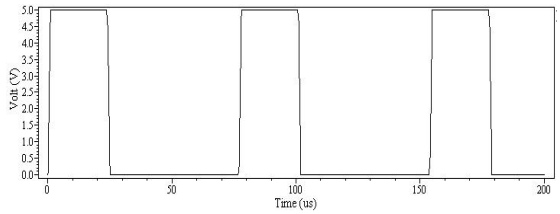

Figure 21. A3 input signal

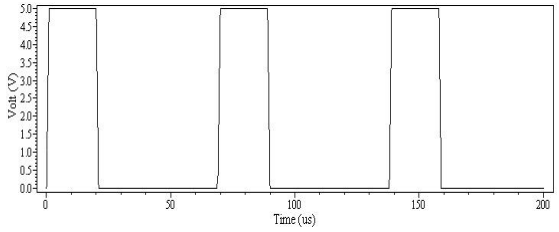

Figure 22. B3 input signal

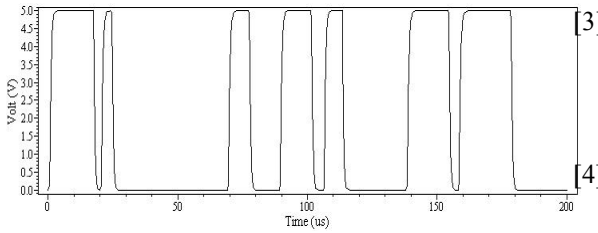

Figure 23. O3 output signal

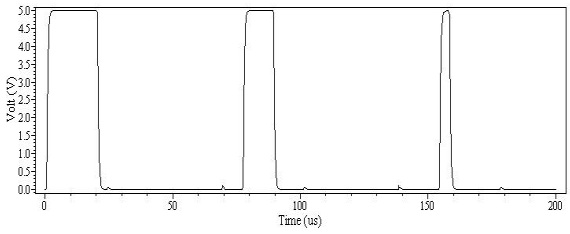

Figure 24. Carry out (Cout) output signal

5. CONCLUSION

The simulation results prove that the 123 decision diagram is efficiently adapted to CMOS pass transistor logic circuit design. Although, the main target for the 123 decision diagram is NMOS pass transistor logic circuits with restoring CMOS buffers, CMOS pass transistor circuit design is successfully done without restoring buffers. Silicon area economy, speed and low power consumption advantages of PTL circuits combined with 123 decision diagram and adapted to CMOS design. This metod is applicable for design of digital signal processing (DSP) chips.

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