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THE SECOND ORDER LOW PASS FILTER DESIGN WITH A NOVEL HIGHER PRECISION SQUARE-ROOT CIRCUIT

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ABSTRACT

In this paper a current-mode square-root circuit with reduced short-channel effect is designed and a second order low pass filter is proposed employing the section designed. The circuit proposed is suitable for standard CMOS fabrication and analog systems. The proposed filter circuit has been simulated with SPICE simulator using 0.35 µm CMOS technology parameters. It is observed that it decreases total harmonic distortion THD compared to classical filter employing stack-MOS current-mode square-root circuit.

Keywords: : *current mode square-root circuit, filtering in square-root domain, reducing MOSFETs short-channel effect.*

1. INTRODUCTION

Due to the trend towards using lower supply voltages, recently more researchers have interested in compressing-expanding (companding) techniques. The main advantages of the circuits employing this technique are large dynamic range and suitability for low voltage-low power applications [1-5].

Interest has been clearly focused on log-domain approaches, exploiting the exponential I-V law of bipolar devices or MOS transistors in weak inversion. In the strong inversion region, MOS transistors characteristics are described by a square law which is the basis for a class of translinear circuits termed square-root domain circuits [6-8]. In a lot of applications, square-root circuit is used by square-root domain circuits [9].

Nowadays, due to the decrease in dimensions of MOSFETs in IC fabrication technologies, second order effects such as short-channel effect causes more errors in the MOS transistor and square-root circuit performance[10].

In this paper a new current-mode square-root circuit that reduces short-channel effect is presented. A second order low pass filter employing this circuit is designed which decreases the total harmonic distortion THD compared to classical filter constructed with stack-MOS current-mode square-root circuit. The proposed circuit and low pass filter have been simulated with SPICE simulator using 0.35 µm CMOS technology.

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2. PROPOSED SQUARE-ROOT CIRCUIT

The conventional current-mode square-root circuit also known as geometric mean cell have two inputs and one output and three of them are in current form as shown in Figure 1.

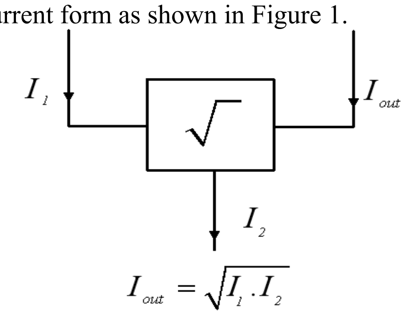

Figure 1. *Block diagram of the current-mode square-root circuit.*

Assuming that the aspect ratios of the transistors satisfy the condition $\beta_1=\beta_2=\beta$ and $\beta_3=\beta_4=2\beta$ where β is the transconductance parameter of the PMOS, current-mode stack MOS square-root circuit can be implemented as illustrated in Figure 2.

I_1 and I_2 are the input currents and the output current I_{out} can be obtained at the output node of the circuit in Figure 2 as the square-root of the multiplying input currents. Decreasing dimensions of MOSFETs affects the accuracy of the output current [11].

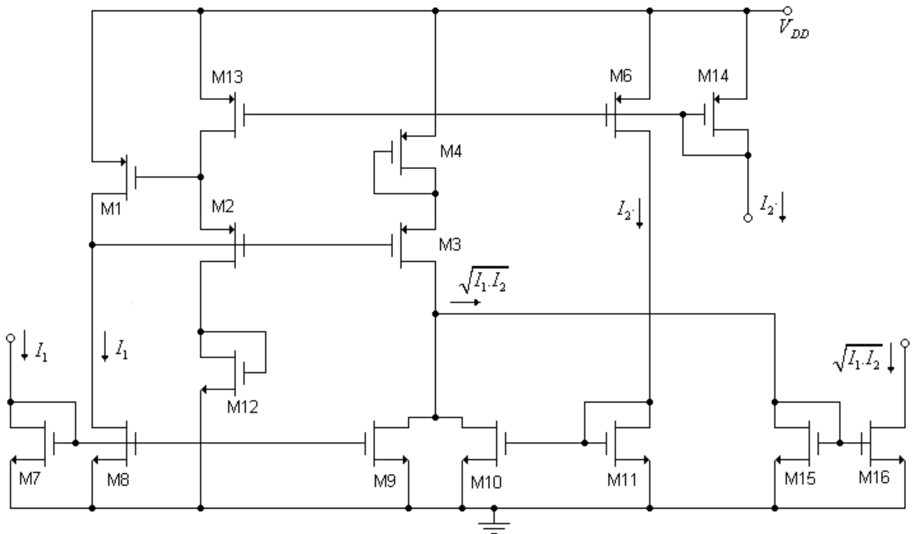

Figure 2. *Conventional current-mode stack MOS square-root circuit.*

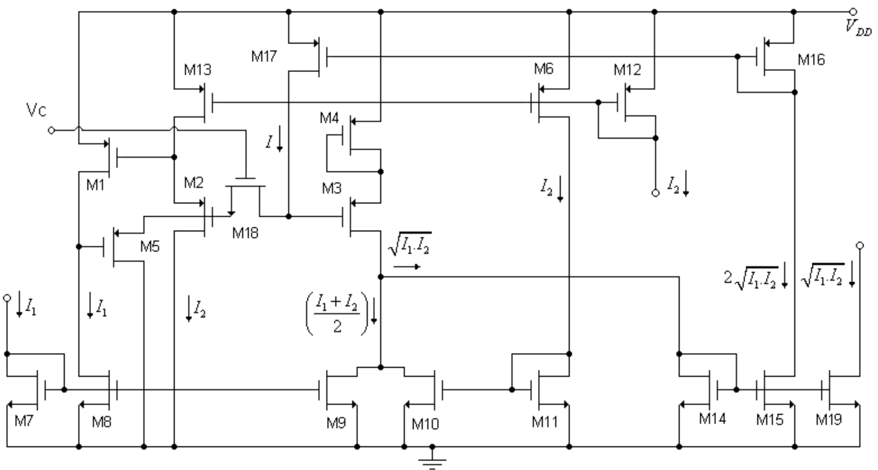

Figure 3. *Proposed higher precision current-mode stack MOS square-root circuit.*

The newly proposed high-precision current-mode stack MOS circuit reducing short channel effects can be realized as shown in Figure 3. The transistor M18 operates as a resistance where its value is controlled by the control voltage V_c. Thus output current function of the circuit can be controlled [12].

To verify the square-root circuit, SPICE simulations were performed using TSMC 0.35 µm LEVEL 3 CMOS process parameters for simulations. The device dimensions of transistors used in square-root circuit are shown in Table 1. The power supply voltage is 3V.

***Table 1**. Transistor dimensions (µm)*

	W	L		W	L		W	L
M1	3	.7	M8	6	.7	M15	12	.7
M2	3	.7	M9	3	.7	M16	6	.7
M3	6	.7	M10	3	.7	M17	12	.7
M4	6	.7	M11	6	.7	M18	6	.7
M5	6	.7	M12	6	.7	M19	6	.7
M6	6	.7	M13	6	.7			
M7	6	.7	M14	6	.7			

To obtain time domain SPICE simulation results of the proposed circuit, the input current I_1 is taken as a fix current of 1 µA and the current I_2 is applied as a triangular wave with an amplitude of 10 µA as shown in Figure 4.

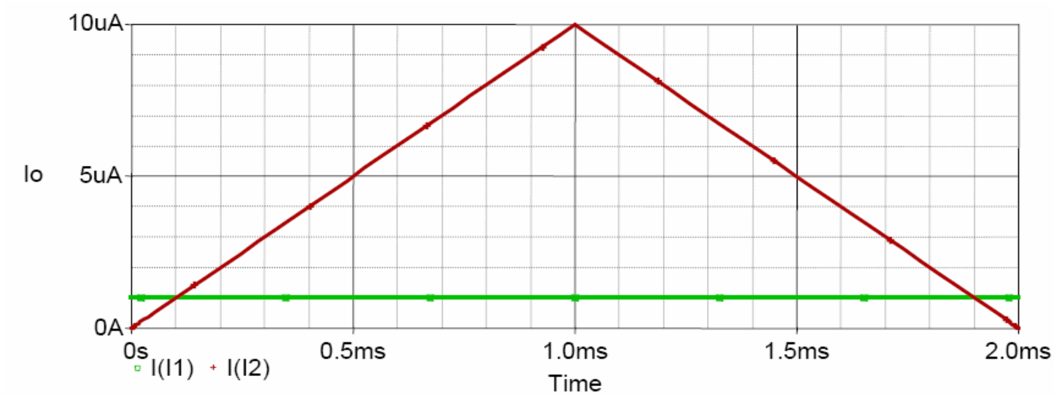

***Figure 4.** Input currents I_1 and I_2*

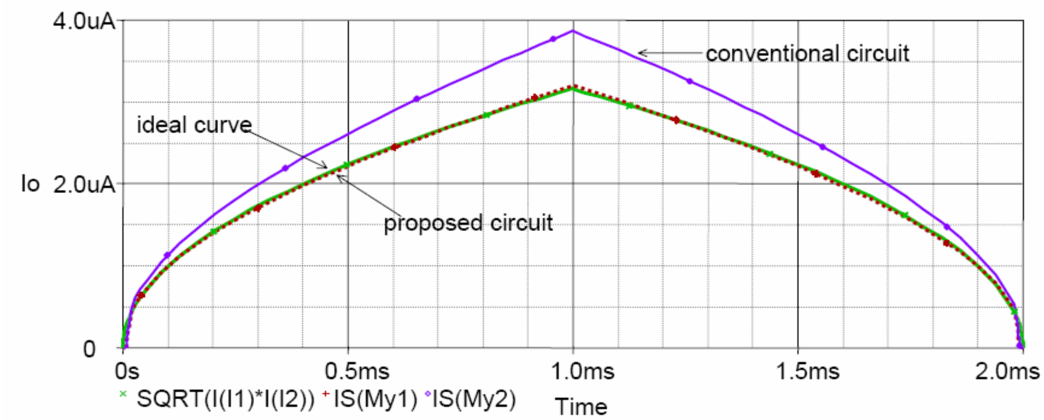

***Figure 5.** Comparison of output currents and ideal curve.*

The output currents of the circuit proposed and conventional circuit are observed and simulated with the ideal square-root function as shown in Figure 5.

The maximum current errors of the conventional circuit and the proposed circuit are about 0.71 µA and 0.04 µA, respectively. As expected, the characteristic of the output current of the proposed circuit shows approximately ideal square-root function. V_c control voltage is 2.55V.

3. SECOND ORDER LOW-PASS FILTER USING PROPOSED CIRCUIT

The transfer function of the second order filter can be written as;

$$H(s)=\frac{as^2+b\omega_o s+c\omega_o^{\,2}}{s^2+\left(\frac{\omega_o}{Q}\right)s+\omega_o^{\,2}} \tag{1}$$

Assuming that a=0, b=0 and c=1, this equation converts to the transfer function of the second order low-pass filter as;

$$H(s)=\frac{\omega_o^{\,2}}{s^2+\left(\frac{\omega_o}{Q}\right)s+\omega_o^{\,2}} \tag{2}$$

According to the state-space approach, the original transfer function can be mapped into the state-space equation as;

$$\begin{bmatrix}\dot{x}_1\\ \dot{x}_2\end{bmatrix}=\begin{bmatrix}0 & -\omega_0\\ \omega_0 & \frac{-\omega_0}{Q}\end{bmatrix}\begin{bmatrix}x_1\\ x_2\end{bmatrix}+\begin{bmatrix}\omega_0\\ 0\end{bmatrix}u \tag{3}$$

$$y=x_2$$

where x_1, x_2, y and u are state variables, output and input signals, respectively. Let the node voltage V_1 and V_2 be the state variables x_1 and x_2, where a voltage signal U denotes the input u, then the equation (3) can be rewritten as;

$$\begin{aligned}\dot{V}_1&=-\omega_o V_2+\omega_o U\\ \dot{V}_2&=\omega_o V_1-\frac{\omega_o}{Q}V_2\end{aligned} \tag{4}$$

$$y=V_2$$

Multiplying both sides of equation (4) with a constant C; we obtain

$$\begin{aligned}C\dot{V}_1&=-C\omega_o V_2+C\omega_o U\\ C\dot{V}_2&=C\omega_o V_1-C\frac{\omega_o}{Q}V_2\end{aligned} \tag{5}$$

$$y=V_2$$

For MOSFET operated in saturation region, voltages of the nodes can be expressed as;

$$I_1=\beta.(V_1-V_T)^2\Rightarrow V_1=\sqrt{\frac{I_1}{\beta}}+V_T \tag{6}$$

$$I_2=\beta.(V_2-V_T)^2\Rightarrow V_2=\sqrt{\frac{I_2}{\beta}}+V_T \tag{7}$$

$$I_U=\beta.(V_U-V_T)^2\Rightarrow U=\sqrt{\frac{I_U}{\beta}}+V_T \tag{8}$$

Substituting equation (6), (7) and (8) in (5), the following expressions can be written;

$$C\dot{V}_1=-C\omega_o V_2+C\omega_o U=C\omega_o\left(U-V_2\right)=C\omega_o\left(\sqrt{\frac{I_U}{\beta}}-\sqrt{\frac{I_2}{\beta}}\right)$$

$$\begin{aligned}C\dot{V}_2&=C\omega_o V_1-\frac{C\omega_o}{Q}V_2=C\omega_o\left(V_1-\frac{V_2}{Q}\right)\\ &=C\omega_o\left(\left(\sqrt{\frac{I_1}{\beta}}+V_T\right)-\frac{1}{Q}\left(\sqrt{\frac{I_2}{\beta}}+V_T\right)\right)\end{aligned} \tag{9}$$

$$y=V_2$$

The pole frequency ω_o can be tuned by changing the DC current as shown below;

$$I_o=\frac{C^2.\omega_o^2}{\beta}\Rightarrow\omega_o=\frac{\sqrt{I_o.\beta}}{C} \tag{10}$$

Thus, the state-space equation becomes;

$$\begin{aligned}C\dot{V}_1&=\sqrt{I_o.I_U}-\sqrt{I_o.I_2}\\ C\dot{V}_2&=\sqrt{I_o.I_1}-\frac{\sqrt{I_o.I_2}}{Q}+I_T\left(1-\frac{1}{Q}\right)\end{aligned} \tag{11}$$

$$y=V_2$$

According to the equation (11), square-root domain second order low pass filter can be realized by using three square-root circuits, two load capacitor, two DC bias current sources, three n-type MOSFETs and current-mirrors.

Figure 6 shows a circuit diagram of the square-root domain second order low pass filter. U is the DC biased input voltage and V_1 is the desired output voltage. The DC bias current I_o is used to control the position of cutoff frequency of filter [13, 14].

The DC bias currents are taken equal as I_{o1}=I_{o2} and changed from 0.2µA to 12.5µA for C_1=C_2=1pF. The gain-frequency curve of the second order low pass filter is shown in Figure 7, transient analysis of the filter is shown in Figure 8.

Three proposed current-mode square-root circuits are used in this filter structure. When I_o DC bias current is changed, cutoff frequency of the filter changes from 830KHz. to 4.63MHz. Thus f_{3dB} frequency of the filter can be adjusted in a frequency range of 3.8MHz. The pole frequency tuning range of the second order low pass filter is shown in Figure 9.

Total Harmonic Distortion (THD) curve of the second order low pass filter is illustrated in Figure 10. MATLAB graph is depicted for conventional square-root circuit and for the proposed square-root circuit respectively for frequency of the input signal f=100KHz and f=250KHz. As expected, THD values of the filter using the proposed circuit is less than THD values of the filter using the conventional circuit.

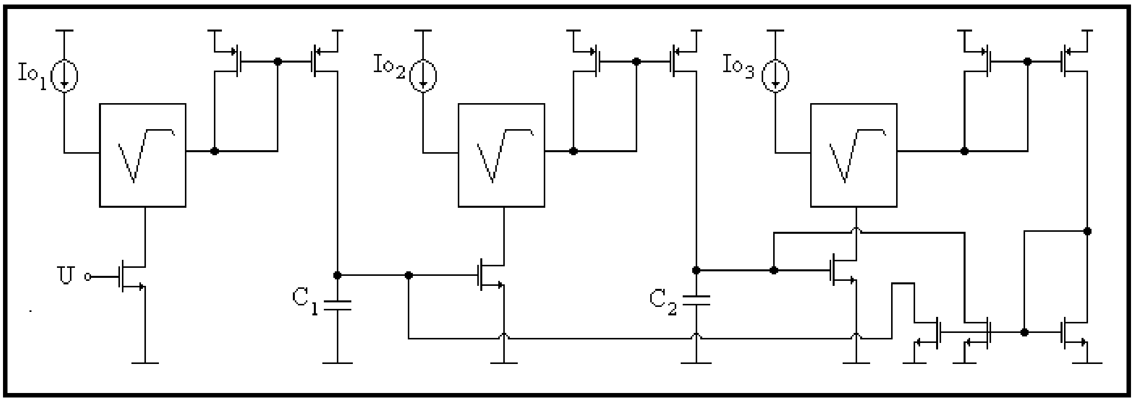

Figure 6. *Square-root domain second order low pass filter.*

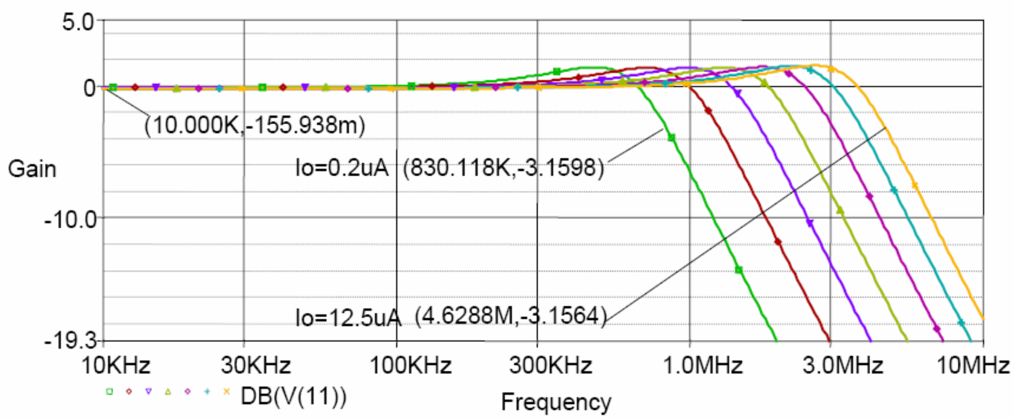

Figure 7*. Gain-frequency curve of the SRD second order low pass filter. (Io 0.2μA-12.5μA).*

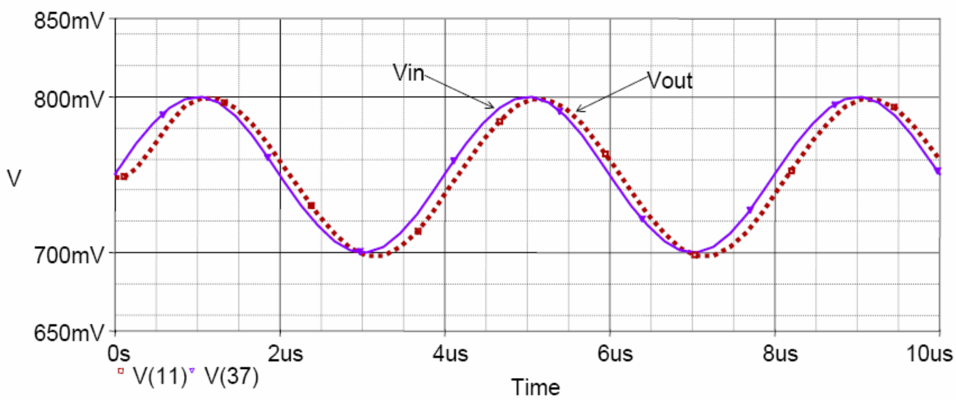

Figure 8. *Input and output voltages of the second order low-pass filter.*

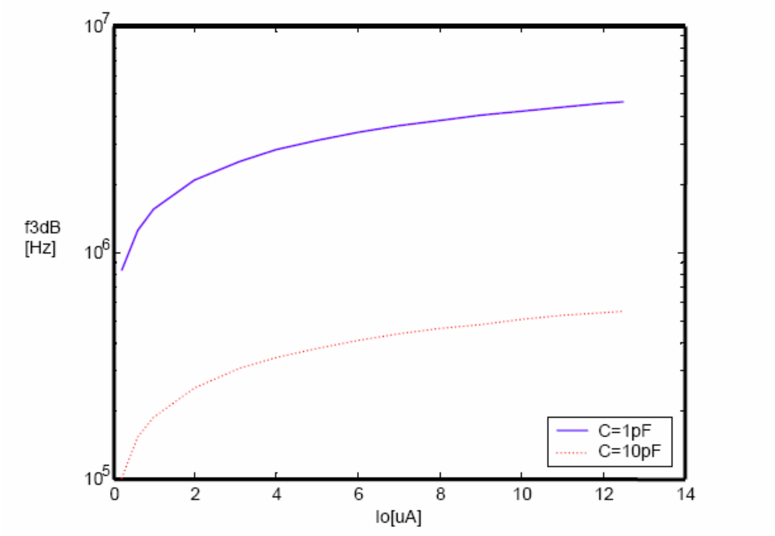

Figure 9. *Frequency tuning range of the filter.*

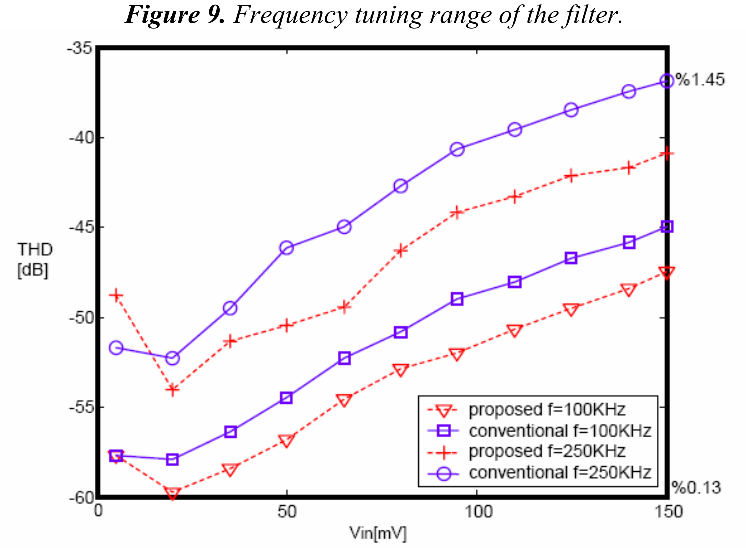

Figure 10. *Total Harmonic Distortion curves of the filter.*

4 . CONCLUSION

In this paper a novel high precision current-mode square-root circuit is proposed. The output current function can be controlled by the control voltage Vc. This circuit decreases the output current errors of the square-root circuit especially employing short-channel MOS transistors. A second order low pass filter using this circuit is designed. It decreases THD compared to filter employing conventional current-mode square-root circuit. When I_o DC bias current is changed from 0.2µA to 12.5µA, the cutoff frequency f_{3dB} of the filter can be adjusted in a frequency range of 3.8 MHz. for C=1pF. All circuits are analyzed with SPICE simulator using TSMC 0.35 µm CMOS technology. The topology proposed provides new possibilities in the design of analogue filters.

REFERENCES

[1] Adams R.W. “Filtering in the log-domain” in 63rd AES Conf., New York, 1979, preprint 1470.

[2] Frey D.R. “Exponential state-space filters: A generic current mode design strategy” IEEE

Trans. Circuits Syst. I, vol.43, pp.34-42, Jan.1996.

[3] Drakakis E.M., Payne A.J., Toumazou C., “Log-domain state-space: A systematic transistor-level approach for log-domain filtering”, IEEE Trans. Circuits Syst. II, vol.46, no.3, pp.290-305, Mar.1999.

[4] Drakakis E.M., Payne A.J., Toumazou C. “Log-domain filtering and Bernoulli cell” IEEE Trans. Circuits Syst. I, vol.46, no.5, pp.559-571, May 1999.

[5] Germanovix W., O’Neill G., Toumazou C., Drakakis E.M., Kitney R.I., Lande T.S. “Analogue micro powered log-domain tone controller for auditory prostheses”, Electr. Lett. Vol.34, no.11, pp.1051-1052, May 1998.

[6] Payne A., Toumazou C. “Linear transfer function synthesis using non-linear IC components” Proceedings ISCAS’96 Atlanta, USA, I, pp. 53-56.

[7] Mulder J., van der Woerd A., Serdjin W., van Roermund A. “A current-mode companding x-domain integrator” Electronics Letters 32, pp.198-199, 1996.

[8] Eskiyerli M., Payne A. “Square root domain filter design and performance” Analog Integrated Circuits and Signal Pocessing 22, pp. 231-243, 2000.

[9] Seevink E., Wiegerink R. “Generalized translinear circuit principle” IEEE Journal of Solid State Circuits 26, pp. 1098-1102, 1991.

[10] Tarcan R.C., Kuntman H. “A New Low Distortion Analog Multiplier“, AEU International Journal of Elec. and Communications, Vol.57, No.6, pp. 365-371, 2003.

[11] Menekay S., Tarcan R.C., Kuntman H. “A Novel Higher Precision Current-Mode Square-Root Cırcuit“, SIU’2006: IEEE 14.Signal Processing and Communication Applications Conference, (CD-ROM), 17-19 April 2006, Belek/Antalya-Türkiye.

[12] Menekay S., Tarcan R.C., Kuntman H. “Doğruluğu Artırılmış Kare-Kök Devresi İle Kurulmuş Düşük Gerilime Uygun İkinci Dereceden Alçak Geçiren Süzgeç Tasarımı“, ELECO’2006 Elektrik - Elektronik ve Bilgisayar Mühendisliği Sempozyumu, Bildiri Kitabı (Elektronik), s. 18-22, EMO Bursa Şubesi, 6-10 Aralık 2006, Bursa.

[13] Yu G.J., Chen J.J., Lin H.Y., Liu B.D., Huang C.Y., ”A low-voltage low-power log-domain band-pass filter”, in Proc. Int.Symp. on VLSI Tech.,Syst. And Applications, Hsinchu, Taiwan, April 23-25, 2003

[14]Chen J.J.”Design and Hardware Implementation of the Low Voltage Square Root Domain Filters” Thesis for Master of Science, Department of Electrical Engineering National Cheng Kung University Tainan, Taiwan, R.O.C., June 2003.