

# A HIGH-SPEED CMOS CURRENT COMPARATOR SUITABLE FOR ALGORITHMIC ANALOG-TO-DIGITAL CONVERTERS

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## **ABSTRACT**

*This paper introduces a high-speed high resolution CMOS current comparator which is used in an algorithmic Analog-to-Digital Converter (ADC) and implemented with a 0.6  $\mu\text{m}$  standard CMOS process. Circuit occupies 170 x 80 $\mu\text{m}^2$ . Proposed circuit performs comparison over a precision of 10-bit at a 100MHz clock within the 0-250  $\mu\text{A}$  input current range. Power consumption is less than 500  $\mu\text{A}$ .*

**Keywords:** Comparators, Analog-Digital Converters, current-mode circuits.

## **1. INTRODUCTION**

The comparator is a crucial and often a limiting component in the design of high-speed data conversion systems due to its accuracy, comparison speed, and area and power consumption those of which affects the ADC performance such as SFDR, ENOB, DNL. This paper presents the design of an area-efficient and high-speed CMOS comparator appropriate for use in current-mode algorithmic ADCs.

The current-mode algorithmic ADC was first proposed by Nairn and Salama [1] where circuits take their inputs in current-mode and the difference of these currents are used to decide on the concerned stage's output. This decision is generally performed with comparators, either voltage or current-mode.

Because the comparators based on regenerative flip-flops can achieve higher speeds than other topologies, regenerative current input comparators seem to be the most efficient way to perform decision.

A comparator based on regeneration was introduced in voltage-mode [2]. The current-mode equivalent for which current inputs are

applied directly to the cross-coupled stage of the regenerative flip-flop was also published [3]. Even though both circuit topologies achieve high-speed, they only provide moderate accuracy and they are less likely to be suitable for current-mode algorithmic ADCs.

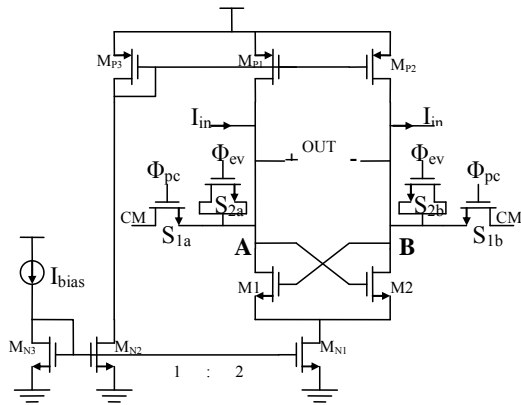
## **2. PROPOSED DESIGN**

The proposed current comparator is shown in Fig. 1. The inputs are applied as current and same nodes are used for outputs as voltage. In this work, instead of applying two currents ( $I_1$  and  $I_2$ ) individually, current differences  $I_1 - I_2$  and  $I_2 - I_1$  are used for comparison. These current differences will be called  $I_{in}$  and  $-I_{in}$ . The architecture is based upon a differential current input topology. The transistors  $M_1$  and  $M_2$  form the cross-coupled pair, namely the regenerative stage. During the precharge phase, switches  $S_{1a}$  and  $S_{1b}$  are used to set the outputs to the common mode, CM (typically  $V_{DD} / 2$ ). Dummy switches  $S_{2a}$  and  $S_{2b}$  are used for eliminating the charge injection during switching. The comparator operates with two clock phases, namely precharge (*Pre\_ch*) and evaluation (*Eval*), which are inverse of each other. The differential stage is

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biased with a bias current of  $2 I_{bias}$  so as to ensure that each branch current will be  $I_{bias}$ .



**Figure 1.** The proposed current comparator.

The circuit operates as follows: Assuming that  $I_{in}$  is positive, as soon as this current is applied to the node A, in the evaluation phase, because of the equal bias currents, the drain voltage of  $M_1$  and the gate voltage of  $M_2$  (node A) will tend to increase to sink this current. A small deviation in gate voltage of  $M_2$  causes a deviation in the drain voltage of  $M_2$  and the gate voltage of  $M_1$  (node B). This positive feedback is carried out so that the differential voltage output (A-B) reaches a value, which can be perceived as a logic level. After comparing the currents, comparator inputs are pre-charged with *Pre\_ch* to the CM and the next comparison starts with *Eval*.

It must be noted that each comparison cycle needs a pre-charge phase. If the fixed output voltages, i.e., nodes A and B, deviate from the CM voltage of 2.5V for  $V_{DD}$  of 5V due to the switching errors, small current differences may not be sensed by the cross-coupled transistor pair properly and the output may go to an undesired logic level. In order to prevent this, a Schmidt Trigger circuit can be used. The hysteretic behavior of the circuit relaxes the output deviations and allows the output change during transients within its hysteretic interval, which is set to 500mV for this work.

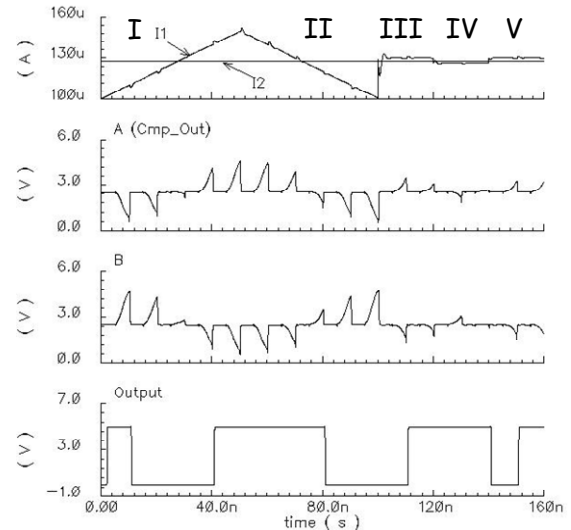
In order to test the proposed current comparator, different cases are generated which are common for comparator tests. Those are as follows:

- I. One input is kept constant and the other is swept within the input range, from low to high.
- II. One input is kept constant and the other is swept within the input range, from high to low.
- III. The input is changed from maximum difference of inputs to one LSB difference.

IV. The input is changed from minimum positive difference to minimum negative difference.

V. The input is changed from minimum negative difference to minimum positive difference.

The simulation results are shown in Fig.2, in which, each case is indicated.



**Figure 2.** Test case simulations for the comparator.

In order to obtain the difference currents cascode current mirrors are used in this design.

The current comparator has been used in a conventional 6-bit algorithmic ADC structure [1] shown in Fig. 2. Here,  $I_1$  is the analog input current which will be converted to digital.  $I_2$  is the reference current. Cascode current mirrors generate  $2I_1 - I_2$  and  $I_2 - 2I_1$  which are the input signals of the proposed current comparator. The input current  $I_1$  is multiplied by two and compared with the reference current  $I_2$ . If twice the input current is greater than the reference current, the comparator generates a digital code of "1", the switch at the output of the comparator turns on, and  $2I_1 - I_2$  is applied to the next stage as an input current. Otherwise, the comparator generates a digital code of "0", the switch at the output of the comparator turns off, and only  $2I_1$  is applied to the next stage. The resolution of the ADC is determined by the number of this ADC cell.

In this work, 6 stages are used, which corresponding to 6-bit and the prototype has been fabricated in AMS 0.6 $\mu$ m standard (double-poly, double-metal) CMOS process. The 6-bit ADC prototype has also been tested and characterized. ADC consumes 1mA of current and DNL/LNL is less than 0.5LSB.

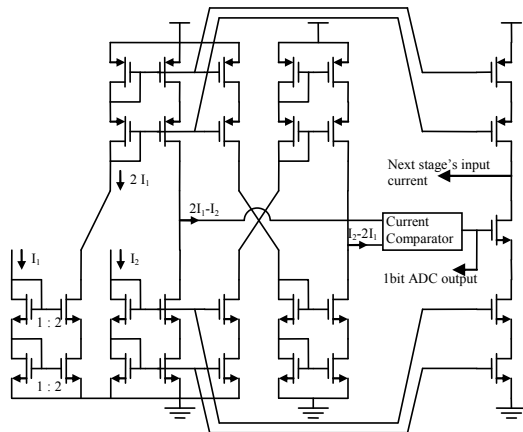


Figure 3. Algorithmic ADC cell.

Fig. 4 shows the ADC chip photo.

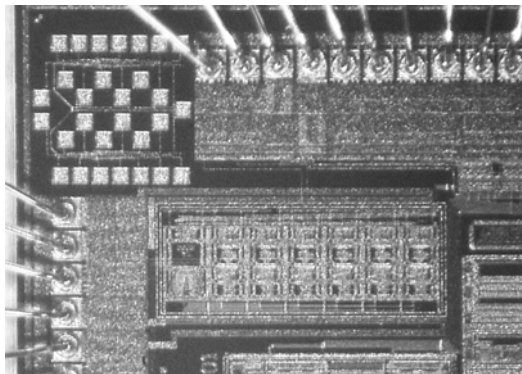


Figure 4. 6-bit ADC chip photograph.

### 3. CONCLUSION

In this work, high-speed, high-resolution, area-efficient CMOS current comparator which is used in an algorithmic Analog-to-Digital Converter (ADC) was implemented with a 0.6  $\mu\text{m}$  standard CMOS process. The circuit occupies an area of 170  $\mu\text{m}$  x 80 $\mu\text{m}$ . The proposed circuit performs comparison over a precision of 10-bits at a 100MHz clock rate for an input current range of 0-250  $\mu\text{A}$ . If the bias current is clocked, comparator can also operate at higher speed. This modification will be included in another paper.

#### REFERENCES

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