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IMPLEMENTATION OF THE UPFC CONTROLLER TEST EQUIPMENT

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Abstract: *This paper instructs the test equipment working principle of the unified power flow controller (UPFC), determines the datum should be sampled for the controlling and recording. Designs the hardware plate-form for the controller equipment. The plate-form is composed by controlling unit, supervising unit and recording unit. The test results, which based on the designed plat-form demonstrate, the implemented equipment can correspond to the power system variations smoothly and efficiently.*

Keywords: UPFC controller, test equipment, sampled parameters, controlling unit, test results

1 INTRODUCTION

Unified power flow controller (upfc) is one of the powerful flexible alternate current transmission system devices. There are many professors engaged in its theory study, in 1998, the first equipment was put in operation in INEZ substation in America[1, 2]. From then on, more and more researchers engaged in the test equipment study[3], but the succeful results have not been reported. This paper instructs the configure for the upfc connected into the simple power system, determines the sampled parameters and implements the test equipment.

2 WORKING PRINCIPLE OF THE UPFC TEST EQUIPMENT

The theory diagram of test equipment of UPFC connected into simple ac power system is shown in Fig.1. The voltage source converter (VSC1) is connected into power system through the coupling transformer T_{sh}; Voltage source converter (VSC2) is connected into power system through the coupling transformer T_{se}. When the bypass switcher (BYPBRK) is switched on, and the series switchers (SEBRK1, SEBRK2) switched off, VSC2 is connected into the power system. Otherwise, series converter VSC2 disconnected from the power system. When the shunt side switcher (SHBRK1) switched on, shunt converter VSC1 connected into the power system, otherwise, disconnected from the power system. When the dc side switcher (DCBRK) switched on, VSC1 and VSC2 are connected back-to-back through the dc capacitor, and operated in UPFC model; when DCBRK switched off, VSC1 and VSC2 operated in STATCOM and SSSC model respectively. In Fig.1, $V_i\angle\theta_i$, $V_j\angle\theta_j$, voltage magnitude and angle at the sending end and receiving end of the transmission line; $V_s\angle\theta_s$, the bus voltage of the UPFC shunt side, $V_R\angle\theta_R$, the bus voltage of the UPFC series output side; P_{sh} , Q_{sh} , the real power and reactive power exchanged between the power system and the UPFC shunt converter; P_L , Q_L , power flow in the transmission line;

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$V_{sh}\angle\theta_{sh}$, $V_{se}\angle\theta_{se}$, voltage magnitude and angle at the ac side of VSC1 and VSC2; I_{line} ,transmission line current; V_{dc} , dc side bus voltage.

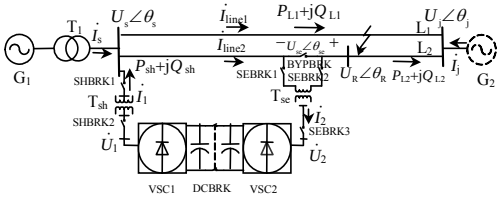

Fig.1 UPFC connected into the simple power system

3 IMPLEMENTATION OF THE CONTROLLER

3.1 SAMPLING PARAMETERS

For the function of the maintaining the bus voltage and regulating the power flow of the transmission line, in Fig.1, the analogy parameters that should be sampled are: the connected to the bus voltage of the UPFC shunt side, $\dot{U}_{\mathrm{s}}$ ($U_{\mathrm{s}}\angle\theta_{\mathrm{s}}$) , the output bus voltage of the UPFC series side, $\dot{U}_{\mathrm{R}}$ ($U_{\mathrm{R}}\angle\theta_{\mathrm{R}}$), transmission line current, $\dot{I}_{\mathrm{line2}}$, the output voltage of the UPFC series side, the current of $\dot{I}_{1}$, which output from the shunt side of UPFC, and the DC voltage of the capacitor, U_{dc} . In case of the unbalance of three-phase load, all of the sampled parameters are three phase values. The sampling frequency is 800Hz, that means, in one period there are 16 sample dots.

The digital datum that should be sampled are the bypass switch of the series side, BYPBRK, connecting the series converter to the system, SEBRK1 and SEBRK2, connecting the shunt side converter to the power system, SHBRK1, and the DC switch DCBRK. Where, BYPBRK, SEBRK1, SEBRK2 and SHBRK1 are three-phase alternative magnetic switch. The entire output digital datum is corresponding to the input digital datum.

3.2 CONTROL SYSTEM

The controller test equipment is designed as shown in Fig.2. Which composed by supervisor unit, recorder unit and control unit. The supervisor computer communicates with the recorder unit and the control unit through RS-232 and RS-485. And the communication with VSC1 and VSC2 is implemented by RS-232. The supervisor computer is the master and the equipment computers are the slaver.

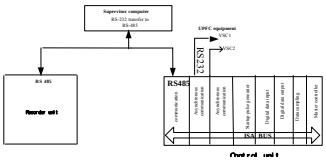

Fig.2 implementation block diagram of UPFC controller

The TMS320F240 is used as bus driving board chipset, which responds for the data exchanging, sending the sampling data in the multiple Chunnel and the input data of the switcher, together with the state data of the UPFC equipment, to the master computer through the asynchronous communication board, in addition to that, also transfers the query and control commands sent out by the master computer the switcher output board or UPFC equipment. The TMS320F206 is used in the controllers communicated with the UPFC equipment, these two control boards respond for the calculation of the single neural adaptive PID control algorithm and the data exchanging, as well as sending the calculation results to the UPFC equipment through RS-232 channel. The data sampling frequency of the recorder unit is 1.2 kHz. Record time is

20s. The CPU in record unit is TMS320F206.

4 TEST SIMULATIONS

4.1 PARAMETERS SETTING[4, 5]

For Fig.1, S_{G1}=15kVA, the output terminal voltage of the generator is 230v, *Xd*=0.56, *Xd'*=0.132, *Xd"*=0.113, *Xq"*=0.135.The capacity of transformer T1 is 15kVA, the reactance when without load is 5Ω, connected in the manner of Y/Δ-11,the voltage of the winding1 is 230v, and the winding2 is 800v. the voltage of the transmission line is 800v, the longer is 260km, r=0.8233x10^{-5}Ω/m, x_L=0.924x10^{-4}, x_c=95.867MΩ*m.the inner reactance of the infinite bus is 0.87Ω, short circuit capacity is 100kVA.For the consideration of the max load, the designed UPFC capacity is 15kVA, both of the series side and shunt side converter capacitor is 7.5kVA. The DC voltage is 400v. both side of the transformer capacity is 10kVA, the transformer of the shunt side is connected in Y/Δ-11, transfer property is 2.5:1, for the consideration of more flexibility, the tapers of the series transformer are 3, when the voltage compensator is 30-50%, the property is 10:8, 15-30% is 6:8 and 0-15% is 3:8. the controller algorithm is PI[6, 7], $k_{T1}=10$, $k_{p1}=0.04$; $k_{T2}=11$, $k_{p2}=0.04$; $k_{T3}=1$, $k_{p3}=0.02$; $k_{T4}=1, k_{p4}=0.02$。

4.2 TEST RESULTS

For the testing of the designed equipment, there are some testing results. One is the variation of the real power and reactive power varied from 1kw to 3kw and 1kvar to 3kvar. The variation curve is shown in Fig.3, the yellow is for the real power and the blue is for the reactive. The other one is in the output bus of UPFC series side, in 16.441s the 44Ωload is switch on and 17.125s is switch off.

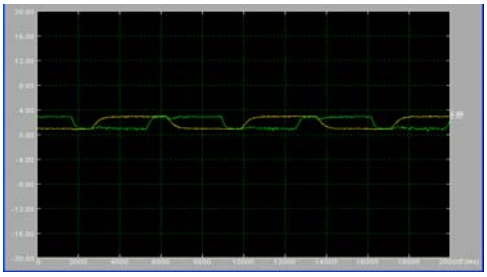

Fig.3 Power flow variation in the line2

5 CONCLUSIONS

This paper presents the test equipment working principle detailed. From the working principal diagram, determines the datum that should be sampled in the controller, and then designs the controller systems and presents the controller systems configure and the chips that used in the designed plat-form. Based on the designed plat-form, power flow variations in the transmission line2 and load switch on and off the power system test simulations are made, the results shows, the designed plat-form can correspond to the variations immediately and effectively.

6 REFERENCE

[1] C. Schauder, L. Gyugyi, E. Stacey, M.Lund, AEP UPFC project: installation, commissioning and operation of the ±160MVA statcom (phase I) [J]. *IEEE Transactions on Power Delivery*, Vol: 13, No: 4, pp. 1530-1535, 1998.

[2] Manzar Rahman, Mohammed Ahmed, Richard Gutman, "UPFC Application on the AEP System: Planning Considerrations". *IEEE Transactions on Power Systems,* Vol. 12, No. 4, P1695-1701. November 1997.

[3] Tan Weipu, He Renmu, Yang Yihan, Liu Zhuo, Application of Digital Signal Processor on UPFC Experimentation Device [J]. *Power System Technology*, Vol: 23, No: 8, pp. 17-20, 1999.

[4] N. Dizdarevic, S. Tesnjak, G. Andersson,

"Converter Rating Powers of Unified Power Flow Controller". *IEEE proceedings*, P603-609. 2002.

[5] Tang Aihong, Cheng Shijie, etal. Design of Parameters of UPFC Equipment [J]. *High Voltage Engineering*. Vol: 31, No: 6, pp. 63-65, 2005.

[6] Aihong TANG, Shijie CHENG. Study of the Impacts of UPFC Upon Dynamic Power Quality [J]. *Istanbul University-Journal of Electrical&Electronics Engineering*, Vol: 5, No: 1, pp.1239-1240, 2005.

[7] Tang Ai-hong, Cheng Shi-jie. DYNAMIC SIMULATION MODEDL OF UNIFIED POWER FLOW CONTROLLER BASED ON PSCAD/EMTDC [J]. *Power system technology*, Vol: 29, No: 16, pp.6-10, 2005.

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