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A STUDY TO IMPROVE SYMMETRICAL CMOS OTA BEHAVIOUR IN SUBTHRESHOLD REGION

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ABSTRACT

The current transfer characteristic of the CMOS symmetrical OTA, operating in the subthreshold region, depends much more on channel length modulation then operating in the strong inversion region. In this paper a new method is proposed to reduce the dependence on channel length modulation and to improve the OTA behaviour by changing one of the MOS transistor dimensions in the CMOS symmetrical OTA. The result is proven by SPICE simulations and by measurements.

Keywords: *CMOS OTA, Low power building blocks, Subthreshold region*

1. INTRODUCTION

In the recent years, the use of analog circuit structures with MOS (Metal Oxide Semiconductor) transistor operating in subthreshold region becomes more importance [1]. The main reason for this is the rapid increasing use of battery-operated portable equipment especially in the medical electronics. However, battery-operated portable equipment must be long-lived. Therefore, the ICs (Integrated Circuit) used in the equipment must operate with low voltage and low power. At this point of view, the MOS transistors, operating in subthreshold region, provides both of them. The MOS transistors, operating in subthreshold region, can operate up to 1.5V with only few nA. Therefore, device sizes can be scaled-down without increased electric field because of the low voltage. Scale-down is one effective method of reducing the cost of IC products in that more components are integrated on a single chip with the same efforts and costs. Furthermore, the parasitic capacitances are reduced and the MOS devices transconductance increases. Therefore, it is useful for implantable bioelementric applications.

In the first part of this study, the output current function of the CMOS (Complementary Metal Oxide Semiconductor) symmetrical OTA

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(Operational Transconductance Amplifier) operating in subthreshold region will be found [1,2]. In the second part, it will be investigated that which term of the output current function especially cause for the unsymmetrical current transfer characteristic. In the last part of this study, it will be discuss how the symmetrical current transfer characteristic can be provided.

2. SUBTHRESHOLD OPERATION

The MOS transistor behaviour in the strong inversion region is represented by the square-law functions. The linear region occurs for $V_{GS}>V_{TH}$ and $V_{GS}-V_{TH}\geq V_{DS}$ where the drain current is expressed as

$$I_D=\frac{W}{L}\cdot\mu\cdot C_{ox}\cdot\left[\left(V_{GS}-V_{TH}\right)\cdot V_{DS}-\frac{V_{DS}^2}{2}\right] \quad (1)$$

$$\cdot\ \left(1+\lambda\cdot V_{DS}\right)$$

The saturation region occurs for $V_{GS}>V_{TH}$ and $V_{DS}\geq V_{GS}-V_{TH}$ where the drain current is given by

$$I_D=\frac{1}{2}\cdot\frac{W}{L}\cdot\mu\cdot C_{ox}\cdot\left(V_{GS}-V_{TH}\right)^2\cdot\left(1+\lambda\cdot V_{DS}\right) \quad (2)$$

where W and L represent the channel width and the channel length, μ and C_{OX} represent the mobility of the carriers in the channel and the oxide capacitance and λ is the channel length modulation parameter of the MOS transistor [1,2,3,4,5].

There also exists a region near the threshold voltage where the drain current depends exponentially on V_{GS}. This region is called weak inversion or subthreshold region. The most important point about subthreshold current is that $V_{GS}<V_{TH}$ does not give $I_D=0$. In the weak inversion or subthreshold region the current-voltage relation is expressed by

$$I_D=I_{ON}\cdot\exp\left[\left(V_{GS}-V_{ON}\right)\cdot\left(\frac{q}{n\cdot k\cdot T}\right)\right] \quad (3)$$

$$n=1+\frac{q\cdot N_{FS}}{C'_{OX}}+\frac{C_D}{C'_{OX}} \quad (4)$$

where I_{ON} is the current in the strong inversion for $V_{GS}=V_{ON}$, V_{ON} is the voltage which acts as a boundary between the weak and strong inversion, q is the electronic charge, k is the Boltzmann constant, N_{FS} is the number of fast surface states per volt, C_D is the capacitance associated with the depleted region and C'_{OX} is the oxide capacitance per unit area. Applying (3) to the transistors of the CMOS symmetrical OTA illustrated in **Figure 1** we find two distinct functions for the output current. One of them is for the positive output current (I_{OUT}^+) related to the transistors M_2, M_4 and M_6 in which the current flows (5) and the other is for the negative output current (I_{OUT}^-) related to the transistors M_1, M_3, M_5, M_7 and M_8. It is obvious that the channel length modulation has a direct effect to the output current as follows:

$$I_{OUT}^+=\frac{KP_P}{2}\cdot\left(\frac{W}{L}\right)_6\cdot\left(V_{ON_P}-V_{TH_P}\right)^2\cdot\exp\left\{\left(\frac{q}{n_p\cdot k\cdot T}\right)^2\cdot\ln\left[\frac{I_B\cdot\left[\left(\frac{W}{L}\right)_6\Big/\left(\frac{W}{L}\right)_4\right]}{\frac{KP_P}{2}\cdot\left(\frac{W}{L}\right)_4\cdot\left(V_{ON_P}-V_{TH_P}\right)^2\cdot\left(1-\lambda_P\cdot V_{DS_4}\right)}\right]\right\} \quad (5)$$

$$I_{OUT}^{-}=\frac{KP_N}{2}\cdot\left(\frac{W}{L}\right)_8\cdot\left(V_{ON_N}-V_{TH_N}\right)^2\cdot\exp\left\{\left(\frac{q}{n_N\cdot k\cdot T}\right)^2\cdot\ln\left[\frac{\frac{KP_P}{2}\cdot\left(\frac{W}{L}\right)_5\cdot\left(V_{ON_P}-V_{TH_P}\right)^2\cdot\left(1-\lambda_P\cdot V_{DS_5}\right)}{\frac{KP_N}{2}\cdot\left(\frac{W}{L}\right)_7\cdot\left(V_{ON_N}-V_{TH_N}\right)^2\cdot\left(1+\lambda_N\cdot V_{DS_7}\right)}\cdot\exp\left(\left(\frac{q}{n_p\cdot k\cdot T}\right)^2\cdot\ln\left(\frac{I_B\cdot\left[\frac{\left(\frac{W}{L}\right)_5}{\left(\frac{W}{L}\right)_3}\right]}{\frac{KP_P}{2}\cdot\left(\frac{W}{L}\right)_3\cdot\left(V_{ON_P}-V_{TH_P}\right)^2\cdot\left(1-\lambda_P\cdot V_{DS_3}\right)}\right)\right)\right]\right\} \quad (6)$$

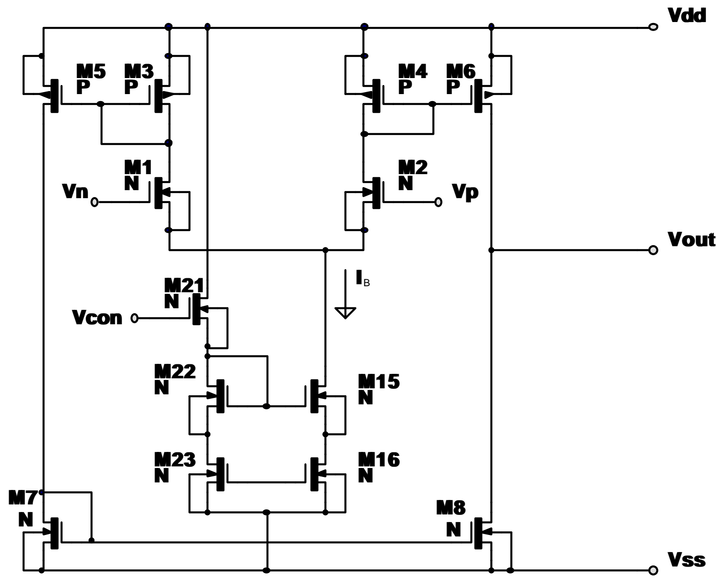

Figure 1. Structure of the CMOS symmetrical OTA.

where $KP_P=\mu_P\cdot C'_{OX_P}$, $KP_N=\mu_N\cdot C'_{OX_N}$ and I_B is the biasing current of the OTA.

3. CHANNEL LENGTH MODULATION

The current of the MOS transistor operating in the subthreshold region is diffusion current. The channel length modulation effect is caused by the shortening of the effective channel length of the transistor because of an increase in the drain depletion region as the drain voltage is increased. As the drain voltage is increased further, the width of the depletion region near the drain will also increase as illustrated in Figure 2. This phenomenon of the effective channel length shortening is known as the channel length modulation and is modelled by

$$I_D=I_0\cdot\frac{L}{L-L_D} \quad (7)$$

where I_0 is the drain current without any channel length shortening (L_D=0), L is the length of the channel and L_D is the length of the channel shortening between the drain and the point G illustrated in Figure 3. For weak inversion the formulation of the distance L_D by Poisson's equation gives

$$L_D=K_2\cdot\left[\sqrt{V_{DS}+\phi_D}-\sqrt{\phi_D}\right] \quad (8)$$

$$K_2=\sqrt{\frac{2\cdot\varepsilon_{Si}}{q\cdot N_{eff}}} \quad (9)$$

where ϕ_D is the contact potential across the pn junction, ε_{Si} is the permittivity of silicon and N_{eff} is the effective doping of the channel region.

For the strong inversion region the drain current of the MOS transistor is a drift current. The channel length modulation depends here on the pinchoff point, which moves away from the drain as the drain voltage is increased. Therefore, the effective channel length decreases and influences the drain current. This effect on the drain current can be modelled by the Eq. (10), which is the same model as it is used for the subthreshold current:

$$I_D = I_{DS} \cdot \frac{L}{L - L_D} \tag{10}$$

Here, L_D is the distance from the pinchoff point to the drain, as illustrated in Figure 4. The electric field tangent to the channel at the pinchoff point P is defined as the pinchoff field E_G. The channel length shortening L_D is calculated such that the electric field at point P is the pinchoff field. The length of the field line from the drain to point P is given as τ where $\tau = L_D \cdot F$. F is the geometry factor that accounts for the path from the drain to point P not being next to the surface. The formulation of the L_D distance by Poisson's equation along the path from the drain to point P gives

$$L_D = \frac{K_2}{F}\left[\sqrt{V_{DS} - V_{DSS} + \left(\frac{E_G \cdot K_2}{2}\right)^2} - \frac{E_G \cdot K_2}{2}\right] \tag{11}$$

$$V_{DSS} = V_{DS} - \left(E_G \cdot \tau + \frac{q \cdot N_{eff} \cdot \tau^2}{2 \cdot \varepsilon_{Si}}\right) \tag{12}$$

$$E_G \approx \left(\frac{2 \cdot I_{DS}}{L \cdot \beta_0 \cdot K_2^2}\right)^{1/3} \tag{13}$$

where V_{DSS} is the pinchoff voltage at point P and β_0 is the conductance coefficient in strong inversion region.

The channel length shortening in the subthreshold region described in (8) depends much more on the drain source voltage than the case of the strong inversion region described in (11). Furthermore, the channel modulation affects the drain current in subthreshold region rather than the drain current in the strong inversion region.

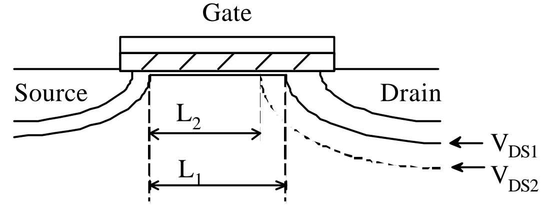

Figure 2 Dependece of depletion region on drain-source voltage, $V_{DS2} > V_{DS1}$, $L_2 < L_1$

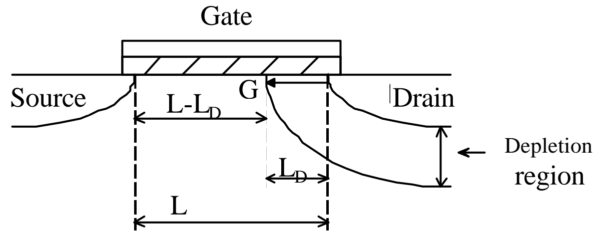

Figure 3. L_D is the width of the drain depletion region from the drain to the point G.

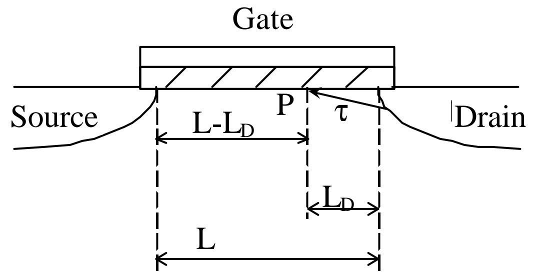

Figure 4. L_D is the distance from the drain to the pinchoff point.

4. METHOD TO IMPROVE THE BEHAVIOUR IN SUBTHRESHOLD OPERATION

The SPICE simulation of the CMOS symmetrical OTAs (Figure 1) current transfer characteristic for the subthreshold region is shown in Figure 5. The MOS transistor dimensions and the model parameters are shown in Table 1 and Table 2, respectively. The CMOS OTA is realized with TUBITAK 3μ technology. Note that the OTA is design with conventional rules.

From Figure 5 it can be seen that in the subthreshold region the characteristic is nonsymmetrical, namely $\left|I_{out}^{+}\right| = 9.28nA$ and $\left|I_{out}^{-}\right| = 13.2nA$. This phenomenon is due to the channel length modulation, which we have described above. To overcome this phenomenon and provide a symmetrical output current the (2) and (3) must be equalized. As a result, we obtain three different states to realize a symmetrical output current:

State 1: increasing $\left|I_{out}^{+}\right|$ to $\left|I_{out}^{-}\right|$,

State 2: decreasing $\left|I_{out}^{-}\right|$ to $\left|I_{out}^{+}\right|$,

State 3: For the current value $\left|I_X\right|$ which is between $\left|I_{out}^{+}\right|$ and $\left|I_{out}^{-}\right|$, decreasing $\left|I_{out}^{-}\right|$ to $\left|I_X\right|$ and increasing $\left|I_{out}^{+}\right|$ to $\left|I_X\right|$.

To realise one of these states above, the transistor dimension from (2) and (3) is to be change. The dimension of the critical transistors for operation at $V_{DD}/V_{SS}=\pm 5V$ are illustrated in Table 3. It can be observed that changing at leased one of the critical transistor dimensions a symmetrical output current characteristic can be provided.

Due to the transistor dimension changing, the linear range of the current transfer characteristic changes. Therefore, it can also a function be used, for all states separately, which provides the symmetrical output current for several power supply voltages. With such a function it can be easier acceptable transistor dimension founded which can be realisable. The function, for state one, is illustrated in (15) and (16). Since, in state one are only two critical transistor dimension changeable, there can also be two function be found to provide a symmetrical output current:

$$W_6 = V_{DD} \cdot \begin{pmatrix} 28.4974 - 31.9727 \cdot V_{DD} + 18.3467 \cdot V_{DD}^2 \\ -5.5763 \cdot V_{DD}^3 + 0.8550 \cdot V_{DD}^4 - 0.05184 \cdot V_{DD}^5 \end{pmatrix} \quad (13)$$

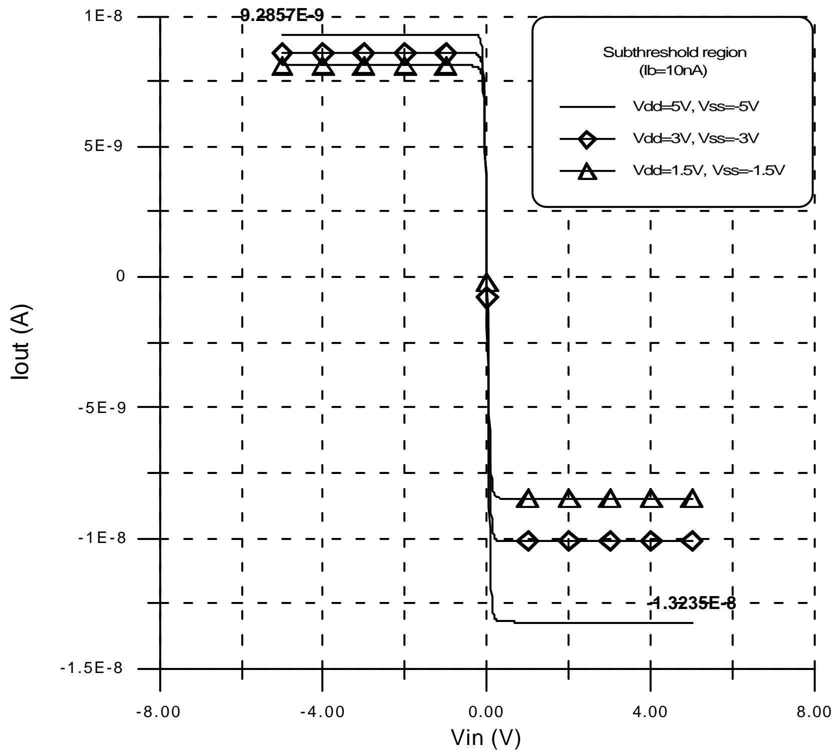

Figure 5. Current transfer characteristic for the subthreshold region.

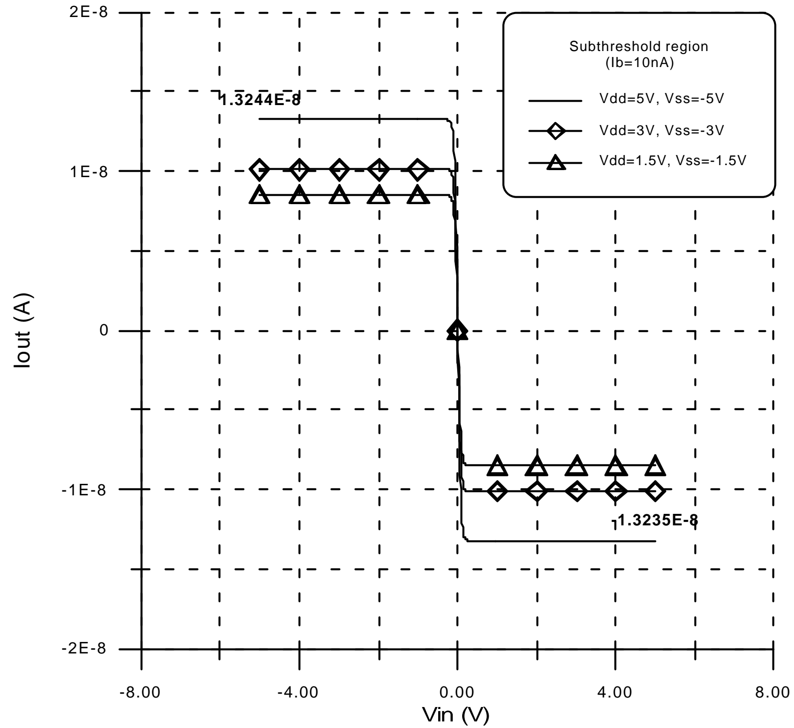

Figure 6. Current transfer characteristic with the new transistor dimension for the subthreshold region.

TABLE 1
MOS TRANSISTOR DIMENSIONS OF THE CMOS SYMMETRICAL OTA.

	M_1	M_2	M_3	M_4	M_5	M_6	M_7	M_8	M_{15}	M_{16}	M_{21}	M_{22}	M_{23}
W (µm)	5	5	12	12	10	10	5	5	5	5	5	5	5
L (µm)	3	3	3	3	3	3	3	3	3	3	3	3	3

TABLE 2
MOS TRANSISTOR MODEL PARAMETERS (TUBITAK 3µm MODEL PARAMETERS) OF THE CMOS SYMMETRICAL OTA.

.MODEL MN NMOS LEVEL=2 LD=1e-7 TOX=4.5E-8
+VTO=0.9 KP=4.4E-5 GAMMA=0.22 PHI=0.58 UEXP=0.15 UCRIT=60000 DELTA=1 +XJ=2.5E-7 LAMBDA=0.035 NFS=1E11 RSH=35 CJ=1.1E-4 +MJ=0.5 CJSW=3E-10 +MJSW=0.4 PB=0.7 XQC=1 WD=3E-7 JS=25E-6
.MODEL MP PMOS LEVEL=2 LD=1e-7 TOX=4.5E-8
+VTO=-1.0 KP=1.5E-5 GAMMA=0.7 PHI=0.7 UEXP=0.17 UCRIT=40000 DELTA=1
+XJ=3.5E-7 LAMBDA=0.035 NFS=1E11 RSH=100 CJ=1.9E-4 MJ=0.3 CJSW=6.3E-10 +MJSW=0.35 PB=0.7 XQC=1 WD=4E-7 JS=1.6E-6

TABLE 3
CRITICAL TRANSISTOR DIMENSIONS TO REALIZE A SYMMETRICAL OUTPUT CURRENT CHARACTERISTIC FOR $V_{DD}/V_{SS}=\pm 5V$.

State 1	State 2	State 3
$\left(\frac{W}{L}\right)_6=\left(\frac{W}{L}\right)_5\cdot 1.30$ or $\left(\frac{W}{L}\right)_4=\left(\frac{W}{L}\right)_3\cdot 0.75$	$\left(\frac{W}{L}\right)_5=\left(\frac{W}{L}\right)_6\cdot 0.77$ or $\left(\frac{W}{L}\right)_8=\left(\frac{W}{L}\right)_7\cdot 0.80$ or $\left(\frac{W}{L}\right)_3=\left(\frac{W}{L}\right)_4\cdot 1.35$ or $\left(\frac{W}{L}\right)_7=\left(\frac{W}{L}\right)_8\cdot 1.27$	For the value $\lvert I_X \rvert$, at leased one of the transistor dimension changing from state 1 and state 2 must be done.

$$W_4=V_{DD}\cdot\begin{pmatrix}2.49725-2.07317V_{DD}+0.85315V_{DD}^2\\ -1.8906V_{DD}^3+0.2140V_{DD}^4-0.00967V_{DD}^5\end{pmatrix} \quad (14)$$

Applying (14) to the CMOS symmetrical OTA in Figure 1 with the dimension from Table 1 for V_{DD}=+5V we find a new dimension value for the transistor M_4 as $\left(\frac{W}{L}\right)_4=\frac{9}{3}$. With this new dimension value the current transfer characteristic is shown in Figure 6. It can be observed that the boundaries of the output current are specified as $\lvert I_{out}^{+}\rvert = 13.2nA$ and $\lvert I_{out}^{-}\rvert = 13.22nA$, respectively. Note that symmetrical boundaries are obtained with the introduced improvement. The OTA is fabricated with TUBITAK 3µm technology. The measured variation of OTA transconductance, G_m, with the control voltage, V_{con}, and with the biasing current, I_B, is given in Figure 7. The measured frequency response of the OTA transconductance in subthreshold region is illustrated in Figure 8.

5. CONCLUSION

OTAs operating in the subthreshold region provide the requirements for low voltage and low power. Although the output current characteristic is not symmetrical for the conventionally designed CMOS OTA, a symmetrical characteristic can be obtained by changing one of the OTAs transistor dimensions. To provide this, three possible states for a change of MOS transistor dimensions are proposed. These changes influence theOTAs performance parameters such as transconductance (G_m), frequency response and the levelof the maximum input signal. An increase in these values is only possible for the state one because of increasing $\lvert I_{out}^{+}\rvert$ to $\lvert I_{out}^{-}\rvert$. Therefore, the state two only increases the output resistance because of the decreasing $\lvert I_{out}^{-}\rvert$ to $\lvert I_{out}^{+}\rvert$. Furthermore, the maximum input signal level is the same as with the unchanged transistor dimension used condition. The improvement provided by State three depends on $\lvert I_X \rvert$. If the value of $\lvert I_X \rvert$ is near to $\lvert I_{out}^{+}\rvert$ then it provides a similar improvement as in state one, if $\lvert I_X \rvert$ is closer to $\lvert I_{out}^{-}\rvert$ then it provides a similar improvement as in state two. From this point of view, state one is more preferred than the other states but in some conditions a realizable transistor dimension can be found providing the output current symmetry. In such a condition, state three or at least state two can be used to find out a realizable transistor dimension. In the most conditions, state one is enough to provide the symmetrical output current. Furthermore, an increase in the supply

voltage also increases the effect of the channel length modulation.

In summary, a method to provide the symmetrical output current of the CMOS symmetrical OTA operating in the subthreshold region has been presented. The realizability in VLSI design techniques is easy because the transistor dimension value of every state has a width range to obtain the symmetrical output current. From the technical point of view, this method can be used in all present-day VLSI technologies.

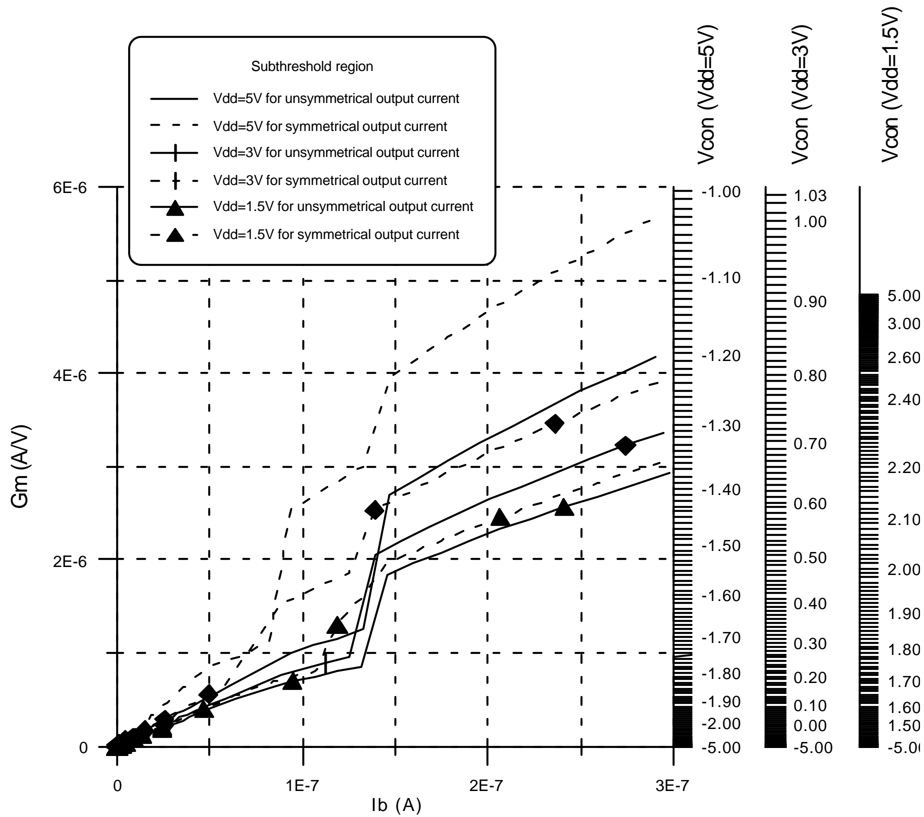

Figure 7. Measured variation of OTA transconductance, G_m, with the control voltage, V_{con}, and with the biasing current, I_B.

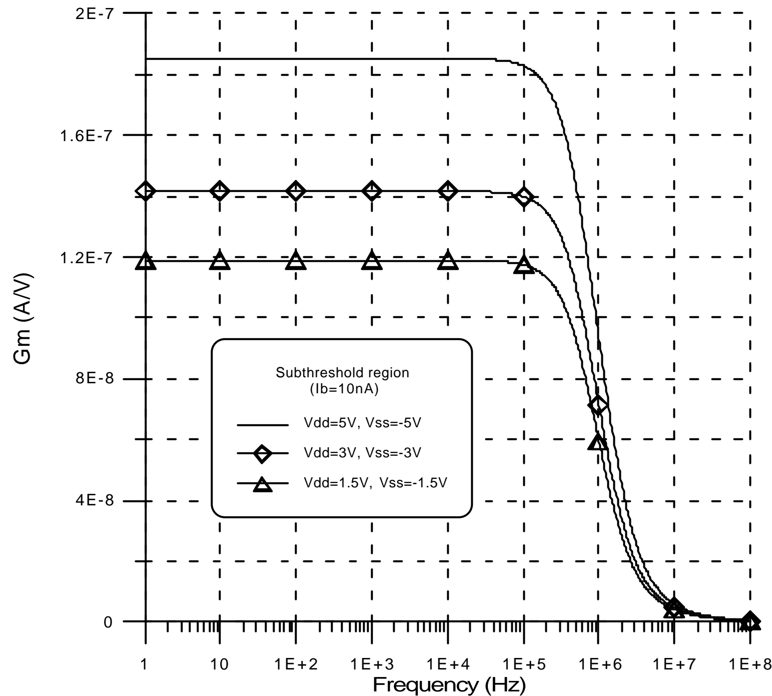

Figure 8. Measured frequency response of the OTA transconductance in subthreshold region.

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