A.Yeşil and F. Kaçar / IU-JEEE Vol. 12(2), (2012), 1493-1497

ELECTRONIC TUNABLE BIQUAD FILTER EMPLOYING DXCCII

Abdullah YEŞİL, Fırat KAÇAR

Department of Electrical and Electronics Engineering
Istanbul University, Istanbul, Turkey
E-mails: abdullah.yesil@istanbul.edu.tr, fkacar@istanbul.edu.tr

Abstract: *In this paper, we present dual-X current conveyor (DXCCII) based current-mode tunable universal filters. The proposed tuneable universal filter with single-input and three-outputs can simultaneously realize current-mode high-pass (HP), band-pass (BP) and low-pass (LP) filters employing two DXCCIIs, two grounded capacitors and two NMOS transistors.* Besides electronic tuneability with the control voltage *applied to the gate, the topology proposed exhibits also low active and passive sensitivity. Literature survey shows that the proposed circuit employs minimum number of passive and active components among the DXCCII based filters. Non-ideal and parasitic effects are investigated and discussed. We performed simulations with PSPICE simulation program. Simulation results are given to confirm the theoretical analysis.*

Keywords: : *Analog MOS Integrated Circuit, Current-Mode Filter, DXCCII, Electronically Tunable,*

1. Introduction

In electrical engineering, it is well-known fact that electronically tunable filters are very important building blocks for analog signal processing applications. CCII based building blocks seem to be flexible and suitable for design and implementation of tunable filters. Consequently, filter topologies, providing electronically tuneability for natural frequency ω_o and quality factor Q, are remarkably attractive for the filter realization. Several implementations of current mode single-input three-outputs or multi-inputs single output filters based on current conveyors have been reported in the literature [1]-[8]. These current-mode universal filters employ at least three active components and at least four passive component. Besides, these filters are not tunable [1]-[4]. Some other filters are tunable, but they employ at least three active components [5]-[8]. Many studies performed on DXCCII-based topologies have been presented. DXCCII based current-mode inductance-simulators, oscillators, gyrator, FDNR and rectifier circuits were proposed and published in the literature [9]-[16]. A current-mode universal filter using two DXCCIIs, two grounded capacitors and three NMOS transistors was presented in [13]. But this circuit realizes only LP and BP filters. Yüce et al. [14] proposed current mode universal filter employing two DXCCIIs, one DO-ICCII, two grounded capacitors and two NMOS transistors. The work by Minaei [15] reported universal current-mode universal filter circuit employing three DXCCIIs, two grounded capacitors and four NMOS transistors. The last comparison, Kaçar et al. [16] proposed current-mode universal filter using three DXCCIIs, two grounded capacitors and three NMOS transistors.

In this paper, a current mode electronically tunable DXCCII universal filter is proposed. The proposed circuit configuration employs two DXCCIIs, two grounded capacitors and two NMOS transistors which provide the advantage of an electronically tuning capability. Furthermore, it exhibits high impedance output which enables easy cascading in current mode. The filter circuit can generate the standard filter functions (HP, BP and LP). From the comparisons given above, one can see that the proposed circuit employs minimum passive and active components. Furthermore, no critical component matching conditions are required; in addition, active and passive sensitivities are low.

2. Circuit Description

The terminal relations of a DXCCII as shown in Figure 1, can be characterized by

$$\begin{bmatrix} I_Y \\ V_{X_P} \\ V_{X_N} \\ I_{Z_P} \\ I_{Z_N} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ \beta_p & 0 & 0 \\ -\beta_n & 0 & 0 \\ 0 & \alpha_p & 0 \\ 0 & 0 & \alpha_n \end{bmatrix} \begin{bmatrix} V_Y \\ I_{X_P} \\ I_{X_N} \end{bmatrix} \quad (1)$$

Received on: 11.04.2012
Accepted on: 28.06.2012

where ideally $\beta_p = \beta_n = 1$ and $\alpha_p = \alpha_n = 1$ which represent the voltage and current transfer ratios of the DXCCII respectively. It is clear that for the ideal case of DXCCII the Y terminal exhibits infinite input impedance. The two X ports exhibit zero output impedance and the two Z ports infinite output impedance. The DXCCII brings some facilities as active element. A MOS transistor connected between X terminals with balanced differential voltage acts as linear resistance. The resistance value can be adjusted with the voltage applied to the gate [13].

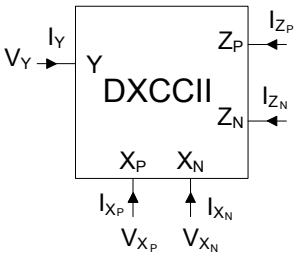

Figure 1. The circuit symbol of the DXCCII

The proposed circuit configuration is illustrated in Figure 2. The proposed current-mode universal filter with single-input three-outputs can realize HP, BP and LP filters; it is constructed employing two DXCCIIs, two grounded capacitors and two NMOS resistors. The circuit exhibits high output impedance, so it enables easy cascadability and can be tuned electronically. The resistances of the NMOS transistors in Figure 2 can be found as [13],

$$R_{Mi} = \frac{1}{\mu_n C_{ox}\left(\frac{W}{L}\right)_i \left(V_{Gi} - V_T\right)} \tag{2}$$

where μ_n is carrier mobility, C_{ox} is the gate oxide capacitance per unit area. W_i and L_i are the channel width and length of i^{th} transistor and V_T is the threshold voltage of the MOSFET, the resistance value is tunable via V_{Gi} of i^{th} transistor.

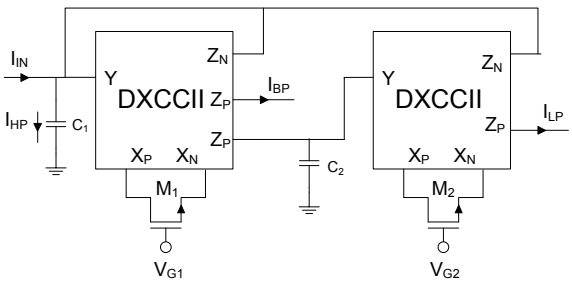

Figure 2. The proposed universal filter employing DXCCII

The routine analysis yields the following for the transfer functions:

$$\frac{I_{HP}}{I_{IN}} = \frac{s^2 C_1 C_2 R_{M1} R_{M2}}{4 + 2sC_2 R_{M2} + s^2 C_1 C_2 R_{M1} R_{M2}} \tag{3}$$

$$\frac{I_{BP}}{I_{IN}} = \frac{2sC_2 R_{M2}}{4 + 2sC_2 R_{M2} + s^2 C_1 C_2 R_{M1} R_{M2}} \tag{4}$$

$$\frac{I_{LP}}{I_{IN}} = \frac{4}{4 + 2sC_2 R_{M2} + s^2 C_1 C_2 R_{M1} R_{M2}} \tag{5}$$

The natural frequency (ω_0) and quality factor (Q) can be given as follows;

$$\omega_0 = \frac{2}{\sqrt{C_1 C_2 R_{M1} R_{M2}}} \tag{6}$$

$$Q = \sqrt{\frac{C_1 R_{M1}}{C_2 R_{M2}}} \tag{7}$$

3. Non-ideal analysis

Transfer functions of proposed circuit are derived and given for non-idealities. Non-ideality analysis considering the current and voltage tracking errors are carried out for these circuits. Taking the DXCCII non-idealities into consideration and rearranging the terminal relations given in Eqn.1, the filter transfer functions must be re-written by using $\beta_j = 1 - \varepsilon_{vj}$ and $\alpha_j = 1 - \varepsilon_{ij}$ for j=1,2. Besides, β_{pi}, β_{ni} and α_{pi}, α_{ni} represent the parameters β_p, β_n and α_p, α_n of the i^{th} DXCCII. Non-ideal equations for the proposed circuit are given at (8-10).

$$\frac{I_{HP}}{I_{IN}} = \frac{s^2 C_1 C_2 R_{M1} R_{M2}}{\alpha_{N2}\alpha_{P1}(\beta_{N1}+\beta_{P1})(\beta_{N2}+\beta_{P2}) + sC_2 R_{M2}\alpha_{N1}(\beta_{N1}+\beta_{P1}) + s^2 C_1 C_2 R_{M1} R_{M2}} \tag{8}$$

$$\frac{I_{BP}}{I_{IN}} = \frac{sC_2 R_{M2}\alpha_{P1}(\beta_{N1}+\beta_{P1})}{\alpha_{N2}\alpha_{P1}(\beta_{N1}+\beta_{P1})(\beta_{N2}+\beta_{P2}) + sC_2 R_{M2}\alpha_{N1}(\beta_{N1}+\beta_{P1}) + s^2 C_1 C_2 R_{M1} R_{M2}} \tag{9}$$

$$\frac{I_{LP}}{I_{IN}} = \frac{\alpha_{P1}\alpha_{P2}(\beta_{N1}+\beta_{P1})(\beta_{N2}+\beta_{P2})}{\alpha_{N2}\alpha_{P1}(\beta_{N1}+\beta_{P1})(\beta_{N2}+\beta_{P2}) + sC_2 R_{M2}\alpha_{N1}(\beta_{N1}+\beta_{P1}) + s^2 C_1 C_2 R_{M1} R_{M2}} \tag{10}$$

In this case, the modified natural frequency (ω_0') and quality factor (Q') can be given as follows

$$\omega_0' = \sqrt{\frac{\alpha_{P1}\alpha_{N2}(\beta_{N1}+\beta_{P1})(\beta_{N2}+\beta_{P2})}{C_1 C_2 R_{M1} R_{M2}}} \tag{11}$$

$$Q' = \sqrt{\frac{C_1 R_{M1}\alpha_{N2}\alpha_{P1}(\beta_{N2}+\beta_{P2})}{C_2 R_{M2}\alpha_{N1}^2(\beta_{N1}+\beta_{P1})}} \tag{12}$$

The modification of natural frequency and quality factor due to tracking errors can be compensated by voltage gates V_{Gi}. The sensitivity analyses with respect to the active and passive parameter can be calculated as follows:

$$\begin{aligned} &-S_{R_{M1}}^{\omega_0} = -S_{R_{M2}}^{\omega_0} = -S_{C_1}^{\omega_0} = -S_{C_2}^{\omega_0} = S_{\alpha_{P1}}^{\omega_0} = S_{\alpha_{N2}}^{\omega_0} = \frac{1}{2}, \quad S_{\alpha_{N1}}^{\omega_0} = S_{\alpha_{P2}}^{\omega_0} = 0, \\ &S_{\beta_{N1}}^{\omega_0} = \frac{\beta_{N1}}{2(\beta_{N1}+\beta_{P1})}, \quad S_{\beta_{P1}}^{\omega_0} = \frac{\beta_{P1}}{2(\beta_{N1}+\beta_{P1})}, \quad S_{\beta_{N2}}^{\omega_0} = \frac{\beta_{N2}}{2(\beta_{N2}+\beta_{P2})}, \quad S_{\beta_{P2}}^{\omega_0} = \frac{\beta_{P2}}{2(\beta_{N2}+\beta_{P2})} \end{aligned} \tag{13}$$

$$S_{R_{M1}}^{Q'}=-S_{R_{M2}}^{Q'}=S_{C_1}^{Q'}=-S_{C_2}^{Q'}=S_{\alpha_{N2}}^{Q'}=S_{\alpha_{P1}}^{Q'}=\frac{1}{2},\qquad S_{\alpha_{N1}}^{Q'}=-1,\qquad S_{\alpha_{P2}}^{Q'}=0,$$
$$S_{\beta_{N2}}^{Q'}=\frac{\beta_{N2}}{2(\beta_{N2}+\beta_{P2})},\qquad S_{\beta_{P2}}^{Q'}=\frac{\beta_{P2}}{2(\beta_{N2}+\beta_{P2})},\qquad S_{\beta_{N1}}^{Q'}=-\frac{\beta_{N1}}{2(\beta_{N1}+\beta_{P1})},\qquad S_{\beta_{P1}}^{Q'}=-\frac{\beta_{P1}}{2(\beta_{N1}+\beta_{P1})} \tag{14}$$

It can be seen that the active and passive sensitivities are equal to or less than 0.5 in magnitude (excluding α_{N1}) and it has low active and passive sensitivities.

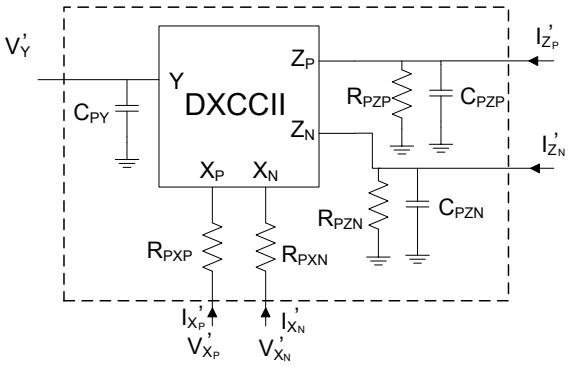

Figure 3. Parasitic resistors and capacitors of DXCCII

Parasitic impedances of DXCCII are shown in Figure 3. The real DXCCII has parasitic resistors and capacitors at terminal Z_P, Z_N and Y to the ground, and a serial resistor at the input terminals X_P and X_N. Considering the DXCCII parasitic impedances, the transfer functions of the proposed circuit are obtained and given in (15-17) for non-ideal case.

$$\frac{I_{HP}}{I_{IN}}=\frac{s^2C_1C_2'R_{M1}'R_{M2}'R_{P1}R_{P2}+sC_1R_{M1}'R_{M2}'R_{P1}}{R_{M1}'R_{M2}'+2R_{M2}'R_{P1}+4R_{P1}R_{P2}+sC_1'R_{M1}'R_{M2}'R_{P1}+sR_{M2}'C_2'(R_{M1}'+2R_{P1})R_{P2}+s^2C_1'C_2'R_{M1}'R_{M2}'R_{P1}R_{P2}} \tag{15}$$

$$\frac{I_{BP}}{I_{IN}}=\frac{2R_{M2}'R_{P1}+2sC_2'R_{M2}'R_{P1}R_{P2}}{R_{M1}'R_{M2}'+2R_{M2}'R_{P1}+4R_{P1}R_{P2}+sC_1'R_{M1}'R_{M2}'R_{P1}+sR_{M2}'C_2'(R_{M1}'+2R_{P1})R_{P2}+s^2C_1'C_2'R_{M1}'R_{M2}'R_{P1}R_{P2}} \tag{16}$$

$$\frac{I_{LP}}{I_{IN}}=\frac{4R_{P1}R_{P2}}{R_{M1}'R_{M2}'+2R_{M2}'R_{P1}+4R_{P1}R_{P2}+sC_1'R_{M1}'R_{M2}'R_{P1}+sR_{M2}'C_2'(R_{M1}'+2R_{P1})R_{P2}+s^2C_1'C_2'R_{M1}'R_{M2}'R_{P1}R_{P2}} \tag{17}$$

where $R_{M1}'=R_{M1}-R_{PXP}-R_{PXN}$, $R_{M2}'=R_{M2}-R_{PXP}-R_{PXN}$, $R_{P1}=R_{PZN}/2$, $R_{P2}=R_{PZP}$ and $C_1'=C_1+C_{PY}+2C_{PZN}$, $C_2'=C_2+C_{PY}+C_{PZP}$ are consisted of these parasitic capacitances or resistances. At the X terminals parasitic series resistances decrease effective resistances, while at the Z and Y terminals parasitic parallel capacitances increase effective capacitances. In effects of parasitic impedance case, natural frequency (ω_0'') and quality factor (Q'') of the proposed circuit is found as,

$$\omega_0''=\frac{\sqrt{\frac{4}{R_{M1}'R_{M2}'}+\frac{2}{R_{M1}'R_{P2}}+\frac{1}{R_{P1}R_{P2}}}}{\sqrt{C_1'C_2'}} \tag{18}$$

$$Q''=\frac{\sqrt{C_1'C_2'}\sqrt{\frac{4}{R_{M1}'R_{M2}'}+\frac{2}{R_{M1}'R_{P2}}+\frac{1}{R_{P1}R_{P2}}}}{\frac{C_1'}{R_{P2}}+C_2'\left(\frac{1}{R_{P1}}+\frac{2}{R_{M1}'}\right)} \tag{19}$$

From (18) and (19), it can be easily observed that magnitude values of the natural frequency (ω_0'') and quality factor (Q'') change, depending on values of parasitic impedances.

4. Simulations

The applicability of the proposed universal filter, shown in Figure 2, was demonstrated with SPICE simulations. The simulations were performed using PSPICE program with TSMC CMOS 0.35 μm process of the CMOS realization of DXCCII [13]. Table 1 lists the dimensions of MOS transistors in CMOS DXCCII circuit used for simulations. Supply voltages are taken as $V_{DD}=-V_{SS}=2.5V$ and $V_{bias}=1.265V$ biasing voltages are used.

Table 1. Transistor dimensions for CMOS DXCCII

Transistors	W(μm)	L(μm)
M1,M2	3	1.5
M3,M7,M8	6	1.5
M4,M5	5	1.5
M6,M9,M10	10	1.5
M11-M20	20	1.5

The dimensions of the NMOS transistors M_1 and M_2 in the proposed filter of Figure 2 are selected as $(W/L)_i=7\mu m/7\mu m$ and $C_1=C_2$=100pF which results in a quality factor of Q=1 and 933 kHz ideal center frequency.

The control voltages of the NMOS transistors are selected as $V_{G1}=V_{G2}=2.5$ V. Figure 4 shows the simulated frequency responses for the HP, BP and LP configurations. To demonstrate the tuneability of the proposed filter, different values V_{Gi} as 1V, 1.5V and 2.5V are selected to obtain center frequencies of 280 kHz, 525 kHz and 933 kHz, respectively. The results are shown for the band-pass response in Figure 5. When considering the influences of the parasitic impedances, simulation result of center frequency is larger than the ideal condition.

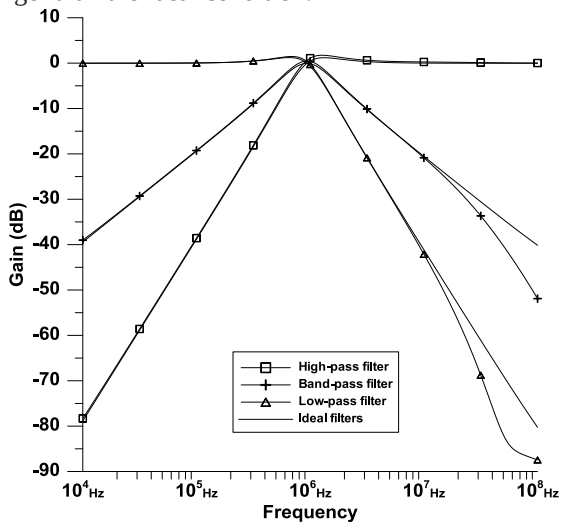

Figure 4. The simulated results of the gain–frequency responses of Figure 2

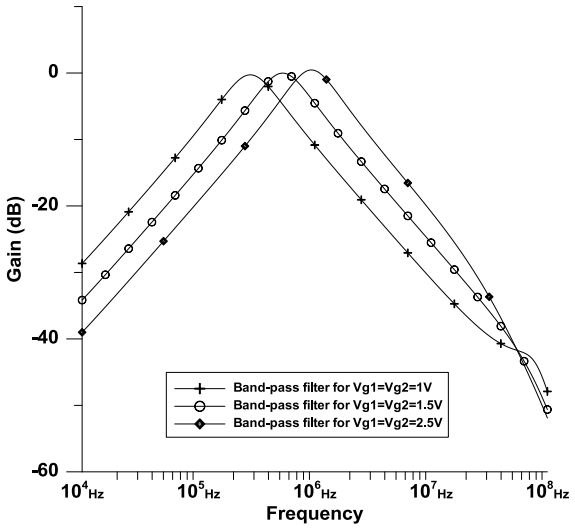

Figure 5. Gain of the band-pass response for various V_{Gi}

Time domain analysis result is given in Fig. 6 for 80μA sine wave at 933 kHz input for band-pass filter. The large signal behavior of the circuit was tested by investigating the dependence of the output harmonic distortion of the band-pass response on the input signal amplitude. Fig. 7 shows that the harmonic distortion increases rapidly. Below 200 μA(p-p), the total harmonic distortion (THD) is in acceptable limits of the order of 2%. The simulated responses with PSPICE have been quite good over a wide frequency range.

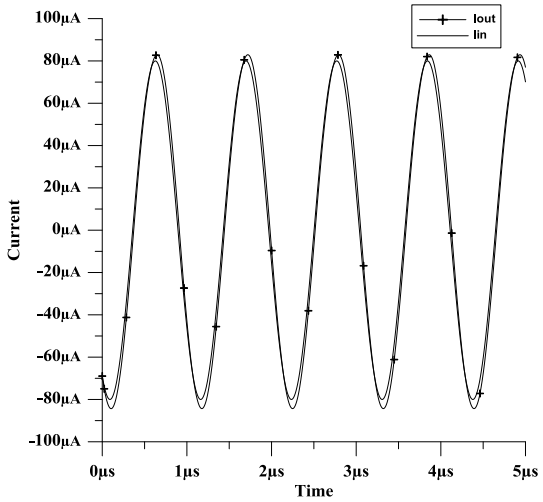

Figure.6 Time domain response of band-pass filter configuration

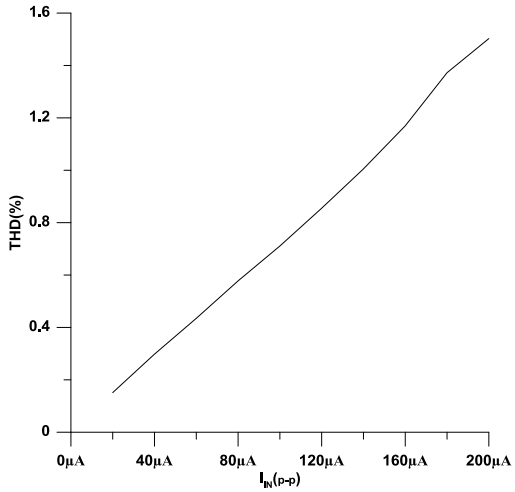

Figure. 7 Dependence of the output harmonic distortion of the band-pass filter on the input signal amplitude

5. Conclusions

In this paper, a current mode universal filter with single-input three outputs is presented. This circuit has the following advantages:
(i) can be tuned electronically.
(ii) employs minimum passive and active components.
(iii) does not require any parameter matching condition.
(iv) realizes standard filter functions without changing the circuit topology.
(v) has low active and passive sensitivities.
(vi) has grounded capacitors, which is advantageous from the viewpoint of integrated circuit manufacturing.
PSPICE simulation results are given to verify the theory. It will be seen that simulation results verify theory. The proposed filter circuits can be considered another good alternative for the filter designer

6. References

[1] O. Çiçekoğlu, "Current-mode biquad with a minimum number of passive elements", *IEEE Trans. Circuits Syst.-II: Analog Digit. Signal Process. vol.*48, 2001, pp.221–222.

[2] A. Toker, S. Özoğuz and C. Acar, "Current-mode KHN-equivalent biquad using CDBAs", *Electron. Lett. vol.*35, 1999, pp.1682–1683.

[3] W. Chunhua, Z. Deshu, Y. Jianzhuo, S. Chen, X. Chen, C. Jianxin, G. Guo and S. Guangdi, "A MOCCII current-mode KHN filter and its non-ideal characteristic research", *4th Int. Conf. ASIC*, Shanghai, China, 2001, pp.289–292.

[4] M. Soliman, "Voltage mode and current mode Tow Thomas bi-quadratic filters using inverting CCII", *Int. J. Circuits Theory Appl., vol.*35, 2007, pp.463–467.

[5] E. Altuntas and A. Toker, "Realization of voltage and current mode KHN biquads using CCCIIs", *Int. J. Electron. Commun. vol.*56, 2002, pp.45–49.

[6] M-A. İbrahim, S. Minaei and H. Kuntman "A 22.5MHz current-mode KHN-biquad using differential voltage current conveyor and grounded passive elements" *Int. J. Electron. Commun. (AEU),* vol.59, 2005, pp.311–318.

[7] S. Minaei and S. Türköz,"Current-Mode Electronically Tunable Universal Filter Using Only Plus-Type Current Controlled Conveyors and Grounded Capacitors" *ETRI Journal*, vol.26(4), 2004.

[8] J. Zhao, J-G. Jiang and J-N. Liu, "Design of tunable biquadratic filters employing CCCIIs: state variable block diagram approach" *Analog Integr Circ Sig Process,* vol.62, 2010, pp.397–406.

[9] A. Zeki and A. Toker, "DXCCII-based tunable gyrator", *International Journal of Electronics and Communications (AEÜ)*, vol.34(1), 2005, pp.59-62.

[10] F. Kaçar, B. Metin and H. Kuntman, "A New Dual-X CMOS Second Generation Current Conveyor (DXCCII) with a FDNR Circuit Application", *AEU: International Journal of Electronics and Communications* vol.64(8), 2010, pp.774-778.

[11] S. Minaei and E. Yüce "A new full-wave rectifier circuit employing single dual-X current conveyor" *International Journal of Electronics,* vol.95(8), 2008, pp.777–784.

[12] S. Yamaçlı and S. Özcan, "Novel Electronically Tunable Inductance Simulator Employing Dual-X Current Conveyors (DXCCIIs)", *IASTED Conference on Circuits, Signals and Systems (CSS 2004), Clearwater, Florida, U.S.A.*, 2004, pp.28-30.

[13] A. Zeki and A. Toker "The Dual-X Current Conveyor (DXCCII): A New Active Device For Tunable Continuous-Time Filters", *Int. J. Electron., vol.*89, 2002, pp.913–923.

[14] E. Yüce and S. Minaei "ICCII-Based Universal Current-Mode Analog Filter Employing Only Grounded Passive Components" *Analog Integr Circ Sig Process,* vol.58, 2009, pp.161–169.

[15] S. Minaei "Electronically Tunable Current-Mode Universal Biquad Filter Using Dual-X Current Conveyors" *Journal of Circuits, Systems, and Computers,* vol.18(4), 2009, pp.665–680.

[16] F. Kaçar, and H. Kuntman, "DXCCII based electronically tunable current-mode universal filter" *Signal Processing and Communications Applications Conference, SIU 2009. IEEE 17th*, pp.157 – 160.