NEW DXCCII-BASED GROUNDED SERIES INDUCTANCE SIMULATOR TOPOLOGIES

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Abstract: *In this paper, five grounded series inductance simulator topologies are proposed. All proposed circuits employing a minimum number of DXCCII and passive components. The proposed topologies realized all grounded parallel inductance variations. To demonstrate the performance of the presented DXCCII based parallel inductance simulators, we use one of the circuits to construct a current mode multifunction filter. Simulation results are given to confirm the theoretical analysis. The proposed DXCCII and its applications are simulated using CMOS 0.35 μm technology.*

Keywords: : *Analog MOS Integrated Circuit, inductance simulator, DXCCII*

1. Introduction

Inductance simulators are very important building for analog filter circuits design. The advantage of integrated circuits has encouraged the design of synthetic inductances, which can be used instead of the bulky inductors in passive filters. Several grounded inductance simulator topologies have been reported in the literature [1]-[22]. These topologies can be classified based on the number of active and passive elements employed and whether they realize a lossy or lossless kind of inductance. However, many of these circuits require more than two active components and three or more passive elements for grounded inductance simulation. Most of these circuits employ two or more active elements to realize grounded inductance [3]-[5], [7]-[9], and [12]. The proposed topologies in [1], [6], [10], and [11] employ a single active element but they do not realize pure inductance. Although the circuit reported in [5] realizes pure inductance with only one positive type second-generation current conveyor (CCII+), it employs five passive elements. In comparison to previous DXCCII based inductor simulator circuit [17], the number of active element reduced by one.

In this paper, we propose grounded inductance simulator topologies employing a minimum number of active and passive components including one dual-x second generation current conveyor (DXCCII), two resistors, and one capacitor. The proposed topologies realized all grounded series inductance variations. Finally, the proposed circuit is tested in the current-mode multifunction filter. Simulations of the circuits by the SPICE program give results that agree well with the theoretical results.

2. Proposed Circuit

The circuit symbol of the dual-x current conveyor (DXCCII) is shown in Fig.1. It has two X terminals, namely X_p (non-inverting X terminal) and X_n (inverting X terminal). The X_p and X_n terminal currents are reflected to the respective Z terminals, namely Z_p and Z_n [23]. The Y terminal is high impedance terminal and X_p, X_n terminals are low impedances. The Z_p and Z_n terminals are high impedance nodes suitable for current outputs.

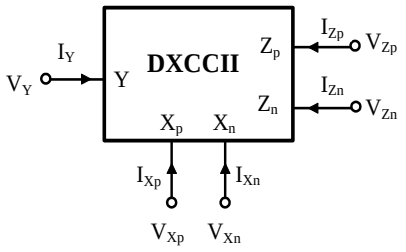

Figure 1. The symbol of the DXCCII

Using standard notation, the port relations of an ideal DXCCII shown in Fig.1 can be characterized by

$$\begin{bmatrix} I_Y \\ V_{Xp} \\ V_{Xn} \\ I_{Zp} \\ I_{Zn} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ \beta_1 & 0 & 0 \\ -\beta_2 & 0 & 0 \\ 0 & \alpha_p & 0 \\ 0 & 0 & \pm\alpha_n \end{bmatrix} \begin{bmatrix} V_Y \\ I_{Xp} \\ I_{Xn} \end{bmatrix} \quad (1)$$

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The proposed series lossless and lossy inductor simulators are given in Figs. 2a, 2b, 2c, 2d 2e. Routine analyses of the circuits in Figs. 2a-2e are given in Table 1. From Table 1 by comparison of various equations belonging to different circuits the following observations are possible: The circuit in Fig.2a and Fig.2b can simulate pure negative and positive inductance, respectively. The circuits which are shown in Fig.2b can simulate also series (+L) with (-R). Fig.2c circuit can simulate series (-L) with (-R). The circuit in Fig.2d. can simulate series (-L) with (+R). The last circuit in Fig.2e. can simulate series (+L) with (+R). Positive inductances can be used to implement filters. Negative inductances are especially important if the parasitics have to be cancelled.

α_p, α_n, β_1 and β_2 are considered in the analysis of the proposed inductance simulator circuit in Fig. 2. Non-ideality analysis with current and voltage tracking errors taken into account are carried out for each circuit separately. Non-ideal equations for each circuit are given in Table.2.

Table 1. The actively realizable inductance forms.

Circuit	Matching	Z_{eq}	L_{eq}	R_{eq}	Type
Fig. 2a	*No*	$Z_{eq} = -\frac{sCR_1R_2}{4}$	$L_{eq} = -\frac{sCR_1R_2}{4}$	-	Pure –L
Fig. 2b	$R_1=2R_2=2R$	$Z_{eq} = \frac{sCR_1R_2}{4} + \frac{R_2}{2} - \frac{R_1}{4}$	$L_{eq} = \frac{sCRR}{2}$	-	Pure L
Fig. 2b	$R_1=4R_2=4R$	$Z_{eq} = \frac{sCR_1R_2}{4} + \frac{R_2}{2} - \frac{R_1}{4}$	$L_{eq} = sCRR$	$R_{eq} = -\frac{R}{2}$	L with series –R
Fig. 2c	*No*	$Z_{eq} = -2sCR_1R_2 - R_1$	$L_{eq} = -2sCR_1R_2$	$R_{eq} = -R_1$	-L with series –R
Fig. 2d	$R_2=4R_1=R$	$Z_{eq} = \frac{-sCR_1R_2 + R_2}{2 + sC\ R_2 - 4R_1}$	$L_{eq} = -\frac{sCRR}{8}$	$R_{eq} = \frac{R}{2}$	-L with series R
Fig. 2e	*No*	$Z_{eq} = \frac{sCR_1R_2}{4} + \frac{R_1}{2}$	$L_{eq} = \frac{sCR_1R_2}{4}$	$R_{eq} = \frac{R_1}{2}$	L with series R

Table 2. DXCCII-based grounded series inductance circuits for the non-ideal case

Circuit	Z_{eq}	Matching
Fig. 2a	$\frac{sCR_1R_2\alpha_p\beta_1}{-\alpha_n\ 1+\alpha_p\ \ \beta_1+\beta_2\ +sC\ \ R_1\ 1+\alpha_p\ \ -1+\beta_1\ -R_2\ \alpha_n-\alpha_p\ \ \beta_1+\beta_2}$	No
Fig. 2b	$\frac{sCR_1R_2 + 2R_2 - R_1\alpha_p}{2 - 2sCR_2\ -1+\alpha_n\ +2\alpha_n\alpha_p}$	$R_1 = R_2\frac{2}{\alpha_p}$
Fig. 2b	$\frac{sCR_1R_2 + 2R_2 - R_1\alpha_p}{2 - 2sCR_2\ -1+\alpha_n\ +2\alpha_n\alpha_p}$	$R_1 = R_2\frac{4}{\alpha_p}$
Fig. 2c	$-\frac{sCR_1R_2\ 1+\alpha_p\ +R_1}{sCR_1\ 1+\alpha_p\ \ -1+\beta_1\ +\alpha_n\beta_2}$	No
Fig. 2d	$\frac{sCR_1R_2 - \alpha_p\beta_1R_2}{-\ 1+\alpha_n\ \alpha_p\beta_1 + sC\ \ -\alpha_p\beta_1R_2 + R_1\ 1+\alpha_n\ \ 1+\beta_2}$	$R_2 = \frac{R_1\ 1+\alpha_n\ \ 1+\beta_2}{\alpha_p\beta_1}$
Fig. 2e	$\frac{sCR_1R_2 + R_1\ 1+\alpha_p}{-\ 1+\alpha_p\ \ 1+\beta_2\ +sC\ \ R_1\ 1+\alpha_p\ \ -1+\beta_1\ +R_2\ -1+\alpha_n\ \ 1+\beta_2}$	No

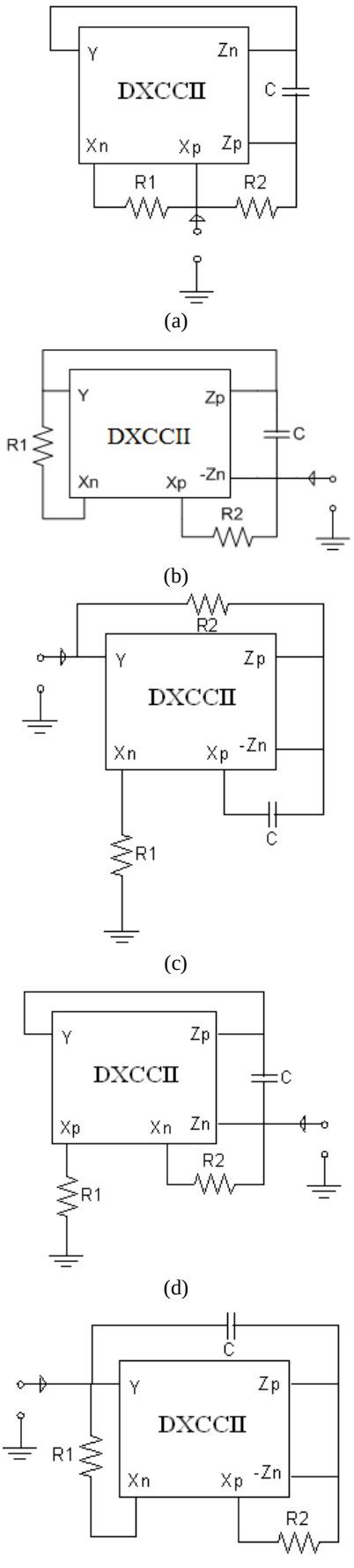

Figure 2. Inductance simulators realized using single DXCCII

3. Simulations

All of the circuits illustrated in Fig. 2 are tested with SPICE simulations. A possible CMOS realization of a DXCCII element is given in Fig.3. The cross-coupled quad configuration proposed by [24], shown in Fig.3, has superior linearity and input voltage range compared with conventional source-coupled differential pair. A high performance output stage, shown in Fig.3, is proposed by [25]. The two complementary current mirrors are composed of transistors M11-M24 and M25-M30. In the regulated-gate-cascade (RGC) parts [25] of the output stage high output impedance is achieved by the negative active-feedback loop along M22 and M28 the source follower M24 and M29. The series inductance configurations presented in this study are simulated using this CMOS-based DXCCII circuit. The supply voltages, are selected as V_{DD}=−V_{SS}=1.5V. The aspect ratios of the transistors are given in Table 3. The MOS transistors are simulated using TSMC CMOS 0.35µm process model parameters.

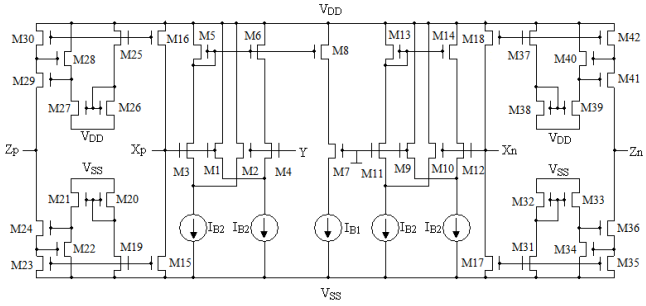

Figure 3. A CMOS implementation of the DXCCII

Table 3. Transistors aspect ratios for the proposed circuit

Transistors	W(µm)	L(µm)
M1-M4, M7, M9-M12	14	0.7
M5, M6, M8, M13, M14	28	0.7
M15, M17, M35-M36 M23-M24	21	0.7
M16, M18, M29, M30, M41,M42	7	0.7
M19, M25, M31,M37	2.1	0.7
M20-M21, M26-M27, M32-M33, M38-M39	1.75	0.7
M34, M22, M28, M40	0.7	0.7

To demonstrate the accuracy of the topology proposed, the frequency responses of the impedances obtained from ideal and simulated circuits are calculated. Furthermore a current-mode multifunction filter was realized as an application example by connecting a parallel capacitor and resistor to the circuit illustrated in Fig.6b. In this Fig actively simulated inductance simulator circuit in Fig.2b replaces the parallel L circuit. The transfer functions are given by

$$\frac{I_{HP}}{I_{IN}} = \frac{s^2}{s^2 + s\dfrac{1}{C_L R_L} + \dfrac{1}{C_L L_{eq}}} \qquad (2)$$

$$\frac{I_{BP}}{I_{IN}} = \frac{s\dfrac{1}{C_L R_L}}{s^2 + s\dfrac{1}{C_L R_L} + \dfrac{1}{C_L L_{eq}}} \quad (3)$$

$$\frac{I_{LP}}{I_{IN}} = \frac{\dfrac{1}{C_L L_{eq}}}{s^2 + s\dfrac{1}{C_L R_L} + \dfrac{1}{C_L L_{eq}}} \quad (4)$$

The element values of the realized filter are chosen as follows: C_L=0.1nF, R_L=1kΩ, R_1=2R_2=2R=1kΩ and C=0.8nF, thus an inductor with L_{eq}=0.1mH is obtained which result in a pole frequency f_p=1.59MHz. The designed filter circuit is simulated with PSPICE program using a CMOS realization of DXCCII shown in Fig 4. Simulated high-pass (I_{HP}) low-pass (I_{LP}) and band-pass (I_{BP}) responses of the current-mode multifunction filter are given in Fig. 5.

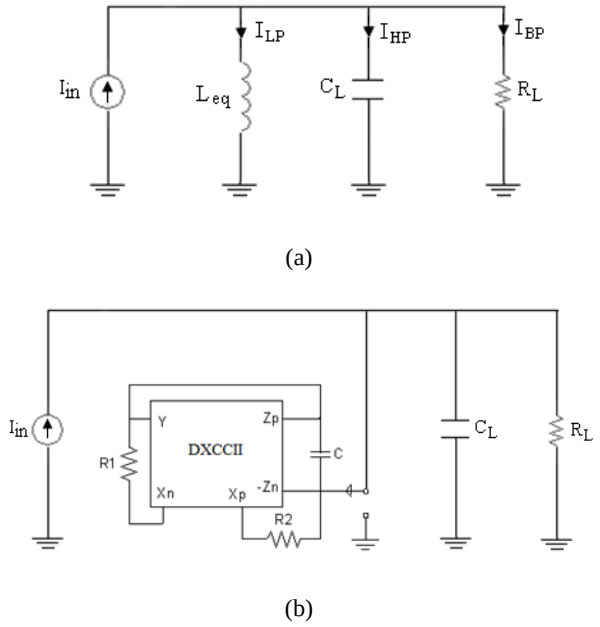

Figure 4. a) Passive multifunction filter b) Multifunction filter constructed with DXCCII inductance simulator

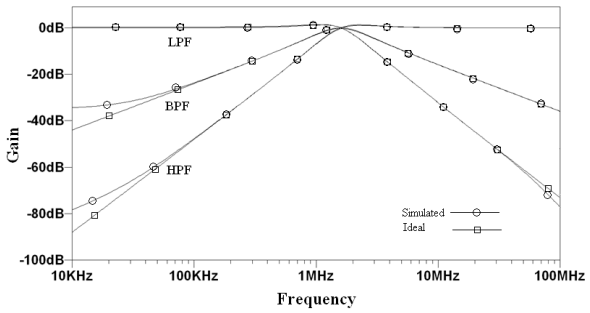

Figure 5. Ideal and simulated high-pass, low-pass and band-pass responses of the current-mode multifunction filter

Time domain analysis result is given in Fig.6 for peak-to-peak 100mV 1.59MHz sine wave input for band-pass filter configuration for the circuit in Fig 4b. Also in Fig.7, for an input signal of 100μA amplitude at 1MHz, variation of the THD value versus output load resistance is shown. For a load resistance lower than 20k, THD is low, less than 3%. Output amplitude change with load resistance for constant input signal is seen in Fig.7 it is seen that, at 1MHz frequency a large swing V_O=1.43V is obtained at the output.

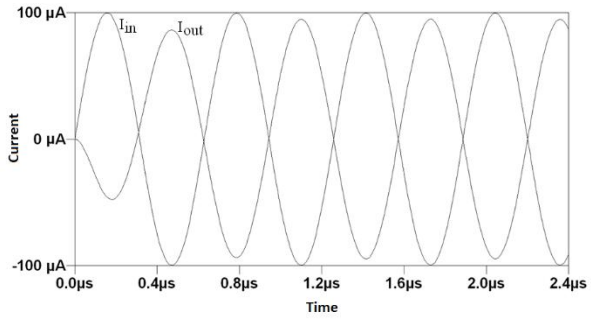

Figure 6. The input and output waveforms of the proposed band-pass filter of Fig. 4b for 1.59MHz sinusoidal input current of 200μV (peak to peak).

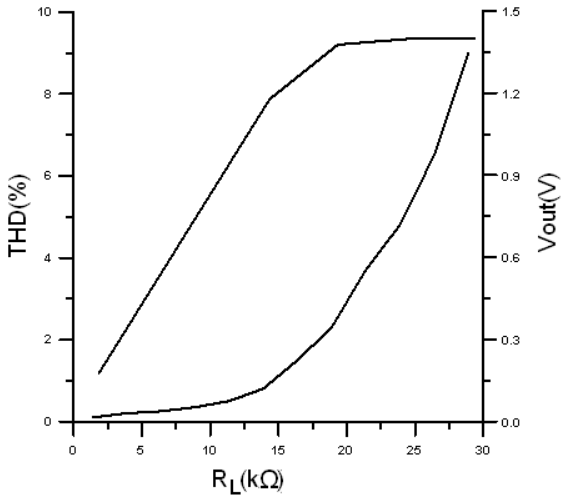

Figure 7. Total harmonic distortion and dependence of the output amplitude versus load resistance for an input signal of 100μA amplitude at 1MHz.

4. Conclusions

New single-DXCCII based lossless and lossy grounded series inductance simulation circuits have been presented. The proposed circuit employs a single DXCCII along with two resistors and a single capacitor. A second-order multifunction filter is realized to illustrate the practical uses of the proposed lossless inductor simulator as application example. The workability of the new circuit was demonstrated by using CMOS DXCCII known earlier [23].

Simulation results well confirm the theoretical analysis. With the availability of any off-the shelf IC DXCCII in future, the inductance simulation circuit proposed in this paper may find use in various analog signal processing signal/generation applications realizable with IC DXCCII.

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